GENERAL DESCRIPTION

The XR16M890[1] (M890) is a single-channel Universal Asynchronous Receiver and Transmitter (UART) with integrated level shifters and 128 bytes of transmit and receive FIFOs.

For flexibility in a mixed voltage environment, the M890 has 4 VCC pins. There is a VCC pin for the core, a VCC pin for the UART signals, a VCC pin for the CPU interface signals and a VCC pin for the GPIO signals. The VCC pins for the UART, GPIO and CPU interface signals allow for the M890 to interface with devices operating at different voltage levels eliminating the need for external voltage level shifters.

The Auto RS-485 Half-Duplex Direction control feature simplifies both the hardware and software for half-duplex RS-485 applications. In addition, the Multidrop mode with Auto Address detection and Address Byte Control features increase the performance by simplifying the software routines.

The Independent TX/RX Baud Rate Generator feature allows the transmitter and receiver to operate at different baud rates. In addition, the Fractional Baud Rate Generator feature provides flexibility for crystal/clock frequencies for generating standard and non-standard baud rates.

The M890 has programmable transmit and receive FIFO trigger levels, automatic hardware and software flow control, and data rates of up to 24 Mbps. Power consumption of the M890 can be minimized by enabling the sleep mode.

The M890 has a 16550 compatible register set that provide users with operating status and control, receiver error indications, and modem serial interface controls. An internal loopback capability allows onboard diagnostics. The M890 has a selectable Intel/Motorola/VLIO bus interface.

NOTE: *1 Covered by U.S. Patent #5,649,122.*

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OPS)

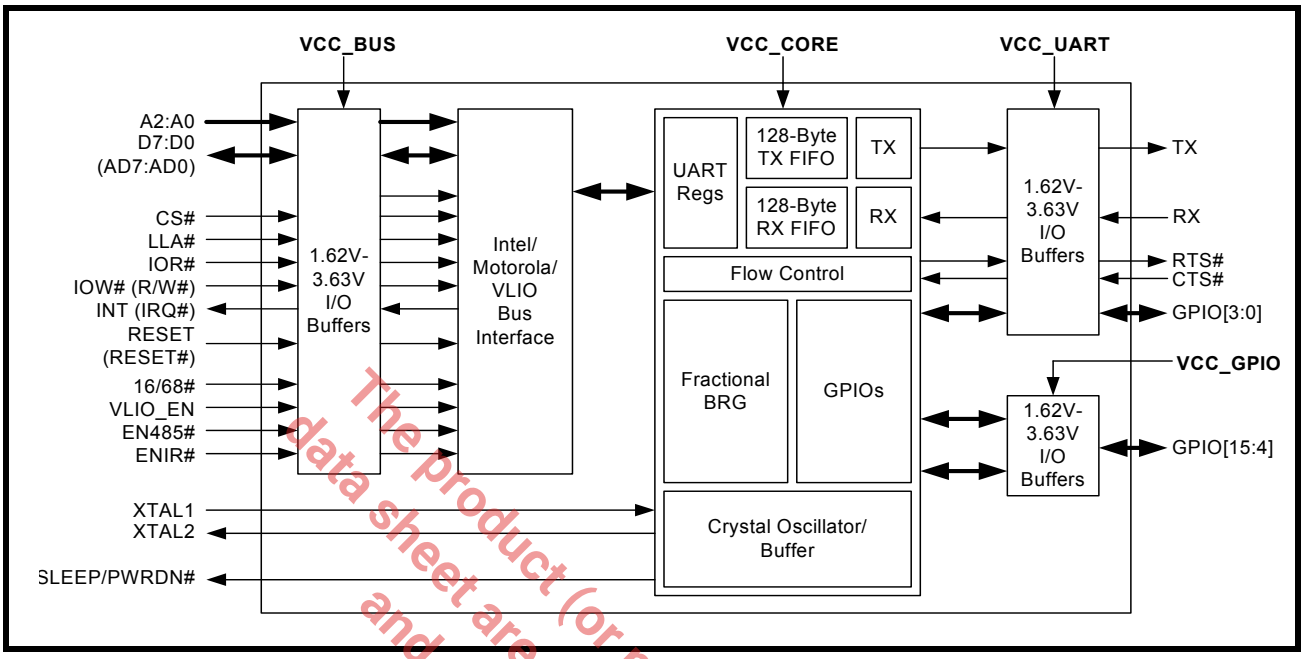
FEATURES

- Integrated Level Shifters on CPU interface, UART and GPIO signals
- Intel/Motorola/VLIO Bus Interface select
  - ’0’ ns address setup/hold times
- 24 Mbps maximum UART data rate
- Up to 16 GPIOs
- 128-Bytes TX and RX FIFOs
- Programmable TX/RX trigger levels
- TX/RX FIFO Level Counters
- Independent TX/RX Baud Rate Generator
- Fractional Baud Rate Generator
- Auto RTS/CTS Hardware Flow Control
- Auto XON/XOFF Software Flow Control
- Auto RS-485 Half-Duplex Direction Control
- Multidrop mode w/ Auto Address Detect (RX)
- Multidrop mode w/ Address Byte Control (TX)
- Sleep Mode with Automatic Wake-up
- Infrared (IrDA 1.0 and 1.1) mode
- 1.62V to 3.63V supply operation
- 5V tolerant inputs
- Crystal oscillator or external clock input

APPLICATIONS

- Personal Digital Assistants (PDA)
- Cellular Phones/Data Devices
- Battery-Operated Devices
- Global Positioning System (GPS)
- Bluetooth

FIGURE 1. XR16M890 BLOCK DIAGRAM



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF GPIOS	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16M890IL32-F	QFN-32	4	-40°C to +85°C	Active
XR16M890IL32TR-F	QFN-32	4	-40°C to +85°C	Active
XR16M890IL40-F	QFN-40	8	-40°C to +85°C	Active
XR16M890IL40TR-F	QFN-40	8	-40°C to +85°C	Active
XR16M890IM48-F	TQFP-48	16	-40°C to +85°C	Active
XR16M890IM48TR-F	TQFP-48	16	-40°C to +85°C	Active

NOTE: **TR = Tape and Reel, F = Green / RoHS**

FIGURE 2. PIN OUT ASSIGNMENTS - 48-PIN TQFP

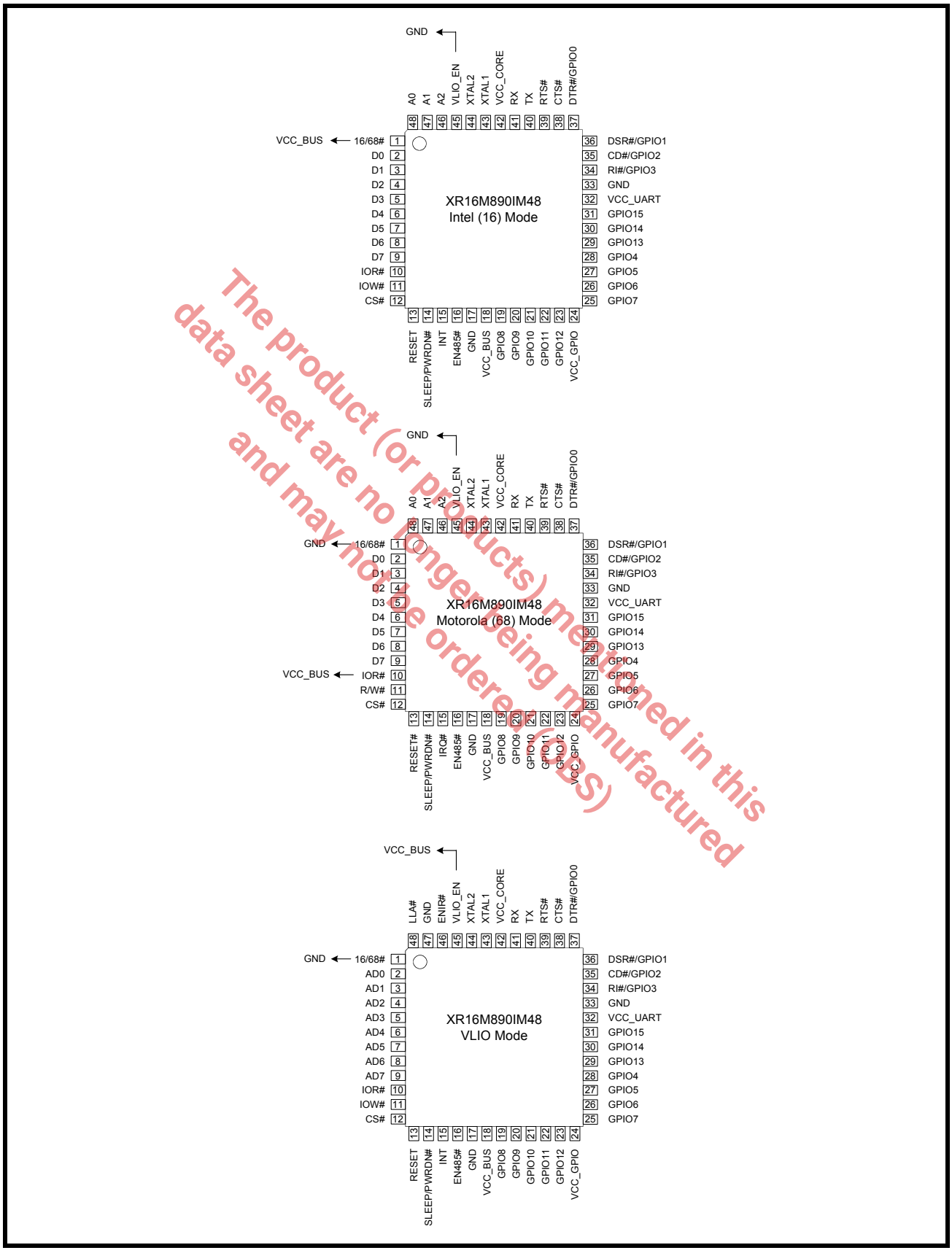


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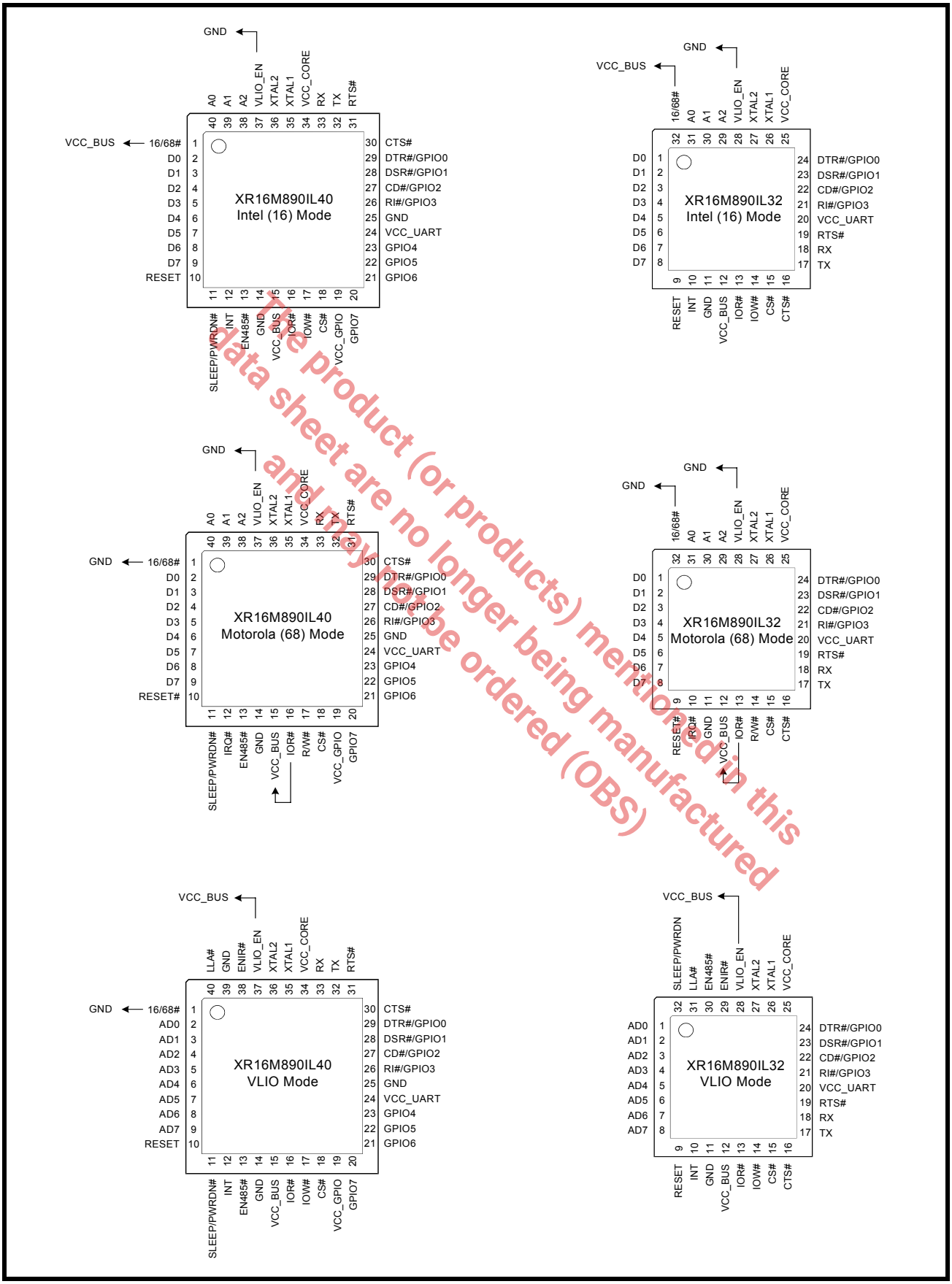
FIGURE 3. PIN OUT ASSIGNMENTS - 40-PIN QFN AND 32-PIN QFN



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PIN DESCRIPTIONS

Pin Description

NAME	QFN-32 PIN#	QFN-40 PIN#	TQFP-48 PIN#	TYPE	DESCRIPTION
DATA BUS INTERFACE - Intel/Motorola					
16/68#	32	1	1	I	Intel or Motorola Bus Select. This pin selects the 16 or 68 mode when VLIO_EN is a logic 0. In the VLIO mode (VLIO_EN is a logic 1), this pin becomes the SLEEP/PWRDN# pin in the QFN-32 package. When 16/68# pin is at logic 1, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When 16/68# pin is at logic 0, 68 or Motorola mode, the device will operate in the Motorola bus type of interface. This pin does not have an internal pull-up or pull-down resistor.
A2 A1 A0	29 30 31	38 39 40	46 47 48	I	Address lines [2:0]. These 3 address lines select the internal registers in UART channel during a data bus transaction. In the VLIO bus mode (details on next page): ■ A2 becomes ENIR# ■ A1 becomes ENRS485# in the QFN-32 package ■ A1 is an unused input on the TQFP-48 and QFN-40 packages and should be connected to GND ■ A0 becomes LLA#
D7 D6 D5 D4 D3 D2 D1 D0	8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2	9 8 7 6 5 4 3 2	I/O	Data bus lines [7:0] (bidirectional). In the VLIO bus mode, D7:D0 becomes AD7:AD0.
IOR#	13	16	10	I	When 16/68# pin is at logic 1, the Intel bus interface is selected and this input becomes read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When 16/68# pin is at logic 0, the Motorola bus interface is selected and this input should be connected to VCC.
IOW# (R/W#)	14	17	11	I	When 16/68# pin is at logic 1, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is at logic 0, the Motorola bus interface is selected and this input becomes read (logic 1) and write (logic 0) signal.
CS#	15	18	12	I	This input is chip select (active low) to enable the device.

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Pin Description

NAME	QFN-32 PIN#	QFN-40 PIN#	TQFP-48 PIN#	TYPE	DESCRIPTION
INT (IRQ#)	10	12	15	O (OD)	When 16/68# pin is at logic 1 for Intel bus interface, this output become the active high device interrupt output. The output state is defined by the user through the software setting of MCR[3]. INT is set to the active mode when MCR[3] is set to a logic 1. INT is set to the three state mode when MCR[3] is set to a logic 0. See MCR[3]. When 16/68# pin is at logic 0 for Motorola bus interface, this output becomes the active low device interrupt output (open drain). An external pull-up resistor is required for proper operation.
RESET (RESET#)	9	10	13	I	When 16/68# pin is at logic 1 for Intel bus interface, this input becomes RESET (active high). When 16/68# pin is at logic 0 for Motorola bus interface, this input becomes RESET# (active low). A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs of the UART. The UART transmitter output will be held at logic 1, the receiver input will be ignored and outputs are reset during reset period (see UART Reset Conditions).
DATA BUS INTERFACE - VLIO					
VLIO_EN	28	37	45	I	VLIO Bus Enable. When VLIO_EN pin is at logic 0, the bus interface is selected by the 16/68# pin. When VLIO_EN pin is at logic 1, the VLIO bus interface is enabled and the 16/68# pin has no effect.
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2	9 8 7 6 5 4 3 2	I/O	Multiplexed Address/Data lines [7:0]. The register address is latched on the rising edge of the LLA#. After the LLA# signal goes high, the UART enters the data phase where the data is placed on these lines.
IOR#	13	16	10	I	Read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the latched address. The UART places the data byte on the data bus to allow the host processor to read it on the rising edge.
IOW#	14	17	11	I	Write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the latched address.
CS#	15	18	12	I	Chip select (active low). The falling edge starts the access to the UART. A read or write is determined by the IOR# and IOW# signals.
LLA#	31	40	48	I	Latch Lower Address (active low). The register address is latched on the rising edge of the LLA# signal. After the LLA# goes high, the device enters the data phase where the data is placed on the AD[7:0] lines. In the Intel/Motorola mode, this pin becomes A0.

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Pin Description

NAME	QFN-32 PIN#	QFN-40 PIN#	TQFP-48 PIN#	TYPE	DESCRIPTION
INT	10	12	15	O	Interrupt output (active high). The output state is defined by the user through the software setting of MCR[3]. INT is set to the active mode when MCR[3] is set to a logic 1. INT is set to the three state mode when MCR[3] is set to a logic 0. See MCR[3].
MODEM I/O and GPIOs					
TX	17	32	40	O	UART Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be a logic 1 during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is a logic 0. If it is not used, leave it unconnected.
RX	18	33	41	I	UART Receive Data or infrared receive data. Normal receive data input must idle at logic 1 condition. The infrared receiver idles at logic 0. This input should be connected to VCC when not used.
RTS#	19	31	39	O	UART Request-to-Send (active low) or general purpose output. This output must be asserted prior to using Auto RTS HW flow control, see EFR[6], MCR[1] and IER[6]. This output can also be used for the Auto RS-485 half-duplex output control.
CTS#	16	30	38	I	UART Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], MSR[4] and IER[7]. This input should be connected to VCC when not used.
DTR#/GPIO0	24	29	37	I/O	General purpose I/O or UART Data-Terminal-Ready (active low).
DSR#/GPIO1	23	28	36	I/O	General purpose I/O or UART Data-Set-Ready (active low).
CD#/GPIO2	22	27	35	I/O	General purpose I/O or UART Carrier-Detect (active low).
RI#/GPIO3	21	26	34	I/O	General purpose I/O or UART Ring-Indicator (active low).
GPIO4	-	23	28	I/O	General purpose I/Os. These GPIOs are only available on the QFN-40 and TQFP-48 packages.
GPIO5	-	22	27	I/O	
GPIO6	-	21	26	I/O	
GPIO7	-	20	25	I/O	
GPIO8	-	-	19	I/O	General purpose I/Os. These GPIOs are only available on the TQFP-48 package.
GPIO9	-	-	20	I/O	
GPIO10	-	-	21	I/O	
GPIO11	-	-	22	I/O	
GPIO12	-	-	23	I/O	
GPIO13	-	-	29	I/O	
GPIO14	-	-	30	I/O	
GPIO15	-	-	31	I/O	
ANCILLARY SIGNALS					
XTAL1	26	35	43	I	Crystal or external clock input. Note: This input is not 5V tolerant.
XTAL2	27	36	44	O	Crystal or buffered clock output.

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Pin Description

NAME	QFN-32 PIN#	QFN-40 PIN#	TQFP-48 PIN#	TYPE	DESCRIPTION
EN485#	30	13	16	I	Enable Auto RS-485 Half-Duplex Mode. This pin is sampled upon power-up. If this pin is HIGH, then the RTS# output can be used for Auto RTS Hardware Flow Control or as a general purpose output. If this pin is LOW, then the RTS# output is the Auto RS-485 Half-Duplex direction control pin. In the QFN-32 package, this pin is the A1 pin when in the Intel/ Motorola mode.
ENIR#	29	38	46	I	Enable IR Mode. This pin is sampled upon power-up. If this pin is HIGH, then the TX output and RX input will behave as the UART transmit data output and UART receive data input. If this pin is LOW, then the TX output and RX input will behave as the infrared encoder data output and the infrared receive data input. In the Intel/Motorola mode, this pin is the A2 pin for all packages.
SLEEP/ PWRDN# (16/68#)	32	11	14	I/O	Sleep / Power Down pin. This pin powers up as the SLEEP input. The SLEEP input can force the UART to enter into the sleep mode after the next byte transmitted or received without meeting any of the sleep mode conditions. **See "Section 1.20.2, Sleep Mode - SLEEP pin" on page 25.** This pin can also be configured as an output pin which can be used to indicate to the CPU that the UART has entered the sleep mode. This output can also be used to power down other devices. In the QFN-32 package, this pin is the 16/68# input pin when the VLIO mode is disabled.
VCC_CORE	25	34	42	Pwr	1.62V to 3.63V VCC for the core. This supply voltage is used for the core logic including the crystal oscillator circuit.
VCC_BUS	12	15	18	Pwr	1.62V to 3.63V VCC for bus interface signals. This supply voltage pin will determine the I/O levels of the CPU bus interface signals.
VCC_UART	20	24	32	Pwr	1.62V to 3.63V VCC for the UART signals. This supply voltage pin will determine the I/O levels of the UART I/O signals including GPIO[3:0].
VCC_GPIO	-	19	24	Pwr	1.62V to 3.63V VCC for the GPIO signals. This supply voltage pin will determine the I/O levels of the GPIO[15:4] signals.
GND	11	14, 25	17, 33	Pwr	Power supply common, ground.
GND	Center Pad	Center Pad	Center Pad	Pwr	The center pad on the backside of the QFN package is metallic and should be connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

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1.0 FUNCTIONAL DESCRIPTIONS

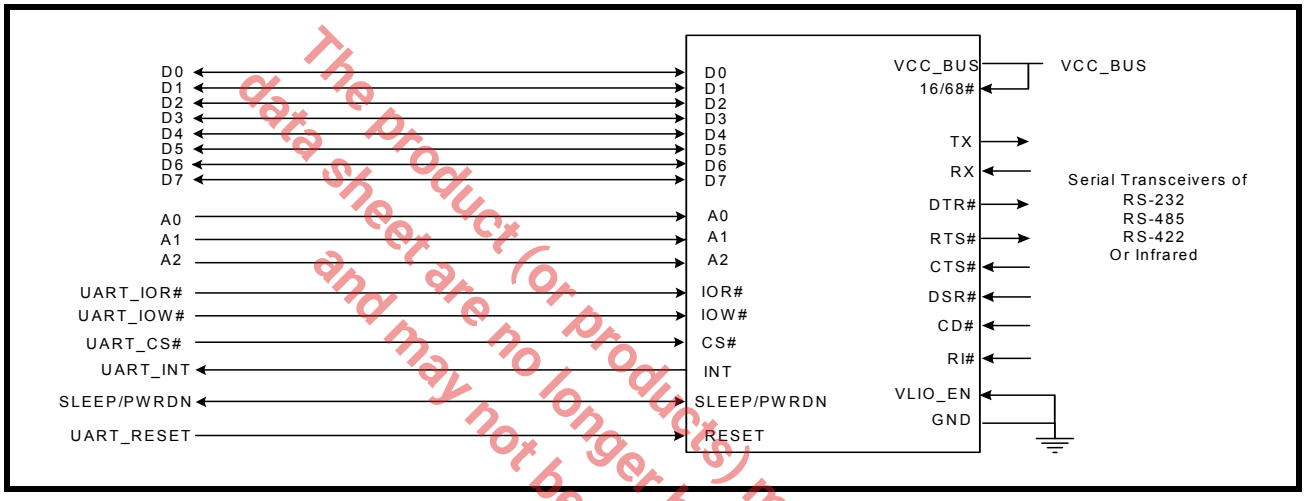
1.1 CPU Interface

There are 3 CPU interfaces that can be selected on the XR16M890. They are the Intel, Motorola and VLIO bus interfaces. Note: no clock (crystal or external clock) is required for data bus transactions. Each bus cycle is asynchronous.

1.1.1 Intel bus interface (16 mode)

The Intel bus interface consists of 8 data bits, 3 address lines and 3 control signals (CS#, IOR# and IOW#) for data bus read/write transactions. In this mode, the interrupt output (INT) is active high. A typical data bus interconnection is shown in Figure 4.

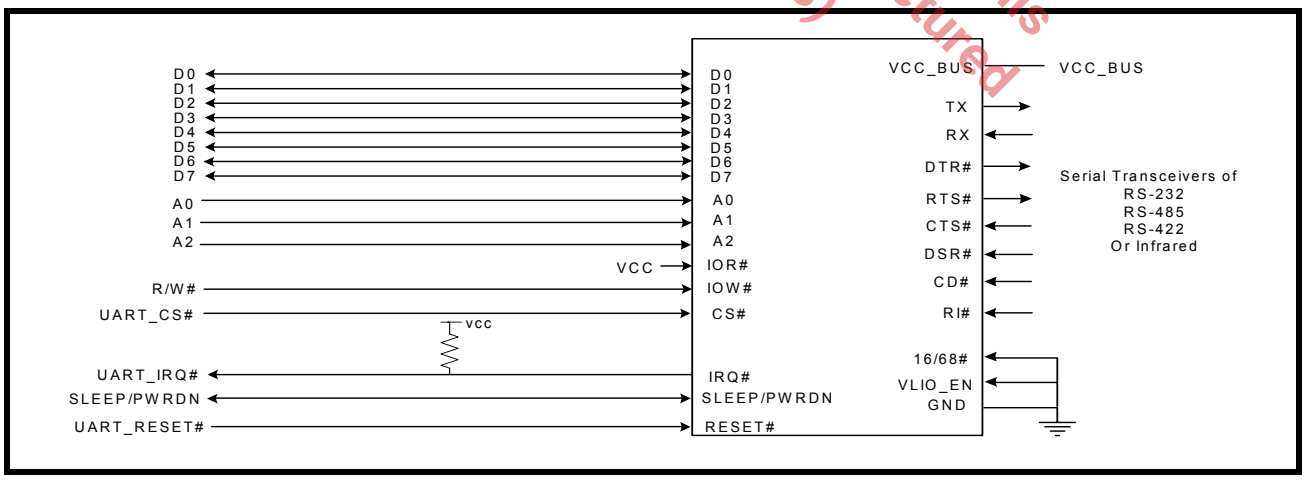
FIGURE 4. XR16M890 TYPICAL INTEL DATA BUS INTERCONNECTION



1.1.2 Motorola bus interface (68 mode)

The Motorola bus interface is similar to the Intel bus interface. This interface consists of 8 data bits, 3 address lines, but only 2 control signals (CS# and R/W#) for data bus read/write transactions. In this mode, the interrupt output (IRQ#) is an open-drain and active low. A typical data bus interconnection is shown in Figure 5.

FIGURE 5. XR16M890 TYPICAL MOTOROLA DATA BUS INTERCONNECTIONS



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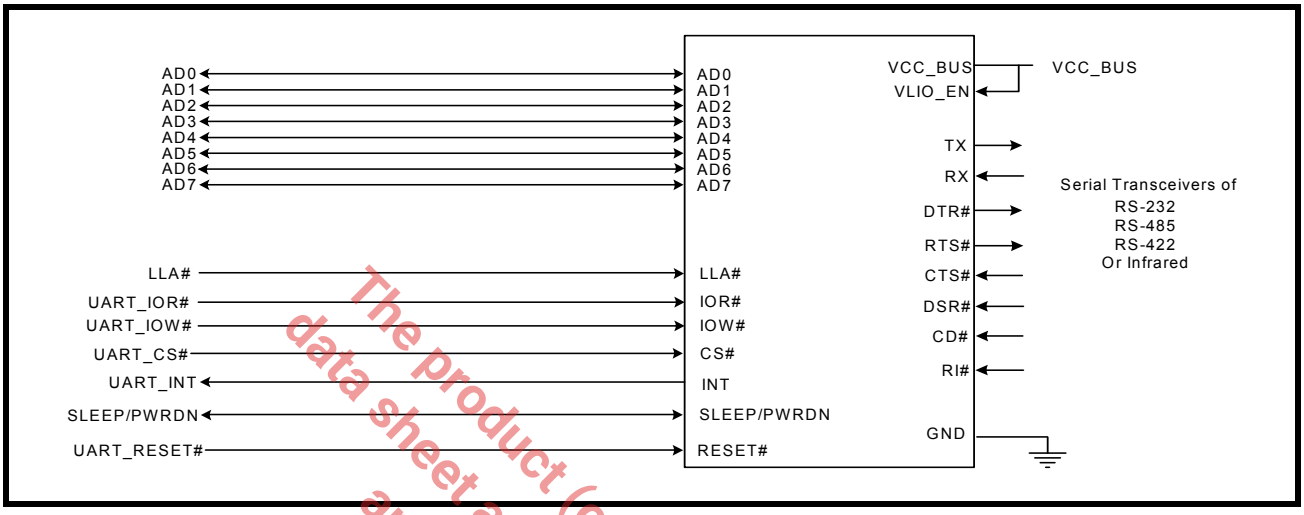
1.1.3 VLIO bus interface

The VLIO bus interface is similar to the Intel bus interface. The only difference is that the address and data lines are shared. A typical data bus interconnection is shown below in Figure 6.

FIGURE 6. XR16M890 TYPICAL VLIO DATA BUS INTERCONNECTIONS

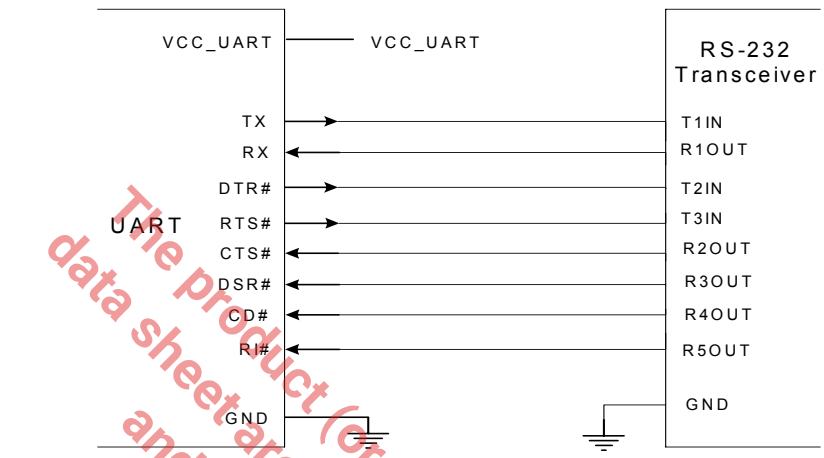


The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

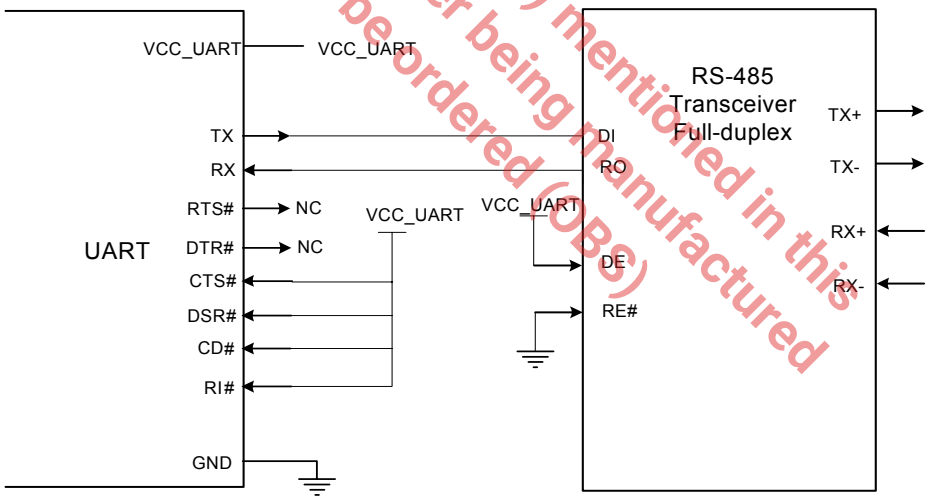
1.2 Serial Interface

The M890 is typically used with RS-232, RS-485 and IR transceivers. The following figure shows typical connections from the UART to the different transceivers. For more information on RS-232 and RS-485/422 transceivers, go to www.exar.com or send an e-mail to uarttechsupport@exar.com.

FIGURE 7. XR16M890 TYPICAL SERIAL INTERFACE CONNECTIONS



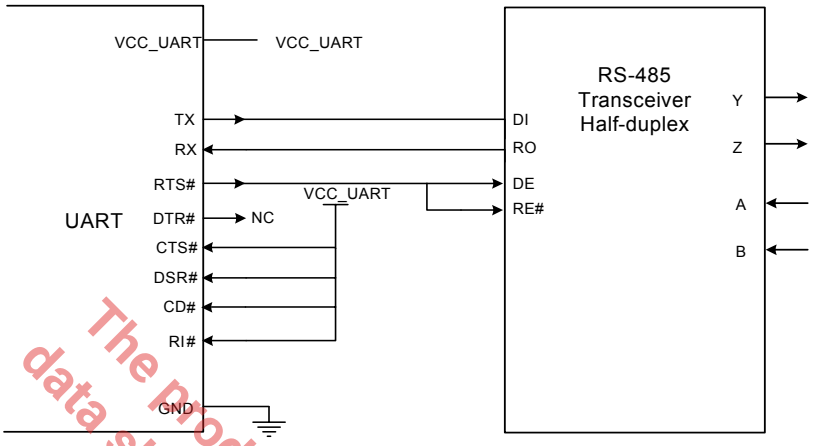
RS-232 Full-Modem Serial Interface



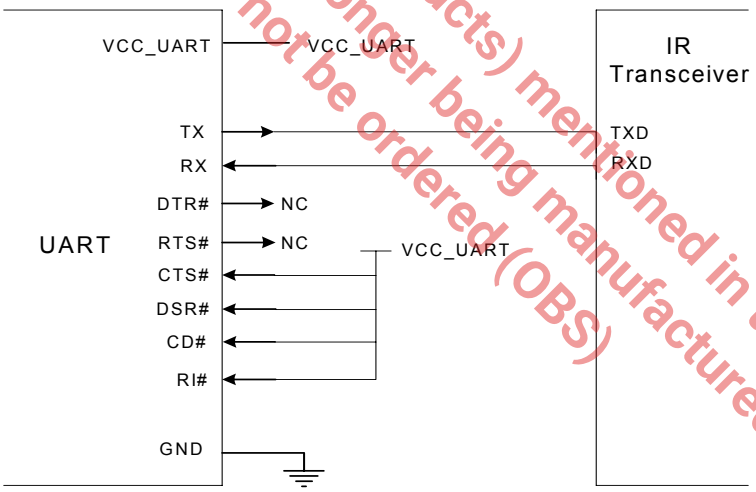
RS-485 Full-Duplex Serial Interface

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 8. XR16M890 TYPICAL SERIAL INTERFACE CONNECTIONS



RS-485 Half-Duplex Serial Interface



Infrared Connection

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

1.3 Device Reset

The RESET (RESET#) input resets the internal registers and the serial interface outputs to their default state (see Table 19). An active high (RESET) or active low (RESET#) pulse of longer than 40 ns duration will be required to activate the reset function in the device. Following a power-on reset or an external reset, the M890 is software compatible with previous generation of UARTs.

1.4 5-Volt Tolerant Inputs

The M890 can accept and withstand 5V signals on the inputs without any damage. But note that if the supply voltage for the M890 is at the lower end of the supply voltage range (ie. 1.8V), its V_{OH} may not be high enough to meet the requirements of the V_{IH} of a CPU or a serial transceiver that is operating at 5V. Caution: XTAL1 is not 5 volt tolerant.

1.5 Internal Registers

The M890 has a set of 16550 compatible registers for controlling, monitoring and data loading and unloading. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM/DLD), and a user accessible scratchpad register (SPR).

Beyond the general 16C550 features and capabilities, the M890 offers enhanced feature registers (EFR, Xon1/Xoff 1, Xon2/Xoff 2, DLD, FCTR, EMSR, FC and TRIG, SFR, SHR, GPIOINT, GPIO3T, GPIOINV, GPIOSEL) that provide automatic RTS and CTS hardware flow control, automatic Xon/Xoff software flow control, 9-bit (Multidrop) mode, auto RS-485 half duplex control, different baud rate for TX and RX and fractional baud rate generator. All the register functions are discussed in full detail later in "Section 2.0, UART Internal Registers" on page 27.

1.6 INT Ouput

The interrupt outputs change according to the operating mode and enhanced features setup. Table 1 and 2 summarize the operating behavior for the transmitter and receiver. Also see Figure 26 through 29.

The product (or products) mentioned in this data sheet is no longer being manufactured and may not be ordered (OBS)

TABLE 1: INTERRUPT PIN OPERATION FOR TRANSMITTER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (Intel or VLIO Mode)	LOW = One byte in THR HIGH = THR empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty
IRQ# Pin (Motorola Mode)	HIGH = One byte in THR LOW = THR empty	HIGH = FIFO above trigger level LOW = FIFO below trigger level or FIFO empty

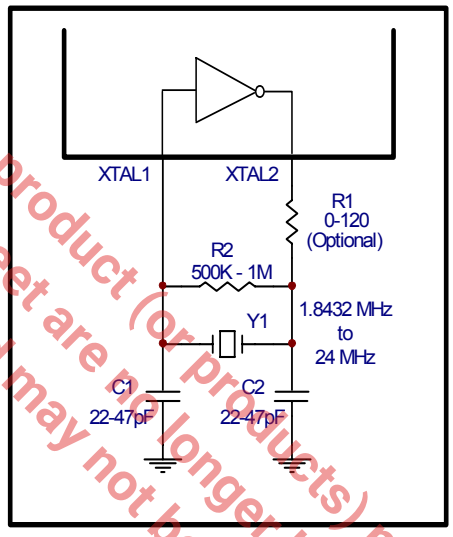
TABLE 2: INTERRUPT PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (Intel or VLIO Mode)	HIGH = One byte in RHR LOW = RHR empty	LOW = FIFO below trigger level HIGH = FIFO above trigger level or RX Data Timeout
IRQ# Pin (Motorola Mode)	HIGH = One byte in THR LOW = RHR empty	HIGH = FIFO above trigger level LOW = FIFO above trigger level or RX Data Timeout

1.7 Crystal Oscillator or External Clock Input

The M890 includes an on-chip oscillator to produce a clock for the baud rate generators in the device when a crystal is connected between XTAL1 and XTAL2 as show below. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRGs) in the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see **"Section 1.8, Programmable Baud Rate Generator with Fractional Divisor" on page 15**.

FIGURE 9. TYPICAL CRYSTAL CONNECTIONS



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The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins. Typical oscillator connections are shown in **Figure 9**. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. For further reading on oscillator circuit, see application note DAN108 on EXAR's web site.

1.8 Programmable Baud Rate Generator with Fractional Divisor

The M890 has independent Baud Rate Generators (BRGs) with prescalers for the transmitter and receiver. The prescalers are controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescalers to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X or 8X or 4X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling.

The BRG divisor (DLL, DLM, and DLD registers) defaults to the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) during power-on reset. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the divisor. The four lower bits of the DLD are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). The divisor values can be calculated with the following equations:

Divisor = (XTAL1 clock frequency / prescaler) / (serial data rate * 16), with 16X mode, **DLD[5:4] = '00'**
Divisor = (XTAL1 clock frequency / prescaler / (serial data rate * 8), with 8X mode, **DLD[5:4] = '01'**
Divisor = (XTAL1 clock frequency / prescaler / (serial data rate * 4), with 4X mode, **DLD[5:4] = '10'**

The BRG divisors can be calculated using the following formulas:

Integer Divisor = TRUNC (Divisor)
Fractional Divisor = Divisor - Integer Divisor

DLM = Integer Divisor / 256
DLL = Integer Divisor & 256
DLD = TRUNC(Fractional Divisor * 16)

In the formulas above, please note that TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

1.8.1 Fractional BRG Example

For example, if the crystal clock is 24MHz, prescaler is 1, and the sampling mode is 16X, the divisor for a baud rate of 38400bps would be:

Divisor = (24000000 / 1) / (38400 * 16) = 39.0625

Integer Divisor = TRUNC (39.0625) = 39

Fractional Divisor = 39.0625 - 39 = 0.0625

DLM = 39 / 256 = 0 = 0x00

DLL = 39 & 256 = 39 = 0x27

DLD = 0.0625 * 16 = 1 = 0x1

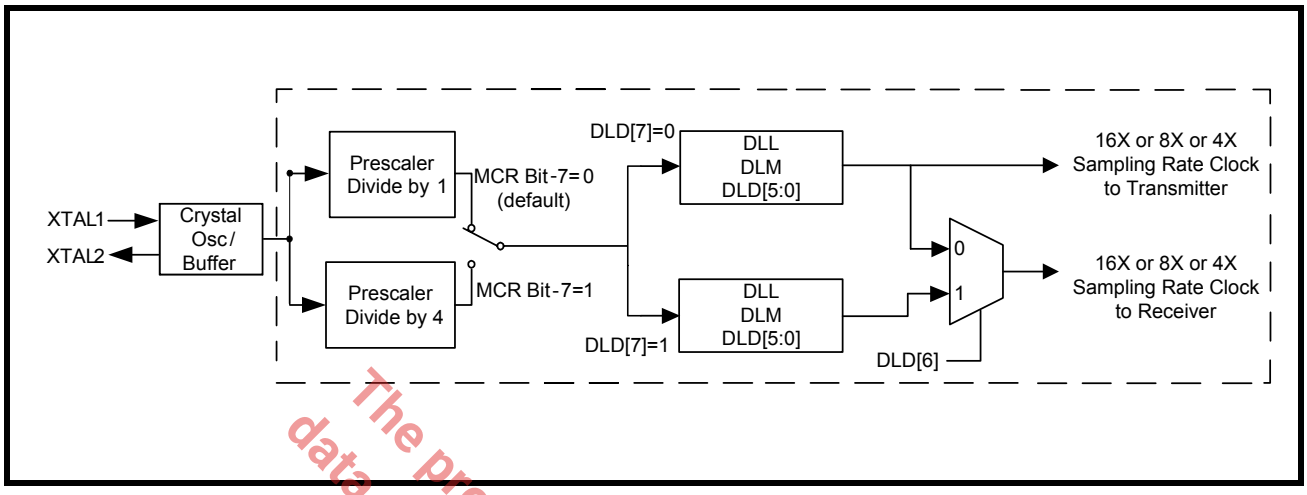
Table 3 shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in Table 3. At 8X sampling rate, these data rates would double. And at 4X sampling rate, they would quadruple. Also, when using 8X sampling mode, please note that the bit-time will have a jitter (+/- 1/16) whenever the DLD is non-zero and is an odd number.

1.8.2 Independent TX/RX BRG

The XR16M890 has two independent sets of TX and RX baud rate generator. See Figure 10. TX and RX can use different baud rates by setting DLD, DLL and DLM register. For example, TX can transmit data to the remote UART at 9600 bps while RX receives data from remote UART at 921.6 Kbps. For the baud rate setting, See "Section 3.15, Baud Rate Generator Registers (DLL, DLM and DLD) - Read/Write" on page 45.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 10. BAUD RATE GENERATOR



The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 3: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	Divisor for 16x Clock (Decimal)	DLM Program Value (HEX)	DLL Program Value (HEX)	DLD Program Value (HEX)	Data Error Rate (%)
400	3750	E	A6	0	0
2400	625	2	71	0	0
4800	312.5	1	38	8	0
9600	156.25	0	9C	4	0
10000	150	0	96	0	0
19200	78.125	0	4E	2	0
25000	60	0	3C	0	0
28800	52.0833	0	34	1	0.04
38400	39.0625	0	27	1	0
50000	30	0	1E	0	0
57600	26.0417	0	1A	0	0.08
75000	20	0	14	0	0
100000	15	0	F	0	0
115200	13.0208	0	D	0	0.16
153600	9.7656	0	9	C	0.16
200000	7.5	0	7	8	0
225000	6.6667	0	6	A	0.31
230400	6.5104	0	6	8	0.16
250000	6	0	6	0	0
300000	5	0	5	0	0
400000	3.75	0	3	C	0
460800	3.2552	0	3	4	0.16
500000	3	0	3	0	0
750000	2	0	2	0	0
921600	1.6276	0	1	A	0.16
1000000	1.5	0	1	8	0

1.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 128 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X/4X internal clock. A bit time is 16/8/4 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

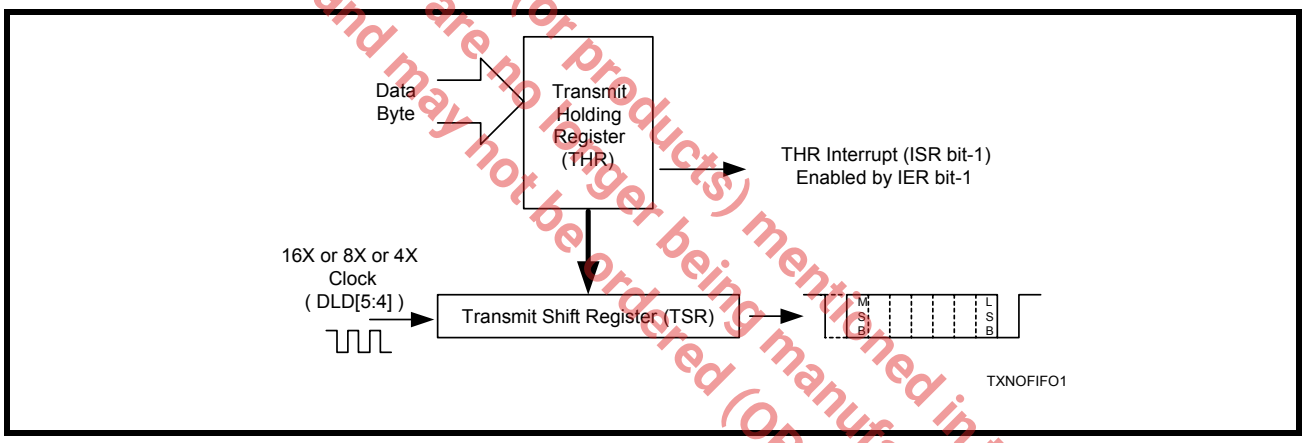
1.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 128 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

1.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 11. TRANSMITTER OPERATION IN NON-FIFO MODE



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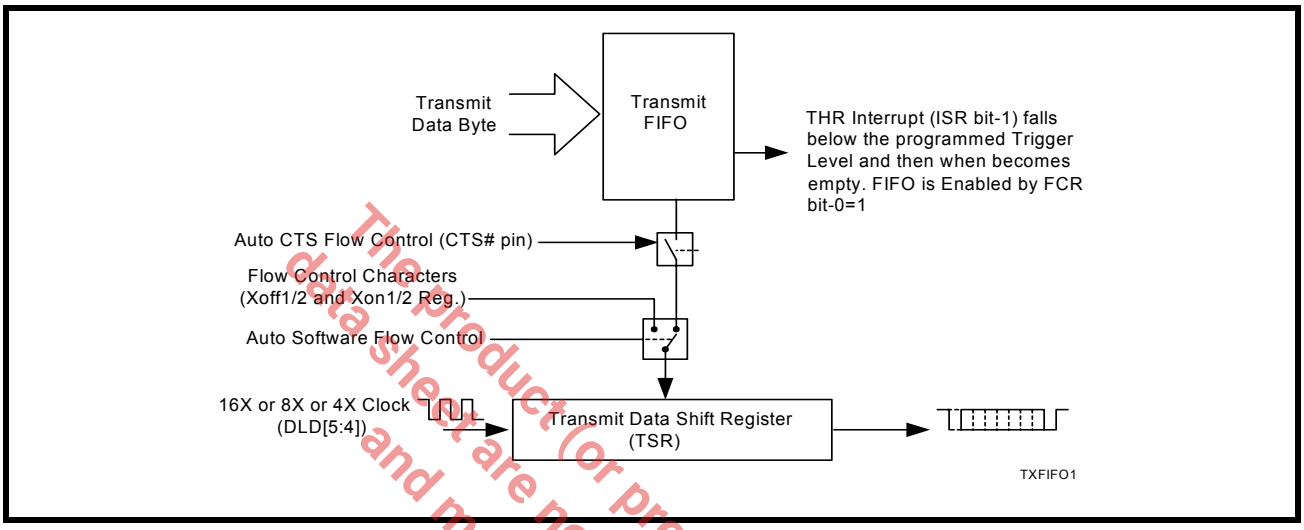
1.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 128 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the FIFO becomes empty. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 12. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (Obs).

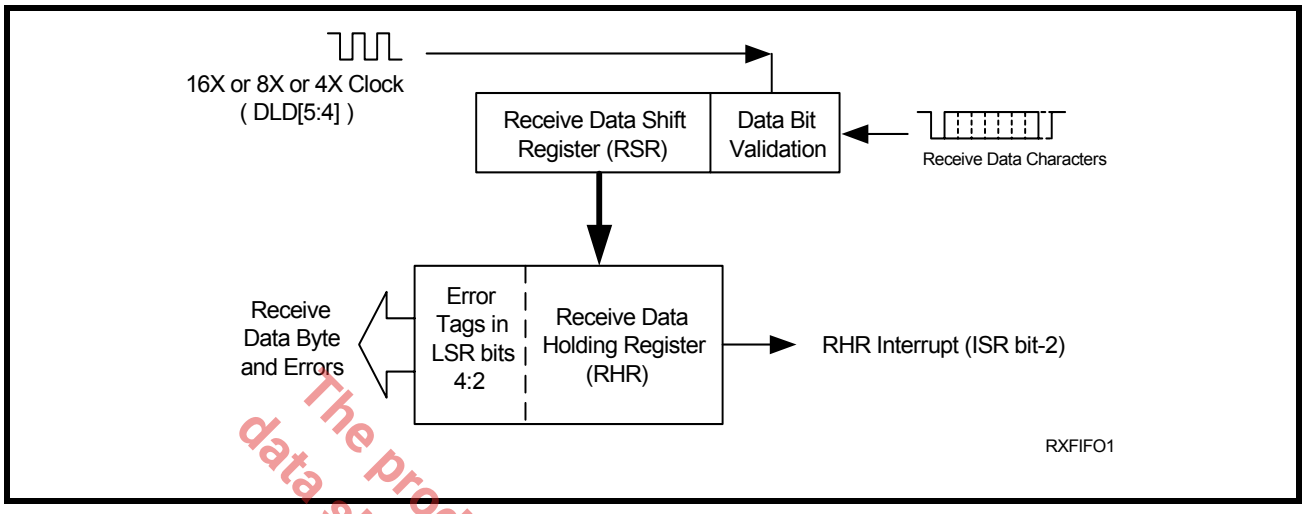
1.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 128 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X/4X clock (DLD[5:4]) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X/4X clock rate. After 8 clocks (or 4 if 8X or 2 if 4X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0. See Figure 13 and Figure 14 below.

1.10.1 Receive Holding Register (RHR) - Read-Only

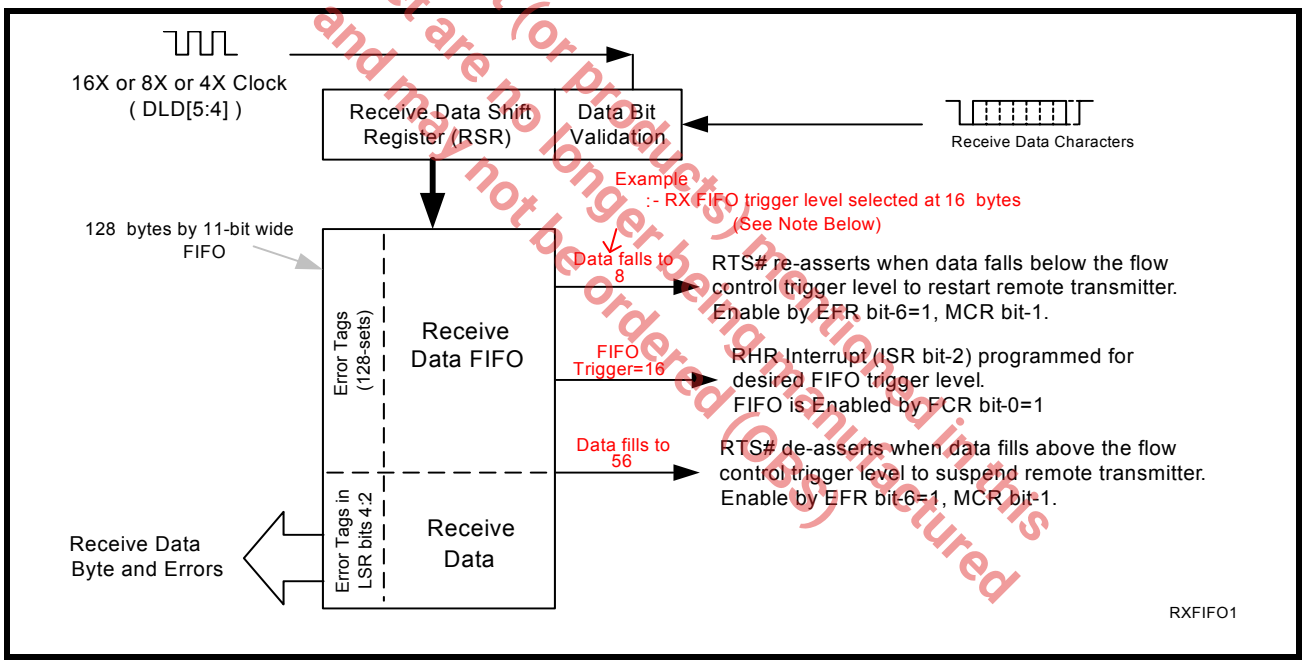
The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 128 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 13. RECEIVER OPERATION IN NON-FIFO MODE



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 14. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



1.11 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 15):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

1.12 Auto RTS Hysteresis

With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the selected RX trigger level. The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches one trigger level above the selected trigger level in the trigger table (Table 10). The RTS# pin will return LOW after the RX FIFO is unloaded to one level below the selected trigger level. Under the above described conditions, the M890 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On). Table 4 below explains this when the Trigger Table-C (Table 10) is selected.

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TABLE 4: AUTO RTS (HARDWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	RTS# DE-ASSERTED (HIGH) (CHARACTERS IN RX FIFO)	RTS# ASSERTED (LOW) (CHARACTERS IN RX FIFO)
8	8	16	0
16	16	56	8
56	56	60	16
60	60	60	56

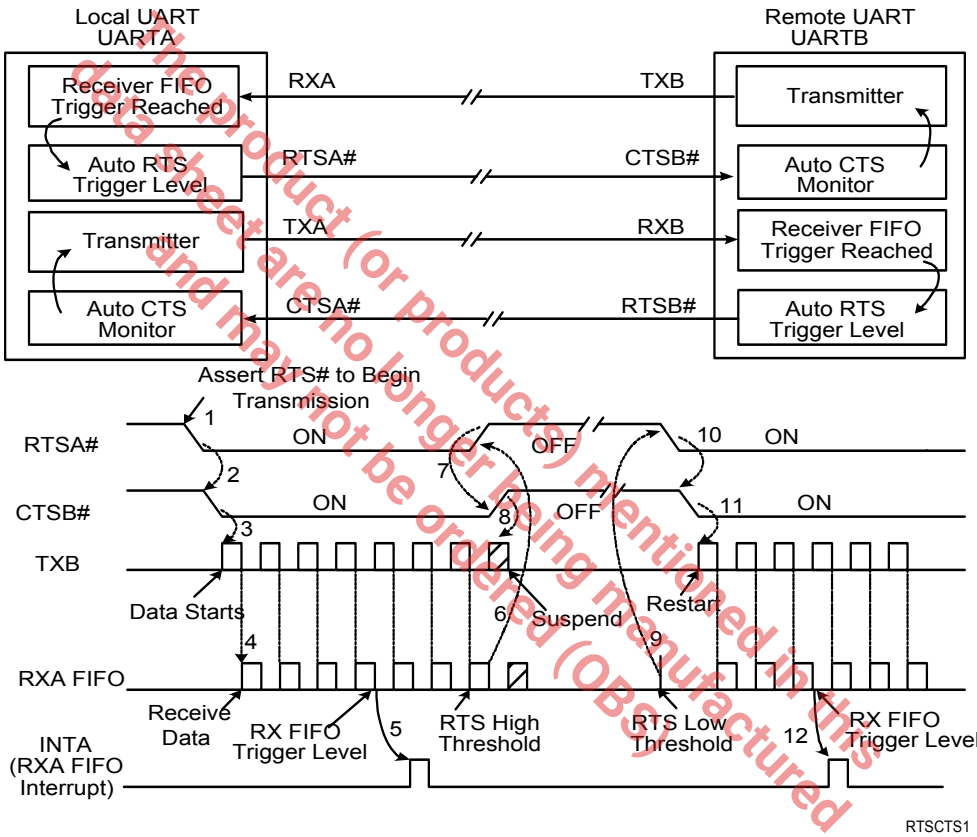
1.13 Auto CTS Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see Figure 15):

- Enable auto CTS flow control using EFR bit-7.

If needed, the CTS interrupt can be enabled through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 15. AUTO RTS AND CTS FLOW CONTROL OPERATION



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The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

1.14 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 18), the M890 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the M890 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the M890 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the M890 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 18) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the M890 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed in the RX FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the M890 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The M890 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the M890 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level. Table 5 below explains this when the Trigger Table-C (Table 10) is selected.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 5: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
56	56	56*	16
60	60	60*	56

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2* characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.

1.15 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The M890 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

1.16 Auto RS485 Half-Duplex Control Operation

The auto RS485 half-duplex direction control feature can be enabled by FCTR bit [3]. The RTS# pin becomes the half-duplex control output when this feature has been enabled. The RTS# pin is typically connected to both the Driver Enable (DE) and Receiver Enable (RE) of an RS-485 transceiver. When the Transmitter is idle, the RTS# pin is de-asserted so that the RS-485 driver is disabled and the RS-485 receiver is enabled. When data is loaded into the TX FIFO, the RTS# pin is asserted to enable the RS-485 driver and disable the RS-485 receiver. This changes the transmitter empty interrupt to TSR empty instead of THR empty.

1.16.1 RS-485 Setup Time

By default, the RTS# pin is asserted immediately before there is data on the TX output pin. For faster baud rates, it may be possible that data is lost due to a long start-up time for an RS-485 transceiver. The M890 can delay the data from 0-15 bit times to allow the RS-485 transceiver to start up (**See "Section , SHR[7:4]: RS-485 Setup Delay" on page 40.**).

1.16.2 RS-485 Turn-Around Delay

At the end of sending data, the RTS# pin is de-asserted immediately after the TX pin goes idle. The RTS# pin can be programmed to delay the RTS# from being asserted from 0-15 bit times (**See "Section , SHR[3:0]: RS-485 Turn-Around Delay / Auto RTS Hysteresis" on page 40.**). The delay optimizes the time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver.

1.17 Normal Multidrop (9-bit) Mode - Receiver

Normal multidrop mode is enabled when SFR[6] = 1 (requires EFR[4] = 1) and EFR[5] = 0 (Special Character Detect disabled). The receiver is set to Force Parity 0 (LCR[5:3] = '111') in order to detect address bytes.

With the receiver initially disabled, it ignores all the data bytes (parity bit = 0) until an address byte is received (parity bit = 1). This address byte will cause the UART to set the parity error. The UART will generate an LSR interrupt and place the address byte in the RX FIFO. The software then examines the byte and enables the receiver if the address matches its slave address, otherwise, it does not enable the receiver.

If the receiver has been enabled, the receiver will receive the subsequent data. If an address byte is received, it will generate an LSR interrupt. The software again examines the byte and if the address matches its slave address, it does not have to do anything. If the address does not match its slave address, then the receiver should be disabled.

1.17.1 Auto Address Detection - Receiver

Auto address detection mode is enabled when SFR[6] = 1 (requires EFR[4] = 1) and EFR bit-5 = 1. The desired slave address will need to be written into the XOFF2 register. The receiver will try to detect an address byte that matches the porgrammed character in the XOFF2 register. If the received byte is a data byte or an address byte that does not match the programmed character in the XOFF2 register, the receiver will discard these data. Upon receiving an address byte that matches the XOFF2 character, the receiver will be automatically enabled if not already enabled, and the address character is pushed into the RX FIFO along with the parity bit (in place of the parity error bit). The receiver also generates an LSR interrupt. The receiver will then receive the subsequent data. If another address byte is received and this address does not match the programmed XOFF2 character, then the receiver will automatically be disabled and the address byte is ignored. If the address byte matches XOFF2, the receiver will put this byte in the RX FIFO along with the parity bit in the parity error bit.

1.18 Multidrop (9-bit) Mode - Transmitter

This feature simplifies sending an address byte (9th bit = 1) and improves the efficiency of the transmit data routine for transmitting 9-bit data. In previous generation UARTs, the only way to send an address byte is by changing the parity to Forced 1 parity, load the address byte in the THR, wait for the byte to be transmitted, change the parity back to Forced 0 parity, then load data into the TX FIFO. In the XR16M890, there's no waiting required and no changing parity. The transmit routine can set SFR[7]=1, then write the address byte into the TX FIFO followed immediately by the data bytes. SFR[7] is self-clearing, therefore, if multiple address bytes need to be transmitted, then SFR[7] will need to be set prior to each address byte written into the TX FIFO. During initialization, the parity must be set to Force Parity 0 (LCR[5:3] = '111').

The product (or product(s) mentioned in this data sheet) are no longer being manufactured and may not be ordered. (OBS)

1.19 Infrared Mode

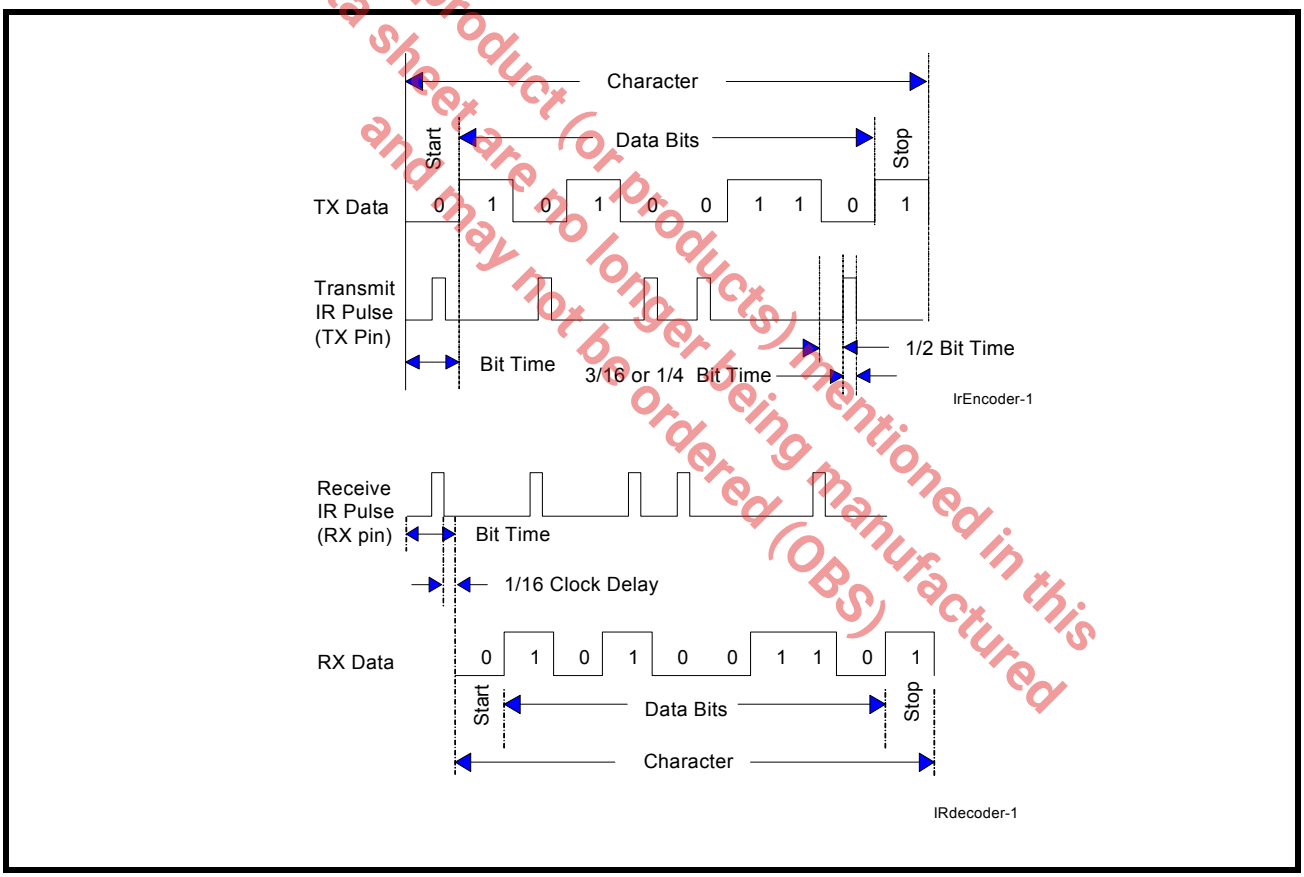
The M890 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0 and 1.1. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream with a data rate up to 115.2 Kbps. For the IrDA 1.1 standard, the infrared encoder sends out a 1/4 of a bit time wide HIGH-pulse for each "0" bit in the transmit data stream with a data rate up to 1.152 Mbps. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 16** below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. With this bit enabled, the infrared encoder and decoder is compatible to the IrDA 1.0 standard. For the infrared encoder and decoder to be compatible to the IrDA 1.1 standard, SFR bit-3 will also need to be set to a ’1’ when EFR bit-4 is set to ’1’. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see **Figure 16**.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 16. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



1.20 Sleep Mode with Auto Wake-Up

The M890 supports low voltage system designs, hence, a sleep mode with auto wake-up feature is included to reduce its power consumption when the chip is not actively used.

1.20.1 Sleep mode - IER bit-4

All of these conditions must be satisfied for the M890 to enter sleep mode:

- no interrupts pending (ISR bit-0 = 1)
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pin is idling HIGH in normal mode or LOW in infrared mode
- divisor is non-zero
- TX and RX FIFOs are empty

The M890 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The M890 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the M890 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the M890 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The M890 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX pin is idling HIGH or “marking” condition during sleep mode. This may not occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on each of the RX input.

1.20.2 Sleep Mode - SLEEP pin

The M890 has a new pin called the SLEEP pin that can be used instead of setting IER bit-4=1. The M890 will enter the sleep mode when:

- the current byte in the TSR has completely shifted out
- the current byte in the RSR has been completely received

Under this condition, there could be data in the TX and RX FIFOs. Any data that is the TX and RX FIFOs when the SLEEP pin is asserted will not be affected. The only data that will be lost is any data that is still being received on the RX pin. The M890 will only wake up after the SLEEP pin has been de-asserted.

1.20.3 Wake-up Interrupt

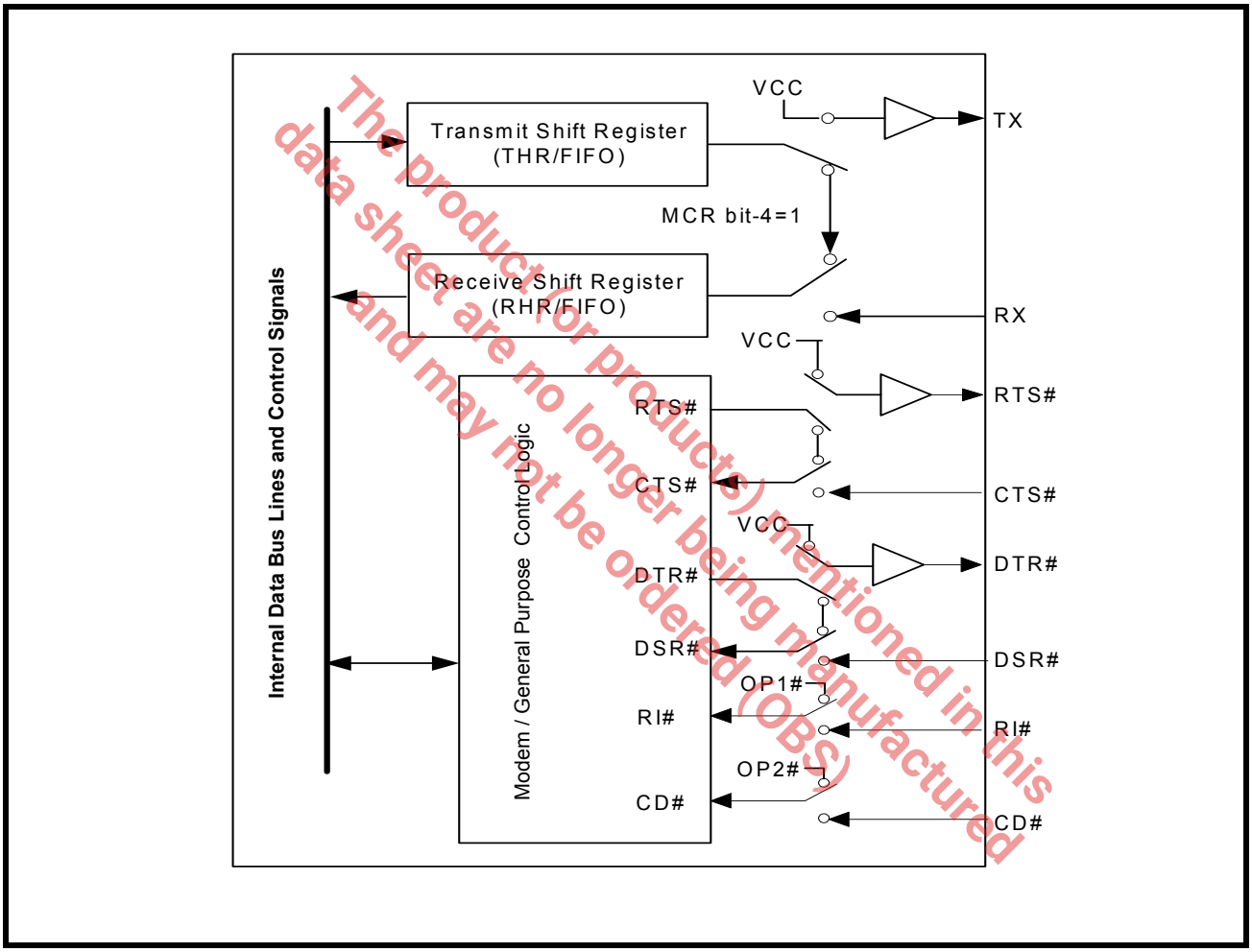
The M890 has the wake up interrupt. By setting the FCR bit-3, wake up interrupt is enabled or disabled. The default status of wake up interrupt is disabled. Please **See ”Section 3.5, FIFO Control Register (FCR) - Write-Only” on page 34.**

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

1.21 Internal Loopback

The M890 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 17 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held HIGH or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 17. INTERNAL LOOPBACK



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2.0 UART INTERNAL REGISTERS

The complete register set for the M890 is shown in Table 6 and Table 7.

TABLE 6: UART INTERNAL REGISTERS

A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	DREV - Device Revision	Read-only	LCR[7] = 1, LCR ≠ 0xBF, DLL = 0x00, DLM = 0x00
0 0 1	DVID - Device Identification Register	Read-only	
0 0 0	DLL - Divisor LSB Register	Read/Write	LCR[7] = 1, LCR ≠ 0xBF See DLD[7:6]
0 0 1	DLM - Divisor MSB Register	Read/Write	
0 1 0	DLD - Divisor Fractional Register	Read/Write	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 1	IER - Interrupt Enable Register	Read/Write	
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR[7] = 0 if EFR[4] = 1 or LCR ≠ 0xBF if EFR[4] = 0
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register	Read-only	
1 0 1	SHR - Setup/Hysteresis Register	Write-only	
1 1 0	MSR - Modem Status Register	Read-only	
1 1 0	SFR - Special Function Register	Write-only	LCR ≠ 0xBF EFR[4] = 1
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR ≠ 0xBF, FCTR[6] = 0, SFR[0] = 0
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	LCR ≠ 0xBF, FCTR[6] = 1, SFR[0] = 0
1 1 1	FC - RX/TX FIFO Level Counter Register	Read-only	
ENHANCED REGISTERS			
0 0 0	FC - RX/TX FIFO Level Counter Register	Read-only	LCR = 0xBF
0 0 0	TRIG - RX/TX FIFO Trigger Level Register	Write-only	
0 0 1	FCTR - Feature Control Register	Read/Write	
0 1 0	EFR - Enhanced Function Register	Read/Write	
1 0 0	Xon-1 - Xon Character 1	Read/Write	LCR = 0xBF SFR[0]=0
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	
1 0 0	GPIOINT - GPIO Interrupt Enable Register	Read/Write	LCR = 0xBF SFR[0]=1
1 0 1	GPIO3T - GPIO Three-State Control Register	Read/Write	
1 1 0	GPIOINV - GPIO Polarity Control Register	Read/Write	
1 1 1	GPIOSEL - GPIO Select Register	Read/Write	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 7: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS# Int. Enable	0/ RTS# Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	LCR[7] = 0
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ RTS CTS Interrupt	0/ Xoff Interrupt	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR[7] = 0 if EFR[4]=1 or LCR≠0xBF if EFR[4]=0
0 1 0	FCR	WR	RX FIFO Trigger	RX FIFO Trigger	TX FIFO Trigger	TX FIFO Trigger	Wake up Int Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Mode ENable	0/ XonAny	Internal Lopback Enable	INT Out-put Enable (OP2#)	OP1#/ GPIO Select	RTS# Output Control	DTR# Output Control	LCR≠0xBF
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
1 0 1	SHR	WR	RS-485 Setup Bit-3	RS-485 Setup Bit-2	RS-485 Setup Bit-1	RS-485 Setup Bit-0	RS-485 Delay Bit-3/ Hystere-sis Bit-3	RS-485 Delay Bit-2/ Hyster-esis Bit-2	RS-485 Delay Bit-1/ Hyster-esis Bit-1	RS-485 Delay Bit-0/ Hystere-sis Bit-0	
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 0	SFR	WR	TX 9-bit	Enable 9-bit mode	Disable RX	Disable TX	Fast IR	GPIO INT Enable	GPIO [15:8]/ [7:0] Select	GPIO Access	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR≠0xBF FCTR[6]=0 SFR[0]=0
1 1 1	GPIOLVL	RD/WR	Bit-15/ Bit-7	Bit-14/ Bit-6	Bit-13/ Bit-5	Bit-12/ Bit-4	Bit-11/ Bit-3	Bit-10/ Bit-2	Bit-9/ Bit-1	Bit-8/ Bit-0	LCR≠0xBF FCTR[6]=0 SFR[0]=1

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 7: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
1 1 1	EMSR	WR	Xoff interrupt mode select	LSR interrupt mode select	Rsvd	Modem 3-State Control	Invert RTS in RS485 mode	Send TX imme-diate	FIFO count control bit-1	FIFO count control bit-0	LCR≠0xBF FCTR[6]=1 SFR[0]=0
1 1 1	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Baud Rate Generator Divisor											
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR≠0xBF DLL= 0x00 DLM= 0x00
0 0 1	DVID	RD	0	0	0	1	0	0	0	1	
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR≠0xBF DLD[7:6]
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 1 0	DLD	RD/WR	BRG select	Enable Indepen-dent BRG	4X Mode	8X Mode	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR≠0xBF EFR[4] = 1
Enhanced Registers											
0 0 0	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
0 0 0	TRIG	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	FCTR	RD/WR	RX/TX select	Swap SPR	Trigger Table bit-1	Trigger Table bit-0	Auto RS485 Half-Duplex	invert RX IR	Rsvd	PWRDN # control	
0 1 0	EFR	RD/WR	Auto CTS# Enable	Auto RTS# Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:3], MCR[7:5], DLD, SHR, SFR	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF SFR[0]=0
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 0	GPIOINT	RD/WR	Bit-15/ Bit-7	Bit-14/ Bit-6	Bit-13/ Bit-5	Bit-12/ Bit-4	Bit-11/ Bit-3	Bit-10/ Bit-2	Bit-9/ Bit-1	Bit-8/ Bit-0	LCR=0xBF SFR[0]=1
1 0 1	GPIO3T	RD/WR	Bit-15/ Bit-7	Bit-14/ Bit-6	Bit-13/ Bit-5	Bit-12/ Bit-4	Bit-11/ Bit-3	Bit-10/ Bit-2	Bit-9/ Bit-1	Bit-8/ Bit-0	
1 1 0	GPIOINV	RD/WR	Bit-15/ Bit-7	Bit-14/ Bit-6	Bit-13/ Bit-5	Bit-12/ Bit-4	Bit-11/ Bit-3	Bit-10/ Bit-2	Bit-9/ Bit-1	Bit-8/ Bit-0	
1 1 1	GPIOSEL	RD/WR	Bit-15/ Bit-7	Bit-14/ Bit-6	Bit-13/ Bit-5	Bit-12/ Bit-4	Bit-11/ Bit-3	Bit-10/ Bit-2	Bit-9/ Bit-1	Bit-8/ Bit-0	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

3.0 INTERNAL REGISTER DESCRIPTIONS

3.1 Receive Holding Register (RHR) - Read- Only

SEE"RECEIVER" ON PAGE 18.

3.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 17.

3.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

3.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

3.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16M890 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when an overrun occurs. LSR bits 2-4 generate an interrupt when the character in the RHR has an error. However, when EMSR bit-6 changes to 1 (default is 0), LSR bit 2-4 generate an interrupt when the character is received in the RX FIFO. Please refer to **"Section 3.14, Enhanced Mode Select Register (EMSR) - Write-only" on page 44**.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR[4] = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR[4]=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt. (default)
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS# Output Interrupt Enable (requires EFR[4]=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from LOW to HIGH (if enabled by EFR bit-6).

IER[7]: CTS# Input Interrupt Enable (requires EFR[4]=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from LOW to HIGH (if enabled by EFR bit-7).

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OPS)

3.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 8, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

3.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xon/Xoff/Special character is by detection of a Xon, Xoff or Special character.
- CTS# is when the remote transmitter toggles the input pin (from LOW to HIGH) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS flow control.
- Wakeup interrupt is generated when the M890 wakes up from the sleep mode.
- GPIO interrupt is generated when a GPIO input has been asserted (polarity selected by GPIOINV register)

3.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xon or Xoff interrupt is cleared by a read to the ISR register.
- Special character interrupt is cleared by a read to ISR register or after next character is received.
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register.
- Wakeup interrupt is cleared by a read to ISR register.
- GPIO interrupt is cleared by a read to the GPIOLVL register

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 8: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)

TABLE 8: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
6	0	1	0	0	0	0	RXRDY (Received Xon, Xoff or Special character)
7	1	0	0	0	0	0	CTS#, RTS# change of state
-	0	0	0	0	0	1	None (default) or Wakeup interrupt

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Table 8).

ISR[4]: Interrupt Status (requires EFR bit-4 = 1)

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff, Xon or special character(s).

ISR[5]: Interrupt Status (requires EFR bit-4 = 1)

ISR bit-5 indicates that CTS# or RTS# has changed state from LOW to HIGH.

ISR[6]: GPIO Interrupt Status

This bit reports the GPIO interrupt status. When a GPIO interrupt has been generated, this bit will be the inverse of ISR[7]. When the GPIO interrupt is not enabled, this bit will match ISR[7] for 16550 compatibility (See Table 9).

ISR[7]: FIFO Enable Status

This bit is set to a logic 0 when the FIFOs are disabled. It is set to a logic 1 when the FIFOs are enabled (See Table 9).

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

TABLE 9: FIFO ENABLE STATUS/GPIO INTERRUPT STATUS

FCR[0]	FIFO MODE	GPIO INTERRUPT ENABLED (GPIOINT REGISTER)	GPIO INTERRUPT STATUS	ISR[7]	ISR[6]
0	FIFO Disabled	No	No GPIO Interrupt	0	0
0	FIFO Disabled	Yes	No GPIO Interrupt	0	0
0	FIFO Disabled	Yes	GPIO Interrupt	0	1
1	FIFO Enabled	No	No GPIO Interrupt	1	1
1	FIFO Enabled	Yes	No GPIO Interrupt	1	1
1	FIFO Enabled	Yes	GPIO Interrupt	1	0

3.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and enable the wake up interrupt. They are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: Enable wake up interrupt (requires EFR bit-4 = 1)

- Logic 0 = Disable the wake up interrupt (default).
- Logic 1 = Enable the wake up interrupt.

Please refer to **"Section 1.20.3, Wake-up Interrupt" on page 25**.

FCR[5:4]: Transmit FIFO Trigger Select (requires EFR bit-4 = 1)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. **Table 10** below shows the selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

FCR[7:6]: Receive FIFO Trigger Select

These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. **Table 10** shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

TRIGGER TABLE	FCTR BIT-5	FCTR BIT-4	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
Table-A	0	0	0 0 1 1	0 1 0 1	0	0	1 (default) 4 8 14	1 (default)	16C550, 16x255x, 16x554, 16x57x, 16x58x
Table-B	0	1	0 0 1 1	0 1 0 1	0 0 1 1	0 1 0 1	8 16 24 28	16 8 24 30	16C650A, 16L651, 16x265x, 16x564
Table-C	1	0	0 0 1 1	0 1 0 1	0 0 1 1	0 1 0 1	8 16 56 60	8 16 32 56	16x654
Table-D	1	1	X	X	X	X	Programmable via TRG register. FCTR[7] = 0.	Programmable via TRG register. FCTR[7] = 1.	16x275x, 16C285x, 16C850, 16C854, 16C864

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

3.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 11 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 11: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, HIGH
1	1	1	Forced parity to space, LOW

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space', logic 0, state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition. (default)
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM/DLD) enable.

- Logic 0 = Data registers are selected. (default)
- Logic 1 = Divisor latch registers are selected.

3.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output HIGH (default).
- Logic 1 = Force DTR# output LOW.

MCR[1]: RTS# Output

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# output HIGH (default).
- Logic 1 = Force RTS# output LOW. It is required to start Auto RTS Flow Control.

MCR[2]: GPIO[3:0] or Modem IO Select

This bit controls whether GPIO[3:0] behave as GPIO pins or as modem IO pins (RI#, CD#, DTR#, DSR#)

- Logic 0 = GPIO[3:0] behave as GPIO pins
- Logic 1 = GPIO[3:0] behave as RI#, CD#, DTR#, DSR#

In the Loopback Mode, this bit is used as the OP1# to write the state of the modem RI# interface signal.

MCR[3]: INT Output Enable

Enable or disable INT outputs to become active or in three-state. This bit is also used to control the OP2# signal during internal loopback mode. This bit applies only to the Intel and VLIO bus modes. This bit has no effect in the Motorola bus mode.

- Logic 0 = INT output disabled (three state). During internal loopback mode, OP2# is HIGH.
- Logic 1 = INT output enabled (active). During internal loopback mode, OP2# is LOW.

TABLE 12: INT OUTPUT MODES

MCR BIT-3	INT OUTPUT
0	Three-State
1	Active

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and Figure 17.

MCR[5]: Xon-Any Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Xon-Any function (for 16C550 compatibility, default).
- Logic 1 = Enable Xon-Any function. In this mode, any RX character received will resume transmit operation. The RX character will be loaded into the RX FIFO , unless the RX character is an Xon or Xoff character and the M890 is programmed to use the Xon/Xoff flow control.

MCR[6]: Infrared Encoder/Decoder Enable (requires EFR bit-4 = 1)

- Logic 0 = Enable the standard modem receive and transmit input/output interface. (Default)
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. The TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels conform to the IrDA infrared interface requirement. The RX FIFO may need to be flushed upon enable. While in this mode, the infrared TX output will be LOW during idle data conditions.

MCR[7]: Clock Prescaler Select (requires EFR bit-4 = 1)

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

3.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is enabled, LSR bit 1 will generate an interrupt immediately and LSR bits 2-4 will generate an interrupt when a character with an error is in the RHR.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

LSR[4]: Receive Break Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was LOW for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, “mark” or HIGH.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

3.9 Setup/Hysteresis Register (SHR) - Write Only

In the Auto RS-485 half-duplex mode, the RTS# control output can be asserted from 0 to 15 bit times before data is transmitted to allow for the startup time of an RS-485 transceiver that may be in shutdown mode. The RTS# control output can also be delayed from 0 to 15 bit times after the last byte has been transmitted to allow the data to propogate down long data cables.

In the Auto RTS flow control mode, this register selects the hysteresis levels that will be used with programmable trigger levels (Trigger Table-D).

SHR[3:0]: RS-485 Turn-Around Delay / Auto RTS Hysteresis

When the Auto RS-485 half-duplex mode is enabled (FCTR[3] = 1), the value programmed in these bits will be the number of bits (0-15) the RTS# pin will wait before it is de-asserted after the last byte that has been transmitted.

When Auto RTS flow control is enabled (EFR[6] = 1) and programmable trigger levels are used (FCTR[5:4] = '11'), these bits select the hysteresis levels for the RTS# flow control pin (See Table 13).

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 13: AUTO RTS HYSTERESIS

SHR BIT-3	SHR BIT-2	SHR BIT-1	SHR BIT-0	RTS# HYSTERESIS (CHARACTERS)
0	0	0	0	0
0	0	0	1	±4
0	0	1	0	±6
0	0	1	1	±8
0	1	0	0	±8
0	1	0	1	±16
0	1	1	0	±24
0	1	1	1	±32
1	0	0	0	±40
1	0	0	1	±44
1	0	1	0	±48
1	0	1	1	±52
1	1	0	0	±12
1	1	0	1	±20
1	1	1	0	±28
1	1	1	1	±36

SHR[7:4]: RS-485 Setup Delay

When the Auto RS-485 half-duplex mode is enabled (FCTR[3] = 1), the value programmed in these bits will be the number of bits (0-15) the RTS# pin is asserted before the first byte is transmitted.

3.10 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used for general purpose inputs when they are not used with modem signals. Reading the higher four bits shows the status of the modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from LOW to HIGH, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

The product (s) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS Flow Control allows starting and stopping of local data transmissions based on the modem CTS# signal. A HIGH on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a LOW will resume data transmission. Normally MSR bit-4 bit is the complement of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

Normally this bit is the complement of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

3.11 Special Function Register (SFR) - Write Only

This register provides access to some of the advanced features of XR16M890. This register can only be written to if EFR[4] = 1.

SFR[0]: Enable GPIO Registers (Requires EFR[4] = 1)

- Logic 0 = GPIO control and status registers are not enabled.
- Logic 1 = GPIOLVL register is accessible at SPR register location. GPIOINT, GPIO3T, GPIOINV, GPIOSEL registers are accessible at XON1, XON2, XOFF1, and XOFF2 register locations.

SFR[1]: GPIO[15:8] or GPIO[7:0] Select (Requires EFR[4] = 1)

- Logic 0 = GPIOLVL, GPIOINT, GPIO3T, GPIOINV and GPIOSEL registers will control and report the status of GPIO[7:0].
- Logic 1 = GPIOLVL, GPIOINT, GPIO3T, GPIOINV and GPIOSEL registers will control and report the status of GPIO[15:8].

SFR[2]: GPIO Interrupt Enable (Requires EFR[4] = 1)

- Logic 0 = GPIO interrupt is disabled.
- Logic 1 = GPIO interrupt is enabled. GPIOs that have been configured as inputs can generate GPIO interrupts if the bit is enabled in the GPIOINT register. The polarity of the GPIO interrupt is selected via the GPIOINV register.

SFR[3]: Enable/Disable fast IR mode (Requires EFR[4] = 1)

The M890 supports the new fast IR transmission with data rate up to 1.152 Mbps.

- Logic 0 = IrDA version 1.0, 3/16 pulse ratio, data rate up to 115.2 Kbps (default).
- Logic 1 = IrDA version 1.1, 1/4 pulse ratio, data rate up to 1.152 Mbps. For more IR mode information, please **See "Section 1.19, Infrared Mode" on page 24.**

SFR[4]: Enable/Disable Transmitter (Requires EFR[4] = 1)

- Logic 0 = Enable Transmitter (default).
- Logic 1 = Disable Transmitter.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

SFR[5]: Enable/Disable Receiver (Requires EFR[4] = 1)

- Logic 0 = Enable Receiver (default).
- Logic 1 = Disable Receiver.

SFR[6]: Enable/Disable 9-bit mode (Requires EFR[4] = 1)

For the 9-bit mode information, **See "Section 1.17, Normal Multidrop (9-bit) Mode - Receiver" on page 23.**

- Logic 0 = Normal 8-bit mode (default).
- Logic 1 = Enable 9-bit or Multidrop mode.

SFR[7]: TX Address Bit (Requires EFR[4] = 1)

This bit requires that forced "0" parity is enabled (LCR[5:3]='111'). If this bit is enabled, the 9th bit of the next byte written to THR will be a '1'. This bit resets after a write to THR. For the 9-bit mode information, **See "Section 1.18, Multidrop (9-bit) Mode - Transmitter" on page 23.**

- Logic 0 = Value of 9th bit will be '0' (default).
- Logic 1 = Value of 9th bit will be '1'.

3.12 Scratch Pad Register (SPR) - Read/Write

This is an 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

3.13 GPIO Level Register (GPIOLVL) - Read/Write

This register provides the current state of the GPIO pins.

If a GPIO has been configured as an input:

- A read will report the current state of the input.
- A write to any GPIO configured as an input will not have any effect.

If a GPIO has been configured as an output:

- A read will report the current value of the register. The current value of the register will also be the current state of the output pin if three-state mode is not enabled (GPIO3T register).
- A write will change the current value of the register. The current value of the register will also be the current state of the output pin if three-state mode is not enabled (GPIO3T register).

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

3.14 Enhanced Mode Select Register (EMSR) - Write-only

This register replaces SPR (during a Write) and is accessible only when FCTR[6] = 1.

EMSR[1:0]: Receive/Transmit FIFO Level Count

When Scratchpad Swap (FCTR[6]) is asserted, EMSR bits 1-0 controls what mode the FIFO Level Counter is operating in.

TABLE 14: SCRATCHPAD SWAP SELECTION

FCTR[6]	EMSR[1]	EMSR[0]	Scratchpad is
0	X	X	Scratchpad
1	X	0	RX FIFO Level Counter Mode
1	0	1	TX FIFO Level Counter Mode
1	1	1	Alternate RX/TX FIFO Counter Mode

During Alternate RX/TX FIFO Level Counter Mode, the first value read after EMSR bits 1-0 have been asserted will always be the RX FIFO Level Counter. The second value read will correspond with the TX FIFO Level Counter. The next value will be the RX FIFO Level Counter again, then the TX FIFO Level Counter and so on and so forth.

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

EMSR[2]: Send TX Immediately

- Logic 0 = Do not send TX immediately (default).
- Logic 1 = Send TX immediately. When FIFO is enabled and this bit is set, the next data will be written to the TX shift register. Thus, the data will be sent out immediately instead of queuing in the FIFO. Every time, only 1 byte will be send out. Once this byte has been sent out, the EMSR[2] will go back to 0 automatically. If more than 1 byte will be sent out, EMSR[2] needs to be set to 1 for each byte.

EMSR[3]: Invert RTS in RS485 mode

- Logic 0 = RTS# output is a logic 0 during TX(default).
- Logic 1 = RTS# output is a logic 1 during TX.

EMSR[4]: Modem Outputs Three-State Control

- Logic 0 = TX, RTS#, and DTR# outputs are active (default).
- Logic 1 = TX, RTS#, and DTR# outputs are in three-state mode.

EMSR[5]: Reserved

This bit is reserved and should be ’0’.

EMSR[6]: LSR Interrupt Mode

- Logic 0 = LSR Interrupt Delayed (default). LSR bits 2, 3, and 4 will generate an interrupt when the character with the error is in the RHR.
- Logic 1 = LSR Interrupt Immediate. LSR bits 2, 3, and 4 will generate an interrupt as soon as the character is received into the FIFO.

EMSR[7]: Xoff/Special character Interrupt Mode Select

This bit selects how the Xoff and Special character interrupt is cleared. The XON interrupt can only be cleared by reading the ISR register.

- Logic 0 = Xoff interrupt is cleared by either reading ISR register or when an XON character is received. Special character interrupt is cleared by either reading ISR register or when next character is received. (default).
- Logic 1 = Xoff/Special character interrupt can only be cleared by reading the ISR register.

3.15 Baud Rate Generator Registers (DLL, DLM and DLD) - Read/Write

These registers make-up the value of the baud rate divisor. The M890 has different DLL, DLM and DLD for transmitter and receiver. It provides more convenience for the transmitter and receiver to transmit data with different rate. The M890 uses DLD[7:6] to select TX or RX. Then it provides DLD[5:0] to select the sampling frequency and fractional baud rate divisor. The concatenation of the contents of DLM and DLL gives the 16-bit divisor value. The value is added to DLD[3:0]/16 to achieve the fractional baud rate divisor. DLD must be enabled via EFR bit-4 before it can be accessed. See Table 15 below and See "Section 1.8, Programmable Baud Rate Generator with Fractional Divisor" on page 15.

DLD[5:4]: Sampling Rate Select

These bits select the data sampling rate. By default, the data sampling rate is 16X. The maximum data rate will double if the 8X mode is selected and will quadruple if the 4X mode is selected. See Table 15 below.

TABLE 15: SAMPLING RATE SELECT

DLD[5]	DLD[4]	SAMPLING RATE
0	0	16X
0	1	8X
1	X	4X

DLD[6]: Independent BRG enable

- Logic 0 = The Transmitter and Receiver uses the same Baud Rate Generator (default).
- Logic 1 = The Transmitter and Receiver uses different Baud Rate Generators. Use DLD[7] for selecting which baud rate generator to configure.

DLD[7]: BRG select

When DLD[6] = 1, this bit selects whether the values written to DLL, DLM and DLD[5:0] will be for the Transmit Baud Rate Generator or the Receive Baud Rate Generator. When DLD[6] = 0 (same Baud Rate Generator used for both TX and RX), this bit must be a logic 0 to properly write to the appropriate DLL, DLM and DLD[5:0].

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

.

TABLE 16: BRG SELECT

DLD[7]	DLD[6]	BRG
0	0	Transmitter and Receiver uses same BRG. Writing to DLL, DLM and DLD[5:0] configures the BRG for both the TX and RX.
0	1	Transmitter and Receiver uses different BRGs. Writing to DLL, DLM and DLD[5:0] configures the BRG for TX.
1	1	Transmitter and Receiver uses different BRGs. Writing to DLL, DLM and DLD[5:0] configures the BRG for RX.
1	0	Transmitter and Receiver uses same BRG. Writing to DLL, DLM and DLD[5:0] has no effect on BRG used by the TX and RX.

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

3.16 Trigger Level Register (TRG) - Write-Only

User Programmable Transmit/Receive Trigger Level Register.

TRG[7:0]: Trigger Level Register

These bits are used to program desired trigger levels when trigger Table-D is selected. FCTR bit-7 selects between programming the RX Trigger Level (a logic 0) and the TX Trigger Level (a logic 1).

3.17 RX/TX FIFO Level Count Register (FC) - Read-Only

This register replaces SPR (during a read) and is accessible when FCTR[6] = 1. This register is also accessible when LCR = 0xBF. It is suggested to read the FIFO Level Count Register at the Scratchpad Register location when FCTR bit-6 = 1. See Table 14.

FC[7:0]: RX/TX FIFO Level Count

Receive/Transmit FIFO Level Count. Number of characters in Receiver FIFO (FCTR[7] = 0) or Transmitter FIFO (FCTR[7] = 1) can be read via this register.

3.18 Feature Control Register (FCTR) - Read/Write

FCTR[0]: SLEEP/PWRDN# Function Control

- Logic 0 = SLEEP pin (input) is enabled. This pin can be used to force the XR16M890 to enter the sleep mode immediately after the next data byte that is being transmitted on the TX pin and being received on the RX pin has been completed.
- Logic 1 = PWRDN# pin (output) is enabled. When the XR16M890 enters the sleep mode, this pin will be LOW. When the XR16M890 is not in sleep mode, this pin will be HIGH.

FCTR[1]: Reserved

This bit is reserved and should be ’0’.

FCTR[2]: IrDa RX Inversion

- Logic 0 = Select RX input as encoded IrDa data (Idle state will be LOW).
- Logic 1 = Select RX input as inverted encoded IrDa data (Idle state will be HIGH).

FCTR[3]: Auto RS-485 Direction Control

- Logic 0 = Standard ST16C550 mode. Transmitter generates an interrupt when transmit holding register becomes empty and transmit shift register is shifting data out.
- Logic 1 = Enable Auto RS485 Direction Control function. The direction control signal, RTS# pin, changes its output logic state from LOW to HIGH one bit time after the last stop bit of the last character is shifted out. Also, the Transmit interrupt generation is delayed until the transmitter shift register becomes empty. The RTS# output pin will automatically return to a LOW when a data byte is loaded into the TX FIFO. However, RTS# behavior can be inverted by setting EMSR[3] = 1.

FCTR[5:4]: Transmit/Receive Trigger Table Select

See Table 17 for more details.

TABLE 17: TRIGGER TABLE SELECT

FCTR BIT-5	FCTR BIT-4	TABLE
0	0	Table-A (TX/RX)
0	1	Table-B (TX/RX)
1	0	Table-C (TX/RX)
1	1	Table-D (TX/RX)

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FCTR[6]: Scratchpad Swap

- Logic 0 = Scratch Pad register is selected as general read and write register. ST16C550 compatible mode.
- Logic 1 = FIFO Count register (Read-Only), Enhanced Mode Select Register (Write-Only). Number of characters in transmit or receive FIFO can be read via scratch pad register when this bit is set. Enhanced Mode Select Register is selected when it is written into.

FCTR[7]: Programmable Trigger Register Select

- Logic 0 = Registers TRG and FC selected for RX.
- Logic 1 = Registers TRG and FC selected for TX.

3.19 Enhanced Feature Register (EFR) - Read/Write

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see Table 18). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[3:0]: Software Flow Control Select

Single character and dual sequential characters software flow control is supported. Combinations of software flow control can be selected by programming these bits.

TABLE 18: SOFTWARE FLOW CONTROL FUNCTIONS

EFR BIT-3 CONT-3	EFR BIT-2 CONT-2	EFR BIT-1 CONT-1	EFR BIT-0 CONT-0	TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	No transmit flow control, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 3-5, MCR bits 5-7, DLD, SHR and SFR to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 3-5, MCR bits 5-7, DLD, SHR and SFR are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 3-5, and MCR bits 5-7, DLD, SHR and SFR are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the EFR[3:0] register bits to be modified by the user.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the receive data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit of the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]= '10') then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]= '01') then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt, if enabled via IER bit-5.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS de-asserts HIGH at the next upper trigger level/hysteresis level. RTS# will return LOW when FIFO data falls below the next lower trigger level/hysteresis level. The RTS# output must be asserted (LOW) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled (default).
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled (default).
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts to logic 1. Data transmission resumes when CTS# returns to a logic 0.

3.20 Software Flow Control Registers (XOFF1, XOFF2, XON1, XON2) - Read/Write

These registers are used as the programmable software flow control characters xoff1, xoff2, xon1, and xon2. For more details, see Table 5. The xoff2 is also used as auto address detect register when the auto 9-bit mode enabled. See "Section 1.17.1, Auto Address Detection - Receiver" on page 23.

3.21 GPIO Interrupt Enable Register (GPIOINT) - Read/Write

If a GPIO has been configured as an input, this register selects which inputs can generate a GPIO interrupt. This register controls GPIO[7:0] when SFR[1] = 0 and GPIO[15:8] when SFR[1] = 1.

- Logic 0 = GPIO interrupt for this input pin is not enabled.
- Logic 1 = GPIO interrupt for this input pin is enabled.

3.22 GPIO Three-State Control Register (GPIO3T) - Read/Write

If a GPIO has been configured as an output, this register selects which outputs will be in three-state mode. This register controls GPIO[7:0] when SFR[1] = 0 and GPIO[15:8] when SFR[1] = 1.

- Logic 0 = GPIO output is in active mode and can be controlled via GPIOLVL register.
- Logic 1 = GPIO output is in three-state mode.

3.23 GPIO Polarity Control Register (GPIOINV) - Read/Write

If a GPIO has been configured as an interrupt, this register selects the polarity that can generate a GPIO interrupt. This register controls GPIO[7:0] when SFR[1] = 0 and GPIO[15:8] when SFR[1] = 1.

- Logic 0 = GPIO interrupt is generated when this input pin transitions from LOW to HIGH. Read GPIOLVL returns GPIO pin state.
- Logic 1 = GPIO interrupt is generated when this input pin transitions from HIGH to LOW. Read GPIOLVL returns inverted GPIO pin state.

3.24 GPIO Select Register (GPIOSEL) - Read/Write

This register selects where a GPIO is an input or an output.

- Logic 0 = GPIO is an output.
- Logic 1 = GPIO is an input (default).

The Product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

TABLE 19: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLM, DLL (Both TX and RX)	DLM = 0x00 and DLL = 0x01. Only resets to these values during a power up. They do not reset when the Reset Pin is asserted.
DLD	Bits 7-0 = 0x00
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
SHR	Bits 7-0 = 0x00
MSR	Bits 7-0 =0xX0 (Bits 7-4 = complement of modem inputs)
SFR	Bits 7-0 = 0x00
SPR	Bits 7-0 = 0xFF
GPIOLVL	Bits 7-0 = 0x00
EMSR	Bits 7-0 = 0x00
FC	Bits 7-0 = 0x00
TRG	Bits 7-0 = 0x01
FCTR	Bits 7-0 = 0x00
EFR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
GPIOINT	Bits 7-0 = 0x00
GPIO3T	Bits 7-0 = 0x00
GPIOINV	Bits 7-0 = 0x00
GPIOSEL	Bits 7-0 = 0xFF
I/O SIGNALS	**RESET STATE**
TX	HIGH
RTS#	HIGH
DTR#	HIGH
INT (Intel or VLIO mode) IRQ# (Motorola mode)	Three-State Condition HIGH

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	3.63 Volts
Voltage at Any Pin	GND-0.3 V to 3.63 V
Operating Temperature	-40° to +85°C
Storage Temperature	-65° to +150°C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (32-QFN)	theta-ja = 33°C/W, theta-jc = 22°C/W
Thermal Resistance (40-QFN)	theta-ja = 32°C/W, theta-jc = 16°C/W
Thermal Resistance (48-TQFP)	theta-ja = 59°C/W, theta-jc = 16°C/W

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC_XXXX IS 1.62V TO 3.63V

SYMBOL	PARAMETER	LIMITS 1.8V MIN	LIMITS 1.8V MAX	LIMITS 2.5V MIN	LIMITS 2.5V MAX	LIMITS 3.3V MIN	LIMITS 3.3V MAX	UNITS	CONDITIONS
V_{ILCK}	Clock Input Low Level	-0.3	0.3	-0.3	0.4	-0.3	0.6	V	(XTAL1 input)
V_{IHCK}	Clock Input High Level	1.4	VCC_CORE	2.0	VCC_CORE	2.4	VCC_CORE	V	
V_{IL}	Input Low Voltage	-0.3	0.2	-0.3	0.5	-0.3	0.7	V	
V_{IH}	Input High Voltage	1.4	5.5	1.8	5.5	2.0	5.5	V	
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V V V	I_{OL} = 6 mA I_{OL} = 4 mA I_{OL} = 1.5 mA
V_{OH}	Output High Voltage	1.4		1.8		2.0		V V V	I_{OH} = -4 mA I_{OH} = -2 mA I_{OH} = -200 uA
I_{IL}	Input Low Leakage Current		±15		±15		±15	uA	
I_{IH}	Input High Leakage Current		±15		±15		±15	uA	
C_{IN}	Input Pin Capacitance		5		5		5	pF	
I_{CC}	Power Supply Current		2		3		4	mA	Ext Clk = 5MHz
I_{SLEEP}	Sleep Current		5		10		20	uA	See Test 1

Test 1: All inputs should remain steady at VCC or GND to minimize Sleep current. RX input must idle at HIGH while asleep.

AC ELECTRICAL CHARACTERISTICS

TA = -40° TO +85°C, VCC IS 1.62 TO 3.63V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 1.8V ± 10%		LIMITS 2.5V ± 10%		LIMITS 3.3V ± 10%		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
XTAL1	UART Crystal Frequency		24		24		24	MHz
ECLK	External Clock Frequency		36		64		100	MHz
T_{ECLK}	External Clock Time Period	13		7		5		ns
16 Mode (Intel) Data Bus Read/Write Timing								
T_{AS}	Address Setup Time	0		0		0		ns
T_{AH}	Address Hold Time	0		0		0		ns
T_{CS}	Chip Select Width	50		45		40		ns
T_{RD}	IOR# Strobe Width	50		45		40		ns
T_{DY}	Read Cycle Delay	50		45		40		ns
T_{RDV}	Data Access Time		45		40		35	ns
T_{DD}	Data Disable Time		25		20		15	ns
T_{WR}	IOW# Strobe Width	50		45		40		ns
T_{DY}	Write Cycle Delay	50		45		40		ns
T_{DS}	Data Setup Time	30		25		20		ns
T_{DH}	Data Hold Time	0		0		0		ns
68 Mode (Motorola) Data Bus Read/Write Timing								
T_{ADS}	Address Setup	0		0		0		ns
T_{ADH}	Address Hold	0		0		0		ns
T_{RWS}	R/W# Setup to CS#	0		0		0		ns
T_{RDA}	Data Access Time		45		40		35	ns
T_{RDH}	Data Disable Time		25		15		10	ns
T_{WDS}	Write Data Setup	20		15		10		ns
T_{WDH}	Write Data Hold	3		3		3		ns
T_{RWH}	CS# De-asserted to R/W# De-asserted	0		0		0		ns
T_{CSL}	CS# Strobe Width	50		45		40		ns
T_{CSD}	CS# Cycle Delay	50		45		40		ns

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

AC ELECTRICAL CHARACTERISTICS

TA = -40° TO +85°C, VCC IS 1.62 TO 3.63V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 1.8V ± 10% MIN	LIMITS 1.8V ± 10% MAX	LIMITS 2.5V ± 10% MIN	LIMITS 2.5V ± 10% MAX	LIMITS 3.3V ± 10% MIN	LIMITS 3.3V ± 10% MAX	UNIT
VLIO Data Bus Read/Write Timing								
T_{AS}	Address Setup Time	15		15		10		ns
T_{AH}	Address Hold Time	5		5		5		ns
T_{CSL}	Delay from CS# to LLA#/IOR#/IOW#	0		0		0		ns
T_{LLA}	LLA# Strobe Width	10		10		10		ns
T_{RD}	IOR# Strobe Width	50		45		40		ns
T_{LLAR}	Delay from LLA# to IOR#	5		5		5		ns
T_{LLAW}	Delay from LLA# to IOW#	5		5		5		ns
T_{DY}	Read/Write Cycle Delay	50		45		40		ns
T_{RDV}	Data Access Time		45		40		35	ns
T_{DD}	Data Disable Time		25		20		15	ns
T_{WR}	IOW# Strobe Width	50		45		40		ns
T_{DS}	Data Setup Time	15		15		15		ns
T_{DH}	Data Hold Time	5		5		5		ns
Modem/Interrupt Timing								
T_{WDO}	Delay From IOW# To Output		50		50		50	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		50		50		50	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		50		50		50	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45		45		45	ns
T_{SI}	Delay From Start To Interrupt		45		45		45	ns
T_{WTS}	Delay From Initial IOW# To Transmit Start (SHR[7:4] = 0x0)	8	33	8	33	8	33	Bclk
T_{WTS}	Delay From Initial IOW# To Transmit Start (SHR[7:4] = 0xF)	8	48	8	48	8	48	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		45		45		45	ns
T_{SSR}	Delay From Stop To Set RXRDY#		1		1		1	Bclk
T_{RR}	Delay From IOR# To Reset RXRDY#		45		45		45	ns
T_{WT}	Delay From IOW# To Set TXRDY#		45		45		45	ns
T_{SRT}	Delay From Center of Start To Reset TXRDY#		8		8		8	Bclk
T_{RST}	Reset Pulse Width	40		40		40		ns
Bclk	Baud Clock	16X or 8X or 4X of data rate						Hz

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 18. CLOCK TIMING

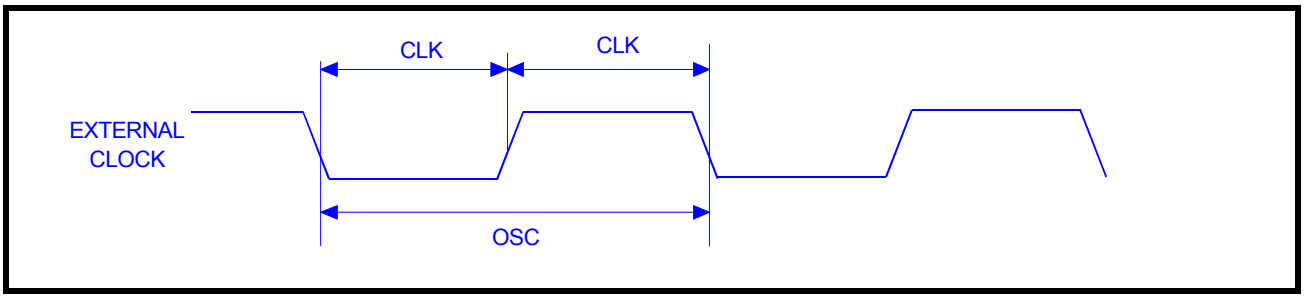

FIGURE 19. MODEM INPUT/OUTPUT TIMING

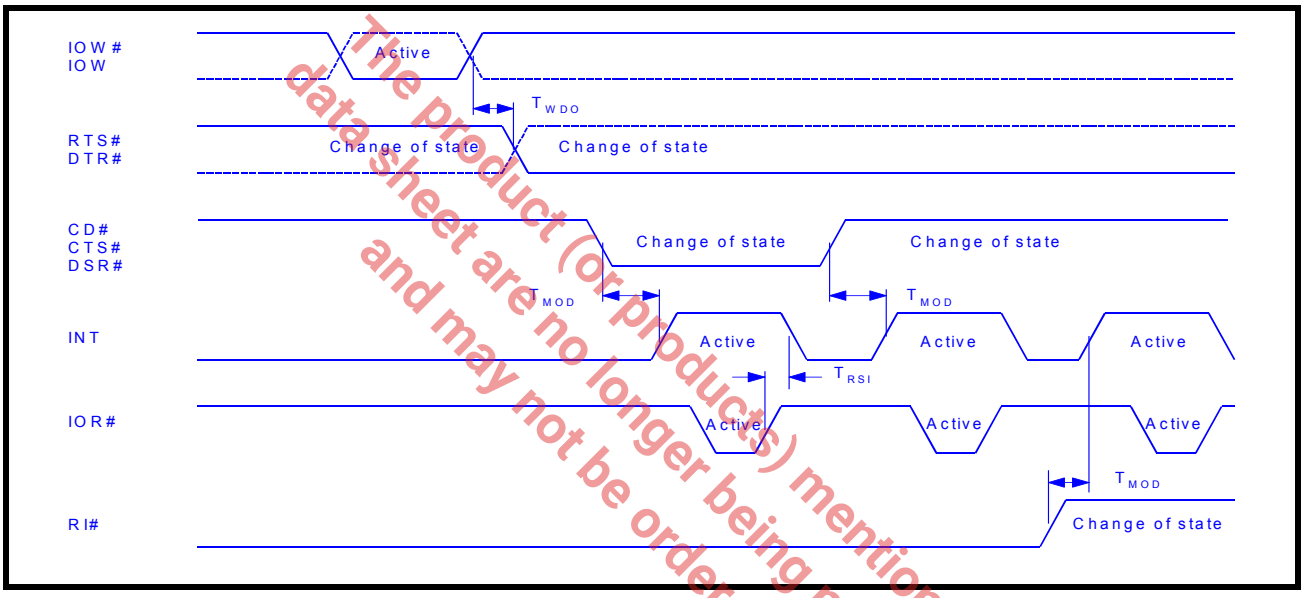

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FIGURE 20. 16 MODE (INTEL) DATA BUS READ TIMING

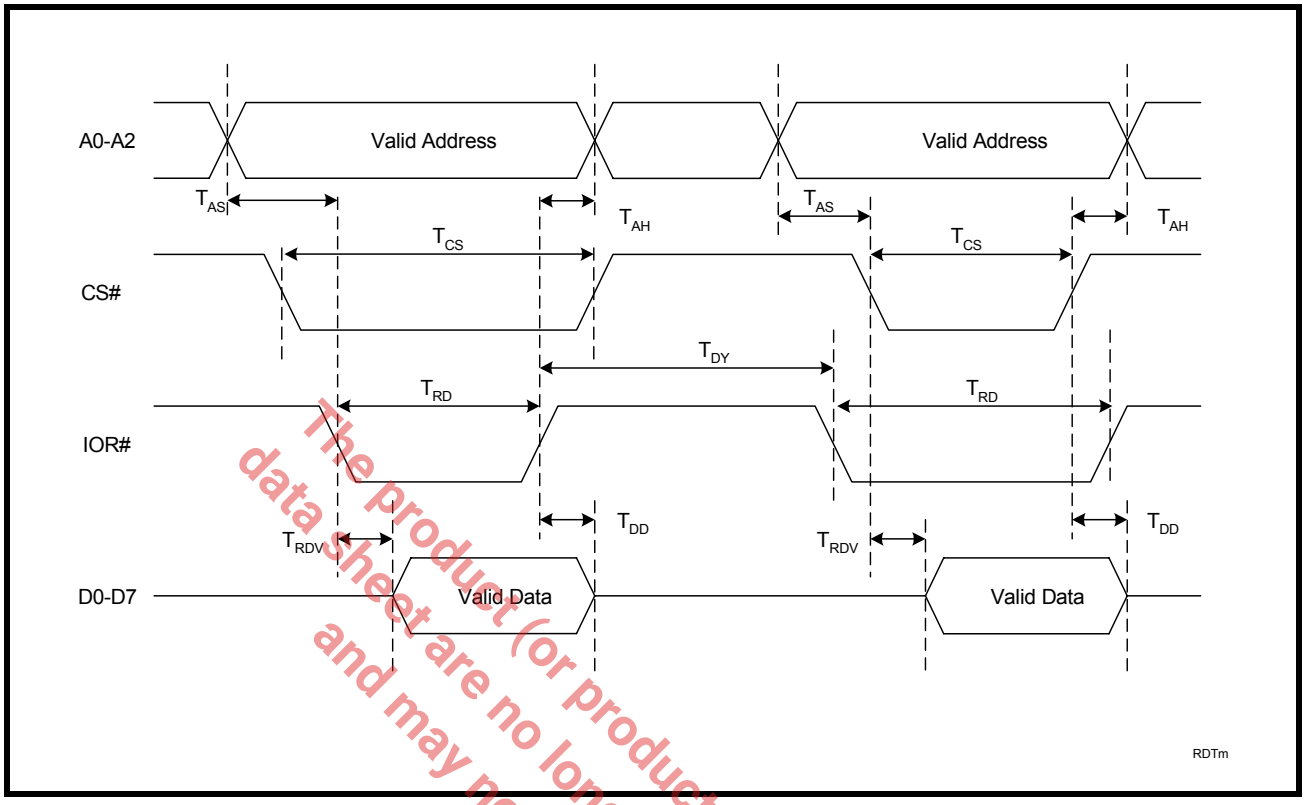
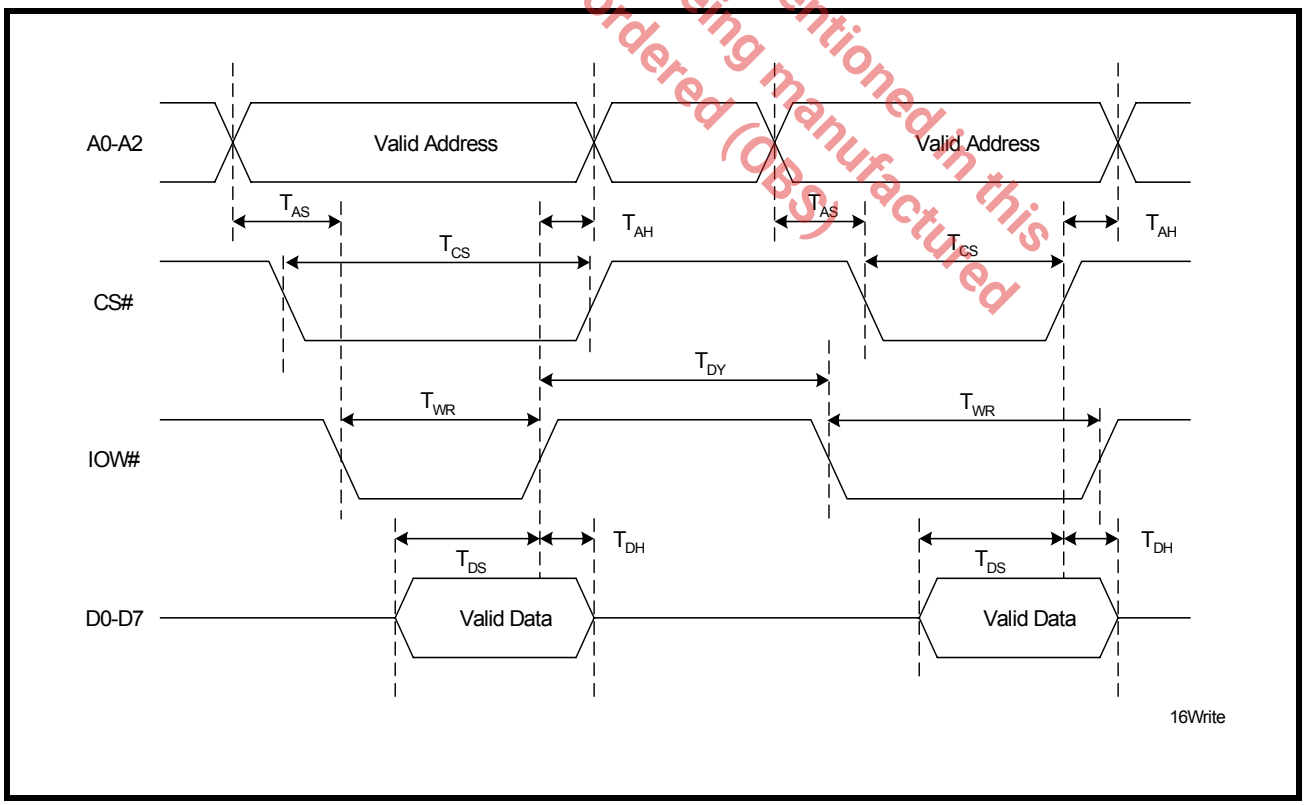


FIGURE 21. 16 MODE (INTEL) DATA BUS WRITE TIMING



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 22. 68 MODE (MOTOROLA) DATA BUS READ TIMING

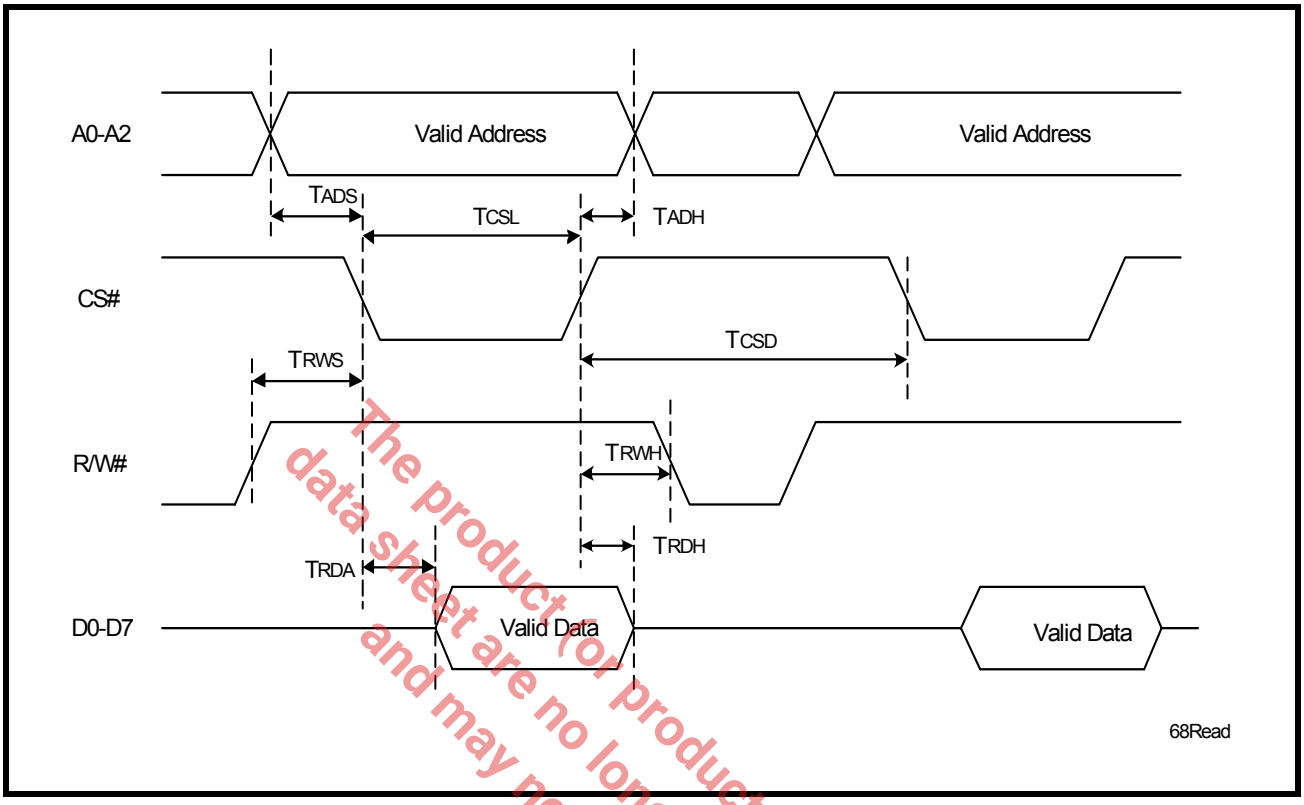
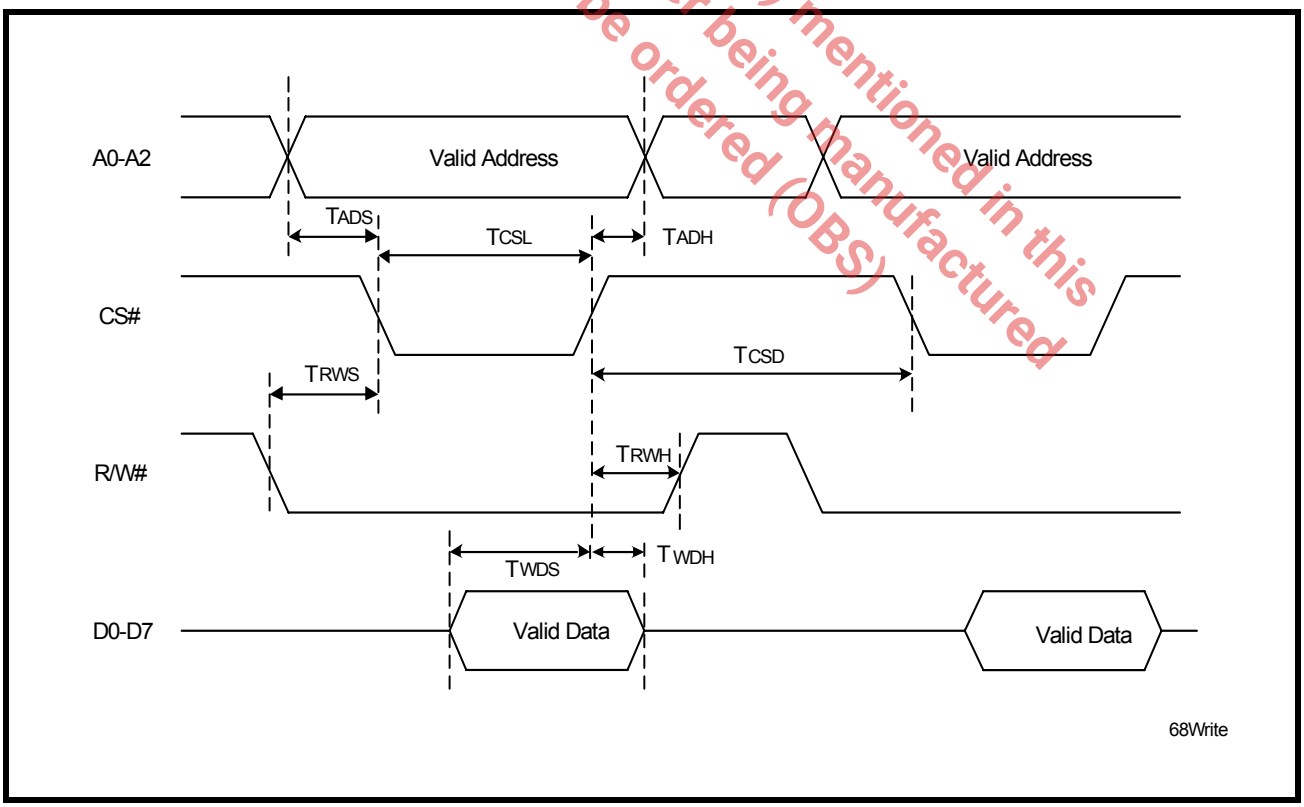
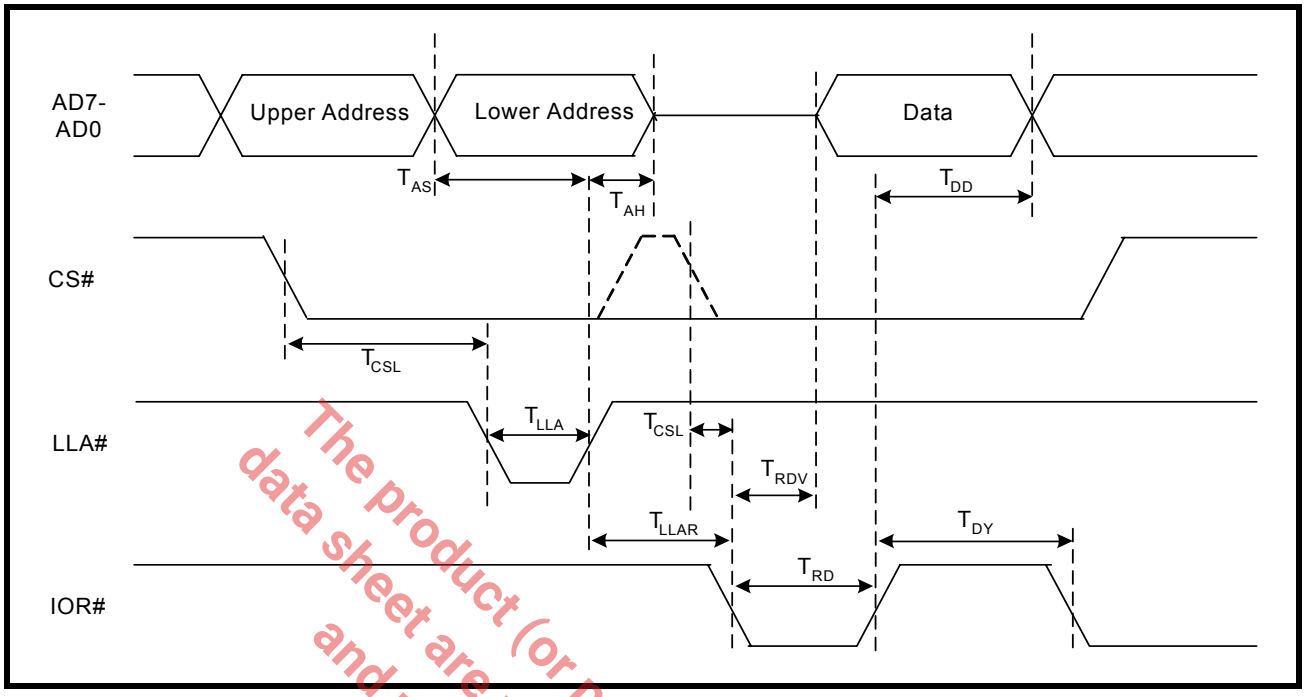


FIGURE 23. 68 MODE (MOTOROLA) DATA BUS WRITE TIMING



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 24. VLIO MODE DATA BUS READ TIMING



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 25. VLIO MODE DATA BUS WRITE TIMING

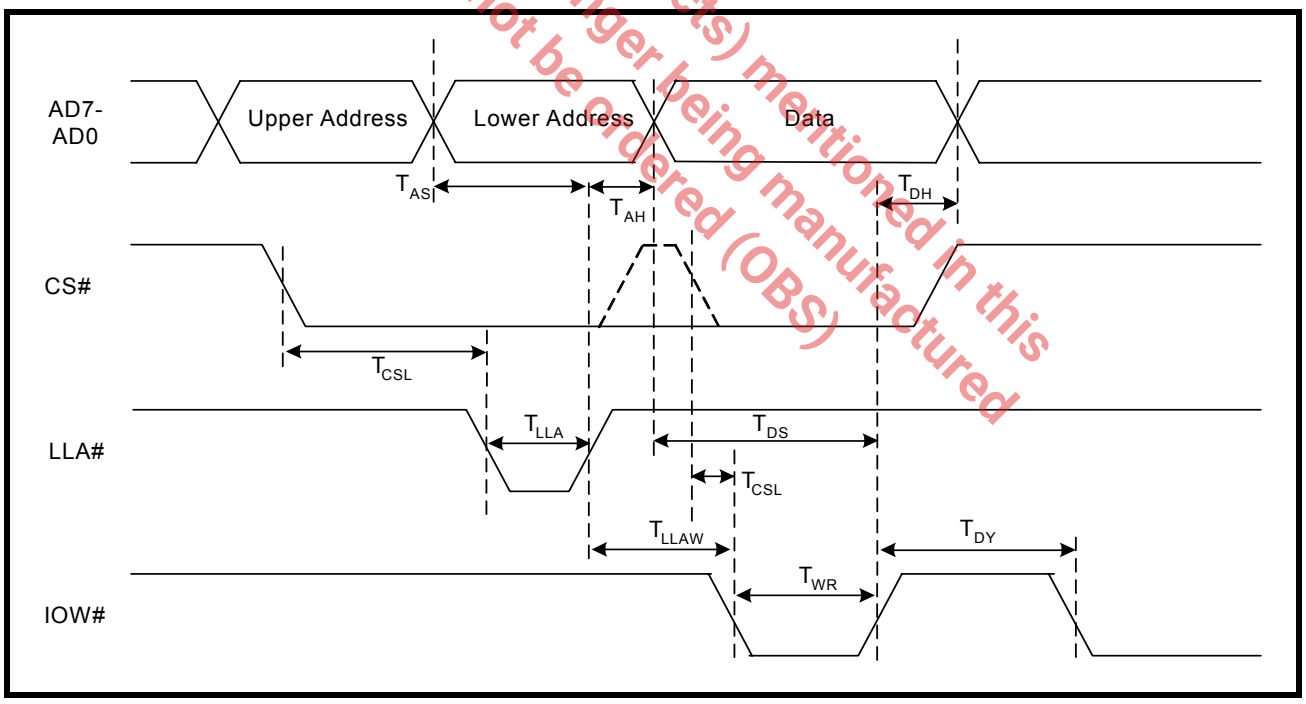
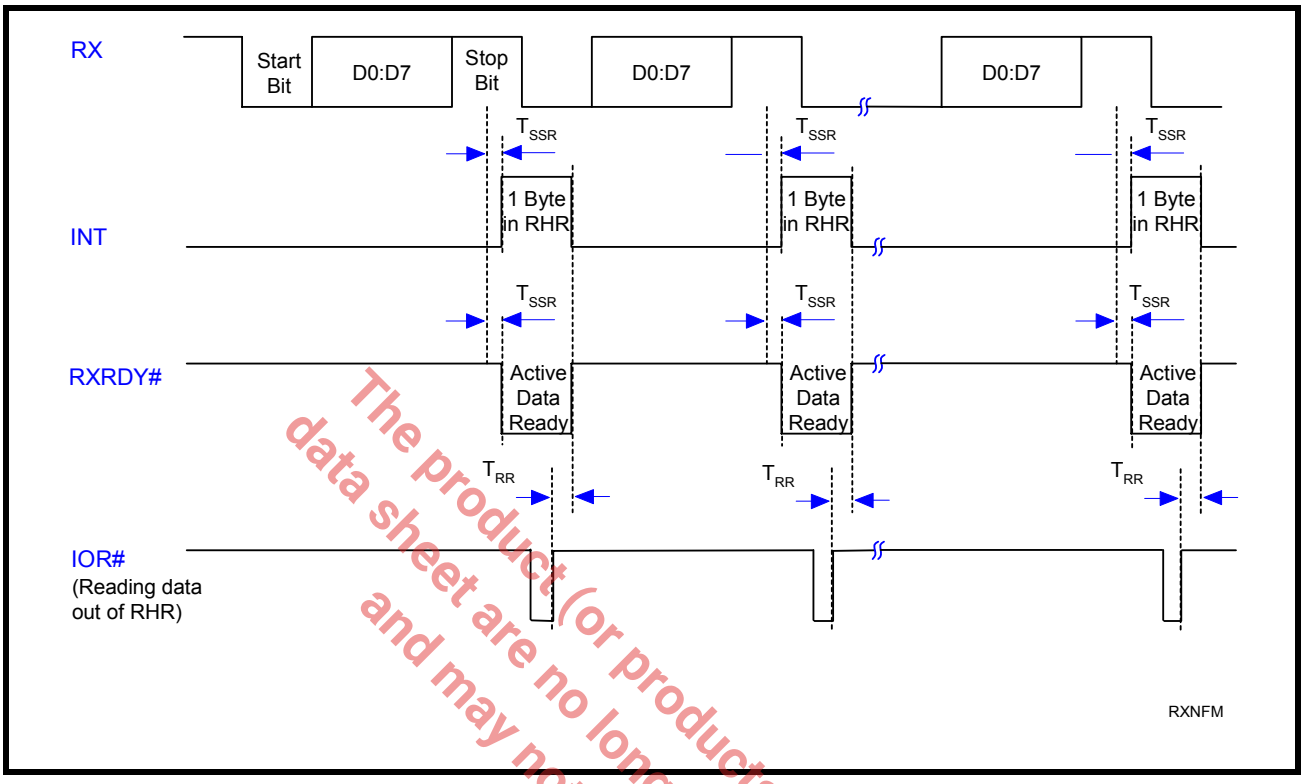


FIGURE 26. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE]



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 27. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE]

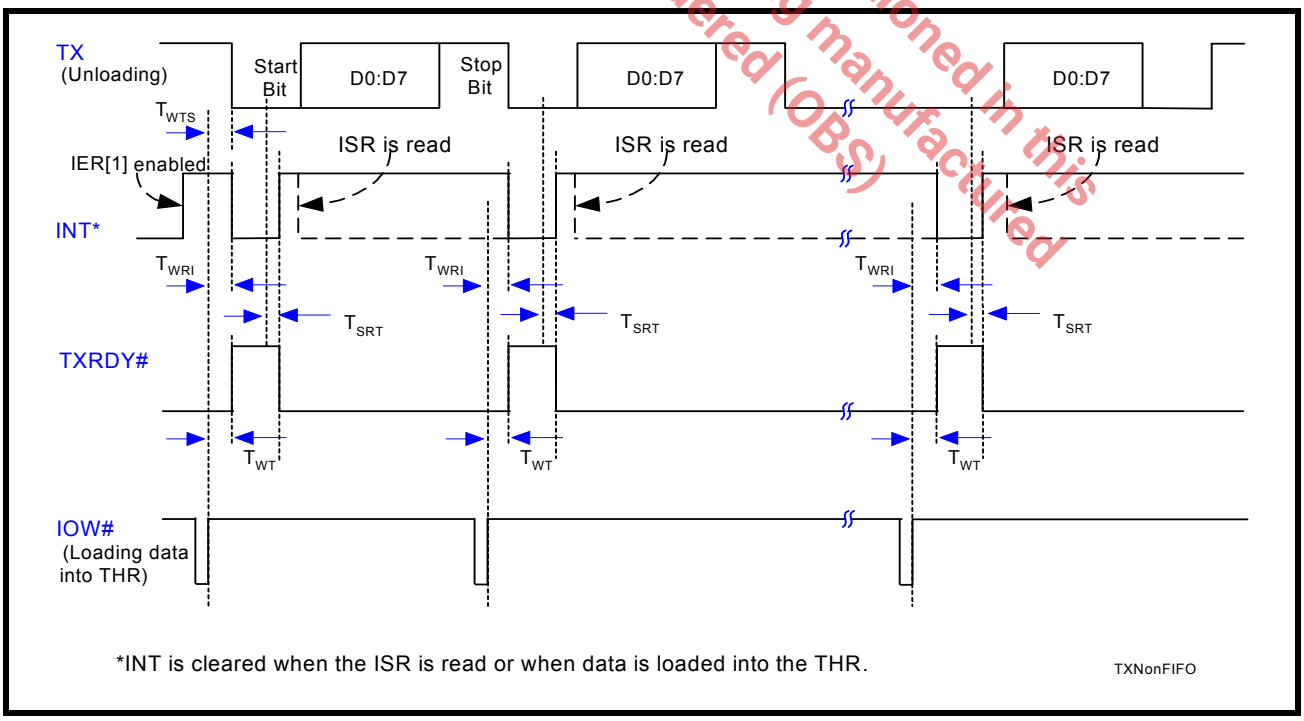


FIGURE 28. RECEIVE READY & INTERRUPT TIMING [FIFO MODE]

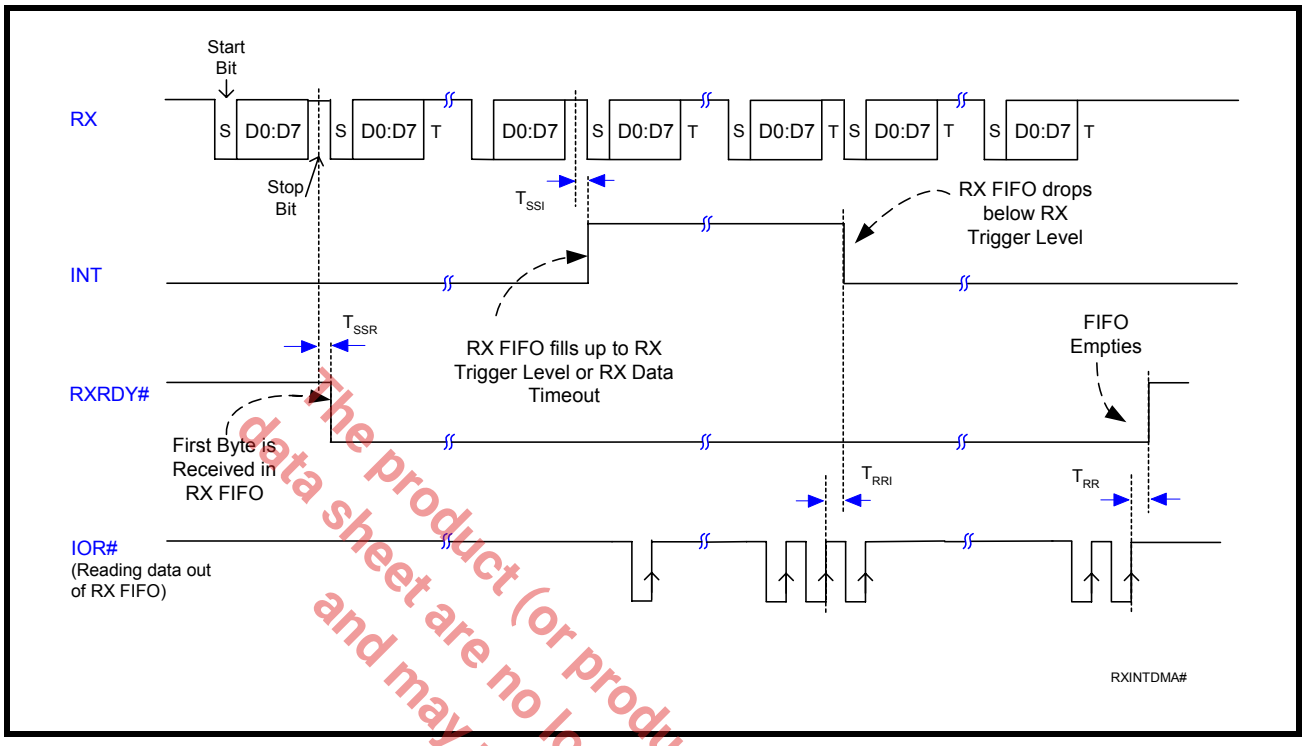
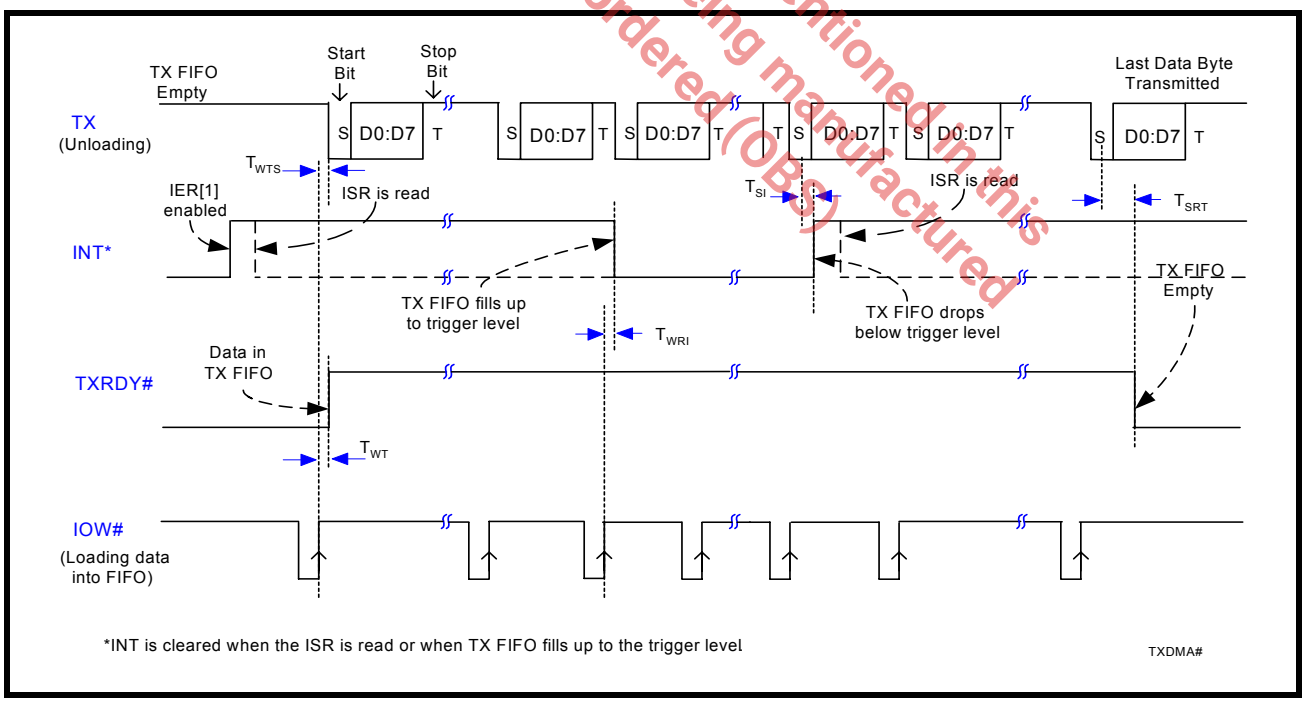
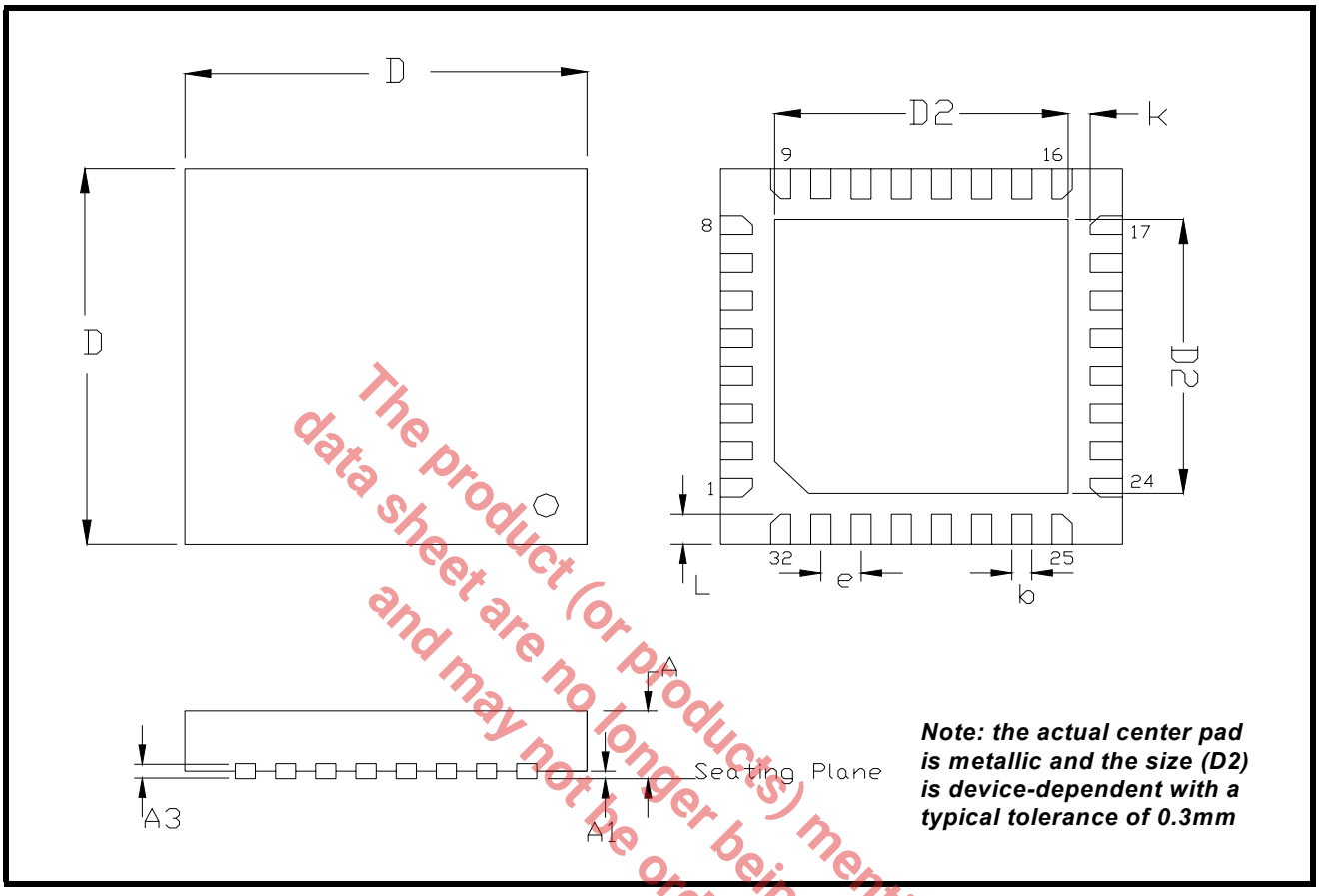


FIGURE 29. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE]



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

PACKAGE DIMENSIONS (32 PIN QFN - 5 X 5 X 0.9 mm)



Note: the actual center pad is metallic and the size (D2) is device-dependent with a typical tolerance of 0.3mm

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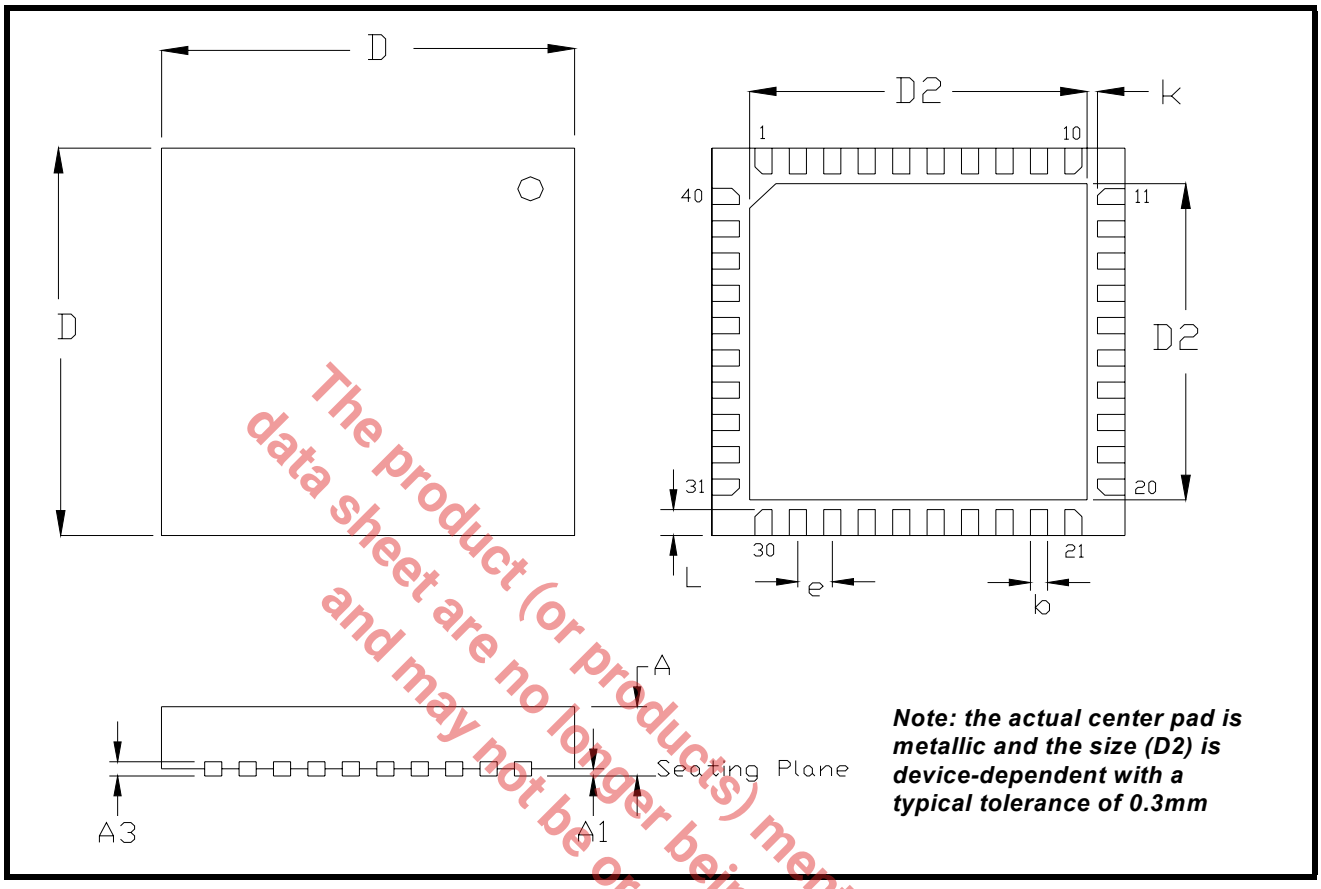
Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.006	0.010	0.15	0.25
D	0.193	0.201	4.90	5.10
D2	0.138	0.150	3.50	3.80
b	0.007	0.012	0.18	0.30
e	0.0197 BSC		0.50 BSC	
L	0.012	0.020	0.35	0.45
k	0.008	-	0.20	-

PACKAGE DIMENSIONS (40 PIN QFN - 6 X 6 X 0.9 mm)



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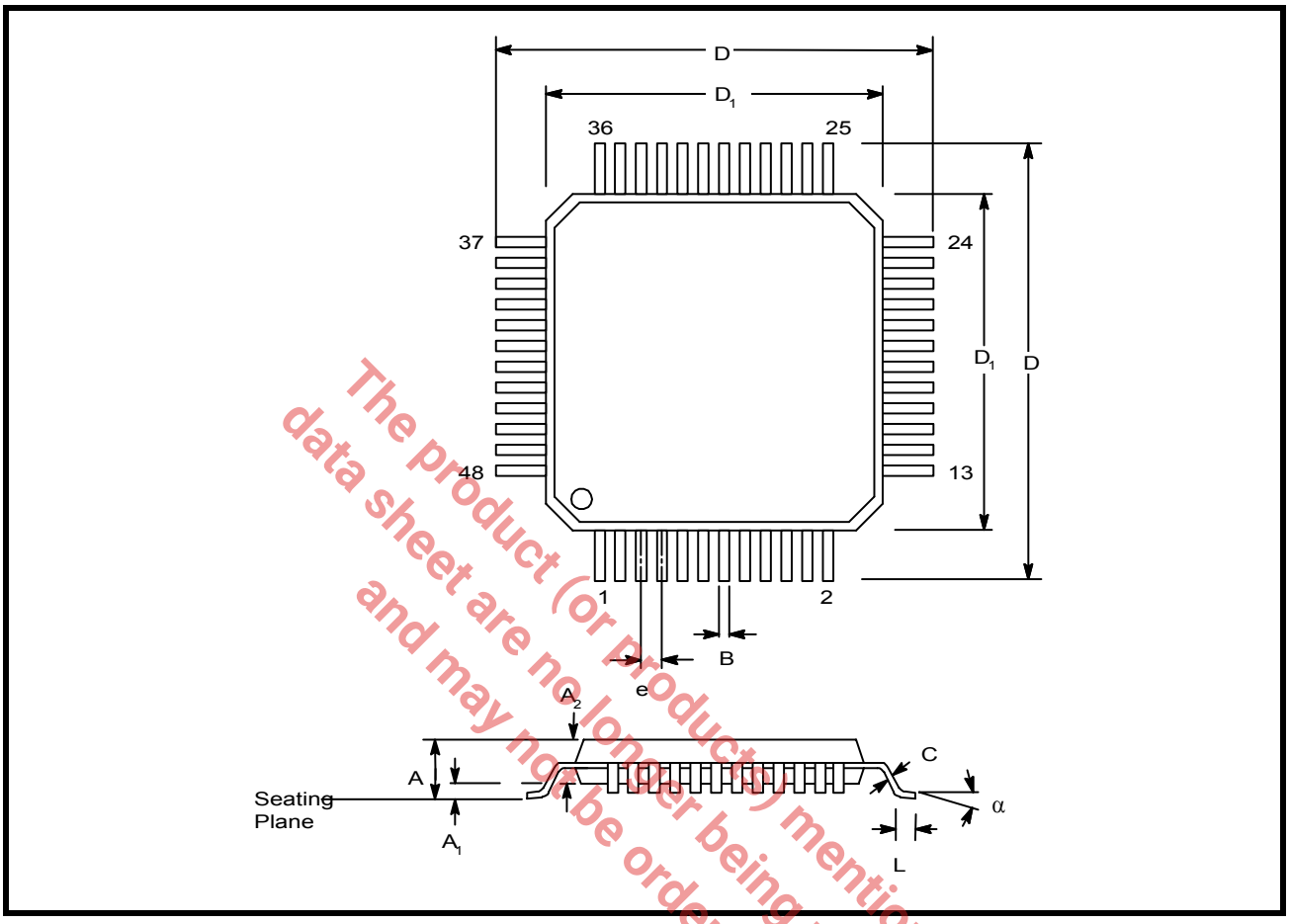
Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.006	0.010	0.15	0.25
D	0.232	0.240	5.90	6.10
D2	0.189	0.197	4.80	5.00
b	0.007	0.012	0.18	0.30
e	0.0197 BSC		0.50 BSC	
L	0.014	0.018	0.35	0.45
k	0.008	-	0.20	-

PACKAGE DIMENSIONS (48 PIN TQFP - 7 X 7 X 1 mm)



The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A1	0.002	0.006	0.05	0.15
A2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISION HISTORY

DATE	REVISION	DESCRIPTION
April 2011	1.0.0	Final Datasheet.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

NOTICE

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