GENERAL DESCRIPTION

The XRP7740 is a quad-output pulse-width modulated (PWM) step-down DC-DC controller with a built-in LDO for standby power and GPIOs. The device provides a complete power management solution in one IC and is fully programmable via an I²C serial interface. Independent Digital Pulse Width Modulator (DPWM) channels regulate output voltages and provide all required protection functions such as current limiting and over-voltage protection.

Each output voltage can be programmed from 0.9V to 5.1V without the need of an external voltage divider. The wide range of the programmable DPWM switching frequency (from 300 KHz to 1.5 MHz) enables the user to optimize between efficiency and component size. Input voltage range is from 6.5V to 20V. An I²C bus interface is provided to program the IC as well as to communicate with the host for fault reporting and handling, power rail parameters monitoring, etc.

The device offers a complete solution for soft-start and soft-stop. The start-up delay and ramp of each PWM regulator can be independently controlled. The device can start up a pre-biased PWM channel without causing large negative inductor current.

APPLICATIONS

- **Multi Channel Programmable Power Supplies**
- **Audio-Video Equipment**
- **Industrial & Telecom Equipment**
- **Processors & DSPs Based Equipment**

FEATURES

- **4 Channel Step Down Controller**
  - 3ohm/1.8ohm driver
  - Programmable Output Voltage 0.9V to 5.1V
  - Programmable 1.5MHz DPWM Frequency
- **6.5V-20V Single Input Voltage Range**
- **Up to 6 Reconfigurable GPIO Pins**
- **Fully Programmable via I²C Interface**
- **Independent Digital Pulse Width Modulator (DPWM) channels**
- **Complete Monitoring and Reporting**
- **Complete Power Up/Down Sequencing**
- **Full On Board Protection OTP, UVLO, OCP and OVP**
- **Built-in 3.3V/5V LDO**
- **PowerArchitect™ Design Software**
- **Green/Halogen Free 40-pin TQFN**

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TYPICAL APPLICATION DIAGRAM

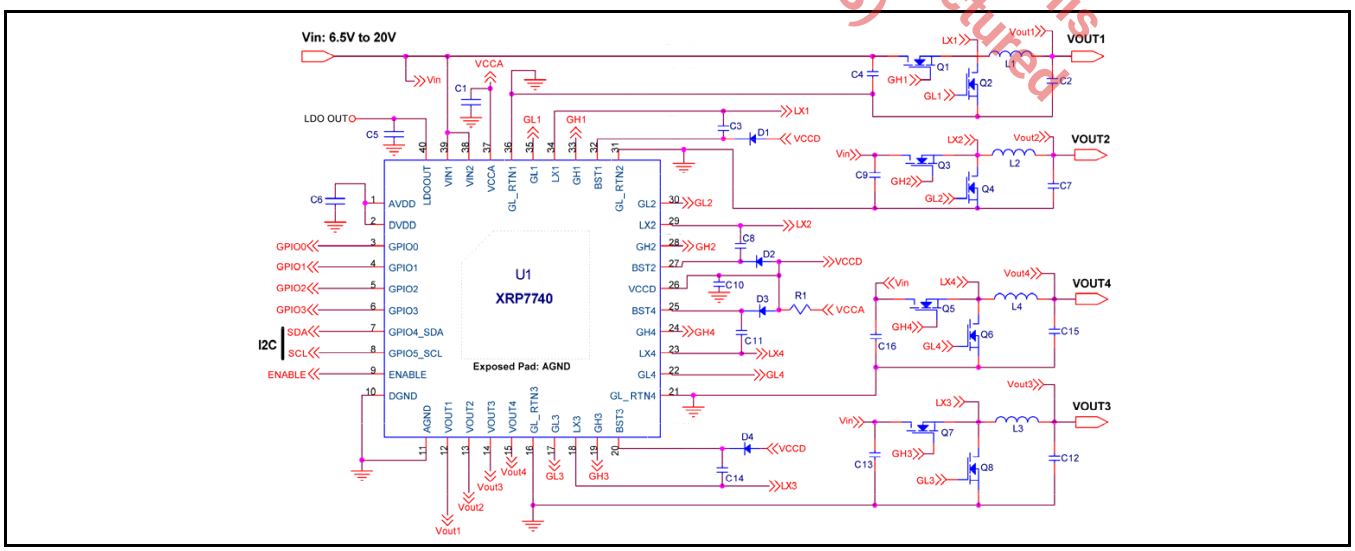


Fig. 1: XRP7740 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

VCCA, VCCD, LDOOUT, GLx, VOUTx..... 6V
AVDD, DVDD 2.0V
VIN1, VIN2 ..... 22V
LXx.....-1V to 22V
Logic Inputs..... 6V
BSTx, GHx.....VLXx + 5V
Storage Temperature..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

OPERATING RATINGS

Operating Input Voltage VIN_X .....6.5V to 20V
Junction Temperature Range .....-40°C to 125°C
Thermal Resistance θ_{JA} .....24.3°C/W

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ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, VIN_1 = 6.5V to 20V, VIN_2 = 6.5V to 20V, Enable=HIGH, C_{GL} = C_{GH} = 1nF.

Quiescent Current

Parameter	Min.	Typ.	Max.	Units		Conditions
VIN Supply Current in STANDBY		9		mA		LDOOUT enabled (no load) No switching converter channels enabled I^2C communication active Switching frequency = 400kHz
VIN Supply Current in SHUTDOWN		180		µA		EN = 0V, VIN1 = VIN2 = 12V
VIN Supply Current		28		mA		4 channels running, GH and GH = 1nF load each VIN=12V, Switching frequency = 300kHz
VIN Supply Current		50		mA		4 channels running, GH and GH = 1nF load each VIN=12V, Switching frequency = 1MHz

Step Down Controllers

Parameter	Min.	Typ.	Max.	Units		Conditions
VOUT Regulation Accuracy	-20		20	mV	•	0.9V ≤ VOUT ≤ 2.5V
	-40		40	mV	•	2.6V ≤ VOUT ≤ 5.1V
VOUT regulation range	0.9		5.1		•	Programmable range of each channel[1]
VOUT set point resolution		50				0.9V ≤ VOUT ≤ 2.5V
VOUT set point resolution		100				2.6V ≤ VOUT ≤ 5.1V
VOUT Input Current			1	µA	•	0.9V < VOUT ≤ 2.5V
VOUT Input Resistance		120		kΩ		2.6V ≤ VOUT ≤ 5.1V

Note 1: Voltages above 5.1V can be obtained by using an external voltage divider.

Low Drop-out Regulator

Parameter	Min.	Typ.	Max.	Units		Conditions
LDOOUT Output Voltage LDO=LOW	3.15	3.3	3.45	V	•	6.5V ≤ VIN1 ≤ 20V 0mA < I_{LDOOUT} < 100mA
LDOOUT Output Voltage LDO=HIGH	4.75	5.0	5.25	V	•	6.5V ≤ VIN1 ≤ 20V 0mA < I_{LDOOUT} < 100mA
LDOOUT Short Circuit Current Limit	110		220	mA	•	V_{LDOOUT} = 0V

Auxiliary ADCs

Parameter	Min.	Typ.	Max.	Units		Conditions
Linearity Error Integral			2	LSB		
Linearity Error Differential	-1		1	LSB		
Input Dynamic Range VIN1	6.5		20	V	•	
Input Dynamic Range VIN2	6.5		20	V	•	

Isense ADC

Parameter	Min.	Typ.	Max.	Units		Conditions
ADC LSB		5		mV		Referred to the input
Input Dynamic Range	0		-320	mV		

PWM Generators and Oscillator

Parameter	Min.	Typ.	Max.	Units		Conditions
Output frequency range	300		1500	kHz	•	Steps defined in the table in the PWM Switching Frequency Setting section below
Channel-to-channel phase shift step		90		deg		With 4 phase setting
Channel-to-channel phase shift step		120		deg		With 3 phase setting
Minimum On Time		40		ns		1nF of gate capacitance
Minimum Off Time		125		ns		1nF of gate capacitance
CLOCK IN Synchronization Range	-5		5	%	•	

Digital Input/Output Pins (GPIO0-GPIO5)

3.3V CMOS logic compatible, 5V tolerant

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level			0.8	V	•	
Input Pin High Level	2.0			V	•	
Input Pin Leakage Current			10	µA	•	V_{IO} = 3.3V
Input pin Capacitance		5		pF		
Output Pin Low Level			0.4	V	•	I_{SINK} = 3mA
Output Pin High Level	2.4			V	•	I_{SOURCE} = 1mA
Output Pin High Level (no load)		3.3	3.6	V	•	I_{SOURCE} = 0mA

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I²C Specification

Parameter	Min.	Typ.	Max.	Units		Conditions
I²C Speed			400	kHz		Based upon I²C master clock
Input Pin Low Level, V_{IL}			1.0	V		
Input Pin High Level, V_{IH}	2.97			V		
Hysteresis of Schmitt Trigger Inputs, V_{HYS}	0.165			V		
Output Pin Low Level (open drain or collector) V_{OL}			0.4	V		I_{SINK}=3mA
Input Leakage Current	-10		10	µA		Input is between 0.33V and 2.97V
Output Fall Time from V_{IHMIN} to V_{ILMAX}	$20+0.1C_b$[2]		250	ns		With a bus capacitance from 10pF to 400pF
Capacitance for each I/O Pin			10	pF		

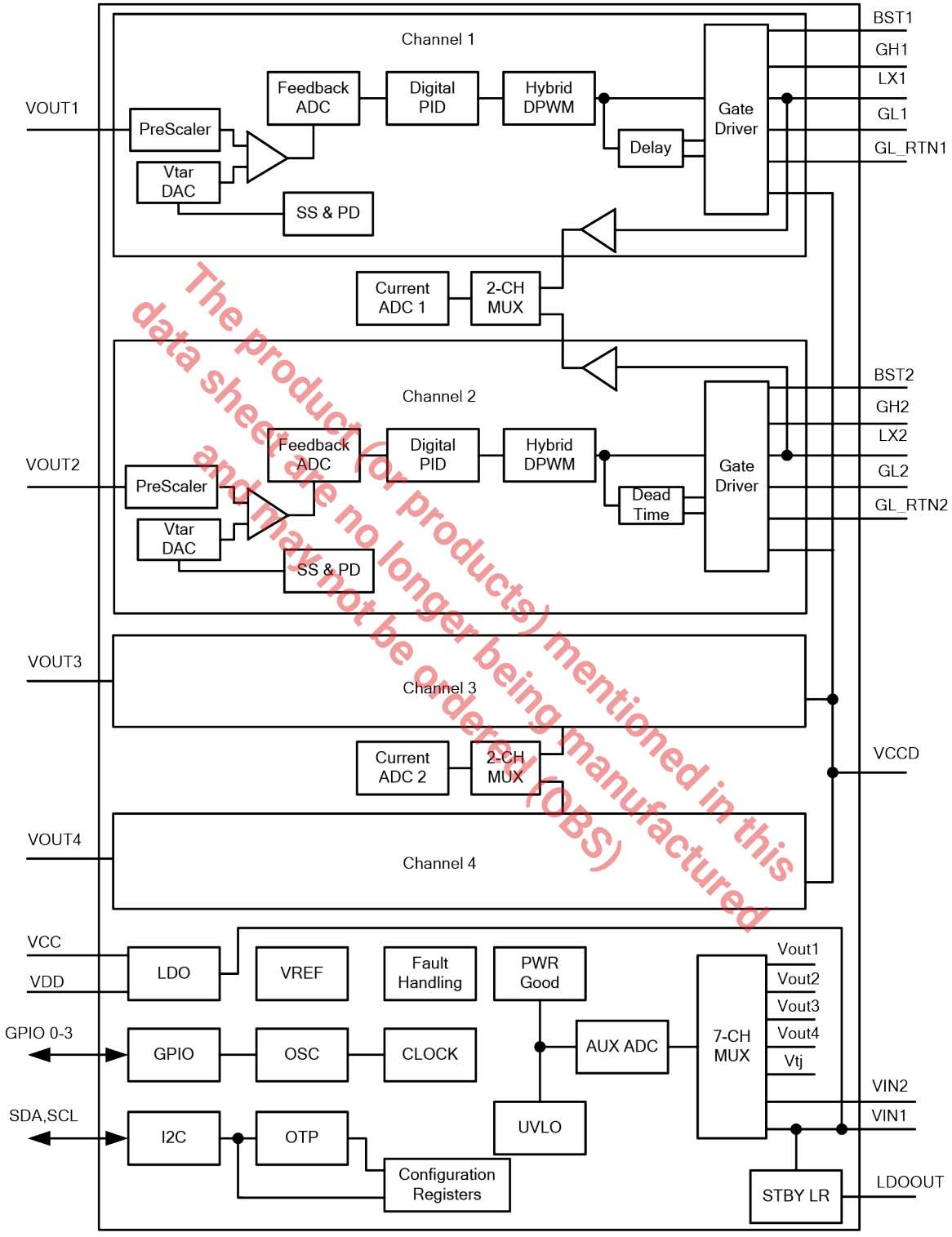
Note 2: C_b is the capacitance one one bus in pF

Gate Drivers

Parameter	Min.	Typ.	Max.	Units		Conditions
GH, GL Rise and Fall Time		30		ns		At 10% to 90% of full scale pulse. 1nF C_{load}
GH, GL Pull-up On-State Output Resistance		3		Ω		
GH, GL Pull-down On-State Output Resistance		1.8		Ω		
GH, GL Pull-down Off-State Output Resistance		50		kΩ		VIN = VCCD = 0V

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BLOCK DIAGRAM



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Fig. 2: XRP7740 Block Diagram

PIN ASSIGNMENT

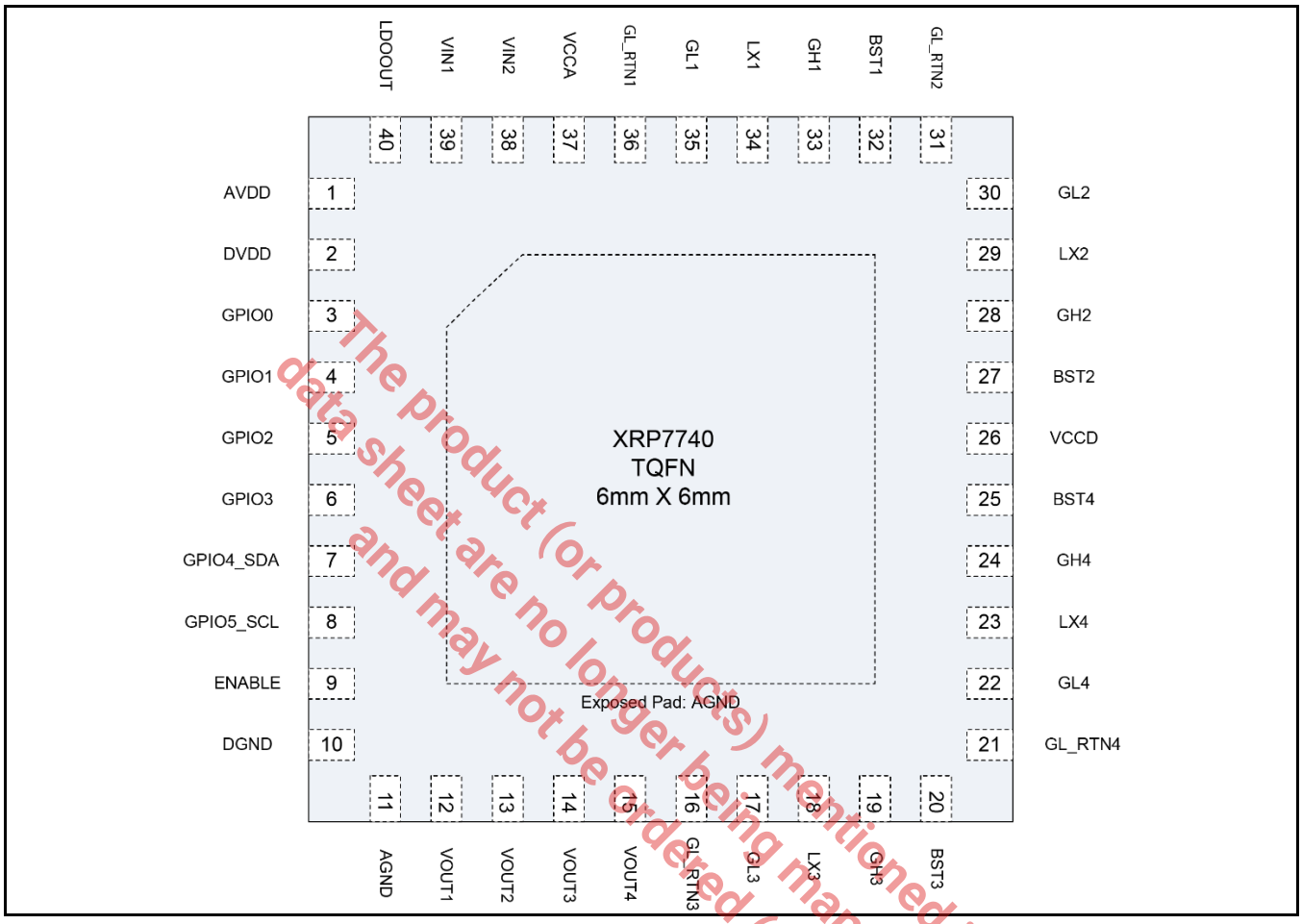


Fig. 3: XRP7740 Pin Assignment

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

PIN DESCRIPTION

Name	Pin Number	Description
VIN1	39	Power source for the internal linear regulators to generate VCCA, VDD and the Standby LDO (LDOOUT). Place a decoupling capacitor close to the controller IC. Also used in UVLO1 fault generation – if VIN1 falls below the user programmed limit, all channels are shut down. The VIN1 pin needs to be tied to VIN2 on the board with a short trace.
VIN2	38	If the Vin2 pin voltage falls below the user programmed UVLO VIN2 level all channels are shut down. The VIN2 pin needs to be tied to VIN1 on the board with a short trace.
VCCA	37	Output of the internal 5V LDO. This voltage is internally used to power analog blocks. This pin should be bypassed with a minimum of 4.7uF to AGND.
VCCD	26	Gate Drive input voltage. This is not an output voltage. This pin can be connected to VCCA to provide power for the Gate Drive. VCCD should be connected to VCCA with the shortest possible trace and decouple with a minimum 1µF capacitor. Alternatively, VCCD could be connected to an external supply (not greater than 5V).
GL_RTN1 - GL_RTN4	36,31,16,21	GL return connection. Ground connection for the low side gate driver. Connect at low side FET source. Connecting to the ground plane at the chip will inject noise into the local ground resulting in potential I^2C communications problems and PWM jitter.
AVDD	1	Output of the internal 1.8V LDO. A decoupling capacitor should be placed between AVDD and AGND close to the chip (with short traces).
DVDD	2	Input for powering the internal digital logic. This pin should be connected to AVDD.

Name	Pin Number	Description
DGND	10	Digital Ground. This pin should be connected to the ground plane at the exposed pad with a separate trace.
AGND	11	Analog Ground. This pin should be connected to the ground plane at the exposed pad with a separate trace
GL1-GL4	35,30,17,22	Output pin of the low side gate driver. Connect directly to the respective gate of an external N-channel MOSFET.
GH1-GH4	33,28,19,24	Output pin of the high side gate driver. Connect directly to the respective gate of an external N-channel MOSFET.
LX1-LX4	34,29,18,23	Lower supply rail for the high-side gate driver (GHx). Connect this pin to the switching node at the junction between the two external power MOSFETs and the inductor. These pins are also used to measure voltage drop across bottom MOSFETs in order to provide output current information to the control engine.
BST1-BST4	32,27,20,25	High side driver supply pin(s). Connect BST to an external boost diode and a capacitor as shown in the front page diagram. The high side driver is connected between the BST pin and LX pin.
GPIO0-GPIO3	3,4,5,6	These pins can be configured as inputs or outputs to implement custom flags, power good signals and enable/disable controls. A GPIO pin can also be programmed as an input clock synchronizing IC to external clock. Refer to the "GPIO Pins" Section and the "External Clock Synchronization" Section for more information.
GPIO4_SDA, GPIO5_SCL	7,8	I^2C serial interface communication pins. These pins can be re-programmed to perform GPIO functions in applications when I^2C bus is not used.
VOUT1-VOUT4	12,13,14,15	Voltage sense. Connect to the output of the corresponding power stage.
LDOOUT	40	Output of the Standby LDO. It can be configured as a 5V or 3.3V output. A compensation capacitor should be used on this pin [see Application Note].
ENABLE	9	If ENABLE is pulled high, the chip powers up (logic reset, registers configuration loaded, etc.). If pulled low for longer than 100us, the XRP7740 is placed into shutdown. See applications section for proper sequencing of this pin.
AGND	Exposed Pad	Analog Ground. Connect to analog ground (as noted above for pin 11).

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ORDERING INFORMATION(1)

Part Number	Junction Temp Range	Package	Packing Method	Lead-Free(2)	Default I^2C Address
XRP7740ILB- F	-40°C ≤ T_J ≤ +125°C	40-pin TQFN	Bulk	Yes	
XRP7740ILB-0X18-F	-40°C ≤ T_J ≤ +125°C	40-pin TQFN	Bulk	Yes	0X18
XRP7740EVB-HC	XRP7740 High Current Demo Board				
XR77EVB-XCM-V80	Configuration Module				

NOTES:

1. Refer to www.maxlinear.com/XRP7740 for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at T_J = T_A = 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

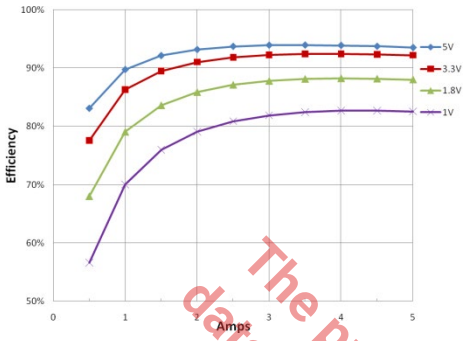


Fig. 4: 12Vin Efficiency: Single Channel
300kHz - Channels not in use are disabled
FET: Si4944; Inductor: 744314xxx 7x7x5mm

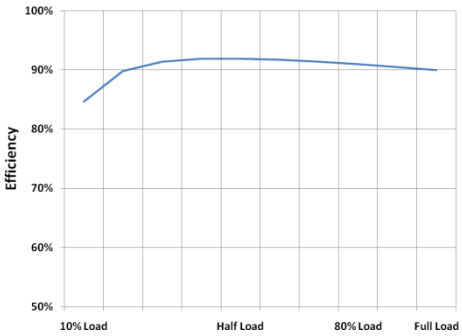


Fig. 5: 12Vin Combined Efficiency, 5V & 3V3 @ 5A, 1V8 & 1V @ 8A, 5V & 3V3 - FET: FDS8984; Inductor: 744314490 7x7x5mm 1V8 & 1V - FETs: SiR466 upper, SiR464 lower; Inductor: 7443551130 13x13x6.5mm

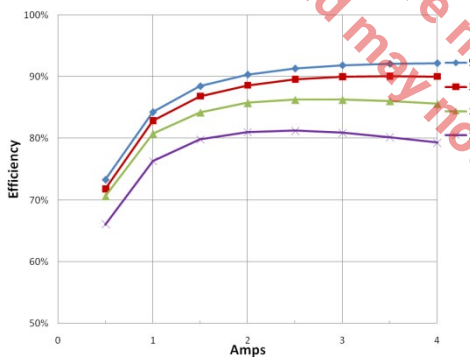


Fig. 6: 12Vin Efficiency: Single Channel
300kHz - Channels not in use are disabled
FET: FDS8984; Inductor:744310200 7x7x3mm

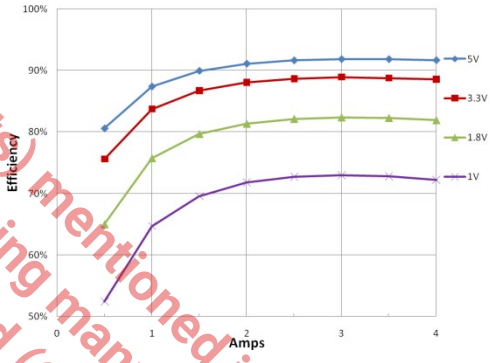


Fig. 7: 12Vin Efficiency: Single Channel
1MHz - Channels not in use are disabled
FET: FDS8984; Inductor:744310200 7x7x3mm

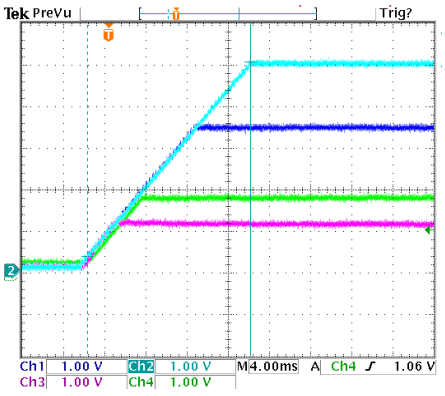


Fig. 8: Simultaneous Start-up Configuration
CH1:3.3V CH2:5V CH3:1V CH4:1.8V

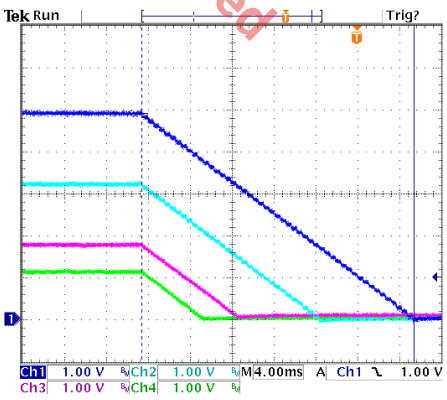


Fig. 9: Simultaneous Soft-Stop
CH1:3.3V CH2:5V CH3:1V CH4:1.8V

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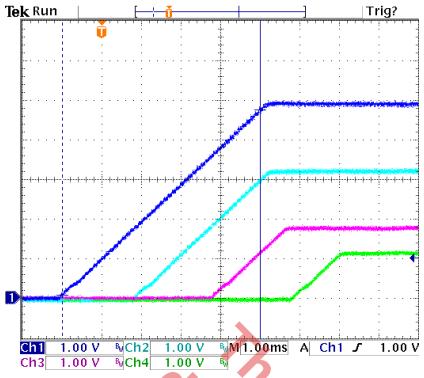


Fig. 10: Sequential Start-up Configuration
CH1:3.3V CH2:5V CH3:1V CH4:1.8V

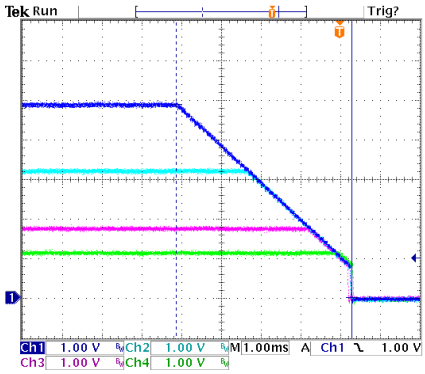


Fig. 11: Sequential Soft-Stop Configuration
CH1:5V CH2:3.3V CH3:1.8V CH4:1.2V
Vout Shutdown = 0.8V, 3A load

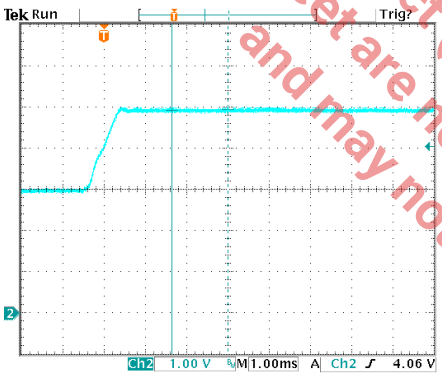


Fig. 12: Startup into 3V prebias – 5V Output
CH1: Vout(5V)

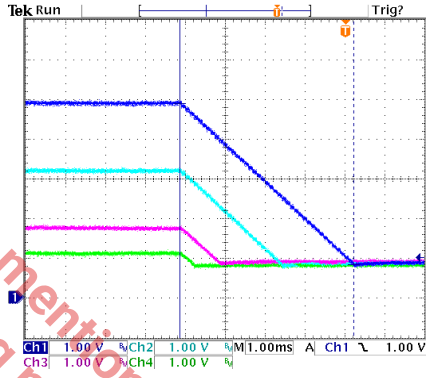


Fig. 13: Sequential Soft-Stop Configuration
Vout Shutdown = 0.8V, No Load
CH1:3.3V CH2:5V CH3:1V CH4:1.8V

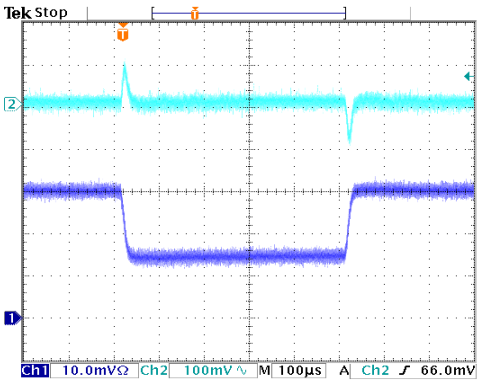


Fig. 14: Load Transient Response
CH1:Iout (1A/div) CH2: Vout (3.3V)

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

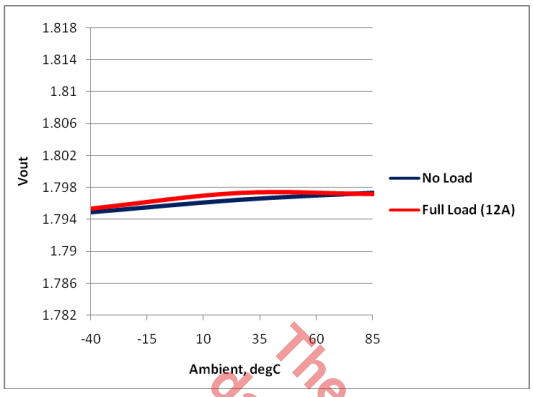


Fig. 15: XRP7740 Temperature Regulation
1.8V out (+/- 1% Vo window)

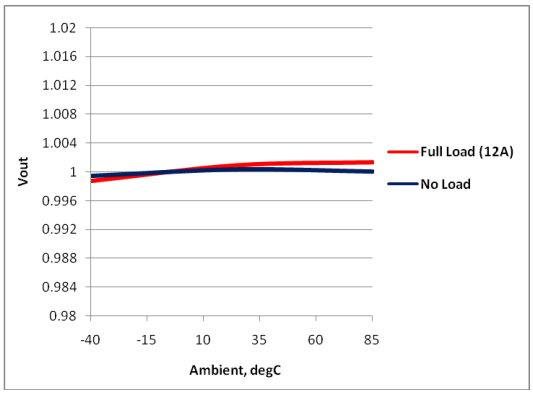


Fig. 16: XRP7740 Temperature Regulation
1.0V out (+/- 1% Vo window)

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FEATURES AND BENEFITS

General DPWM Benefits:

- Eliminate temperature and time variations associated with passive components in:
  - Output set point
  - Feedback compensation
  - Frequency set point
  - Under voltage lock out
  - Input voltage measurement
  - Gate drive dead time
- Tighter parameter tolerances including operating frequency set point
- Easy configuration and reconfiguration for different Vout, Iout, Cout, and Inductor selection by simply changing internal PID coefficients. No need to change external passives for a new output specification.
- Higher integration: Many external circuits can be handled by monitoring or modifying internal registers
- Selectable DPWM frequency and Controller Clock Frequency

Other Benefits:

- A single voltage is needed for regulation [no External LDO required].
- I^2C interface allows:
  - Communication with a System Controller or other Power Management devices for optimized system function
  - Access to modify or read internal registers that control or monitor:
    - Output Current
    - Input and Output Voltage
    - Soft-Start/Soft-Stop Time
    - 'Power Good'
    - Part Temperature
    - Enable/Disable Outputs
    - Over Current
    - Over Voltage
    - Temperature Faults
    - Adjusting fault limits and disabling/enabling faults
- 6 Configurable GPIO pins, (4 if I^2C is in use). Pins can be configured in several ways:
  - Fault reporting (including OCP, OVP, Temperature, Soft-Start in progress, Power Good)
  - Allows a Logic Level interface with other non-digital IC's or as logic inputs to other devices
  - Possible to configure as traditional 'enable' pin for all 4 outputs
  - 2 GPIOs can be dedicated to the I^2C Interface as required by the customers design
- Frequency and Synchronization Capability
  - Selectable switching frequency between 300kHz and 1.5MHz
  - Each output can be programmed to any one of 4 possible phases
  - Both internal clock and DPWM clock can be synchronized to external sources
  - 'Master', 'Slave' and 'Stand-alone' Configurations are possible
- Internal MOSFET Drivers
  - Internal FET drivers for each Channel: 3Ω/1.8Ω
  - Built-In Automatic Dead-time adjustment
  - 30ns Rise and Fall times
  - Soft-start into a pre-biased load and Soft-stop with programmable endpoint voltage
- PowerArchitect™ Design and Configuration Software:
  - In its simplest form only VIN, VOUT, and Iout for each channel is required.
  - The software calculates configuration register content based upon customer requirements. PID coefficients for correct loop response (for automatic or customized designs) can be generated and sent to the device.
  - Configurations can be saved and/or recalled
  - GPIOs can be configured easily and intuitively
  - Synchronization configuration can be adjusted
  - Interface can be used for real-time debugging and optimization
- Customizing XRP7740 with customer parameters
  - Once a configuration is finalized it can be sent to MaxLinear and can reside in pre-programmed parts that customers can order with an individual part number.
  - Allows parts to be used without I^2C interface

System Benefits:

- Reliability is enhanced via communication with the system controller which can obtain real time data on an output voltage, input voltage and current.
- System processors can communicate with the XRP7740 directly to obtain data or make adjustments to react to circuit conditions
- A system process or could also be configured to log and analyze operating history, perform diagnostics and if required, take the supply off-line after making other system adjustments.
- If customer field service is a possibility for your end product, parameter reporting and history would provide additional capabilities for troubleshooting or aid in future system upgrades.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FUNCTIONAL DESCRIPTION AND OPERATION

The XRP7740 is a quad-output digital pulse width modulation (DPWM) controllers with integrated gate drivers for the use in synchronous buck switching regulators. Each output voltage can be programmed from 0.9V to 5.1V without the need of an external voltage divider. The wide range of the programmable DPWM switching frequency (from 300 kHz to 1.5 MHz) enables the user to optimize for efficiency or component sizes. The digital regulation loop requires no external passive components for network compensation. The loop performance does not need to be compromised due to component tolerance, aging, and operating condition. Each digital controller provides a number of safety features, such as over-current protection (OCP) and over-voltage protection (OVP). The chip also provides over-temperature protection (OTP) and under-voltage lock-out (UVLO) for two input voltage rails. The XRP7740 also has up to 6 GPIOs and a Standby Linear Regulator to provide standby power. An I^2C bus interface is provided to program the IC as well as to communicate with the host for fault reporting and handling, power rail monitoring, channel enable and disable, Standby Low Drop-out Regulator voltage reconfiguration, and Standby LDO enable and disable.

The XRP7740 offers a complete solution for soft-start and soft-stop. The delay and ramp of each PWM regulator can be independently controlled. When a pre-bias voltage is present, the device holds both high-side and low-side MOSFETs off until the reference voltage ramps up higher than the output voltage. As a result, large negative inductor current and output voltage disturbance are avoided. During soft-stop, the output voltage ramps down with a programmable slope until it reaches a pre-set stop voltage. This pre-set value can be programmed between within zero volts and the target voltage with the same set target voltage resolution (see shutdown waveforms in Applications).

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REGISTER TYPES

There are two types of registers in the XRP7740: read/write registers and read-only registers. The read/write registers are used for the control functions of the IC and can be programmed using configuration non-volatile memory (NVM) or through an I^2C command. The read-only registers are for feedback functions such as error/warning flags and for reading the output voltage or current.

NON-VOLATILE CONFIGURATION MEMORY

The non-volatile memory (NVM) in XRP7740 stores the configuration data for the chip and all of the power rails. This memory is normally configured during manufacturing time. Once a specific bit of the NVM is programmed, that bit can never be reprogrammed again [i.e. one-time programmable]. During chip power up, the contents in the NVM are automatically transferred to the internal registers of the chip. Programmed cells have been verified to be permanent for at least 10 years and are highly reliable.

POWER UP AND SEQUENCING REQUIREMENTS

The XRP7740 can be programmed to sequence its outputs for nearly any imaginable loading requirement. However, there are some important sequencing requirements for the XRP7740 itself.

When power is applied to the XRP7740, the 5V VCCA and 1.8V AVDD regulators must come up and stabilize to provide power for the analog and digital blocks of the IC. The Enable Pin must remain below its logic level high threshold until the AVDD is regulating to ensure proper loading of the configuration registers. For systems that control the Enable signal through a microcontroller or other processor, this is simply a matter of providing the proper delay to the Enable signal after power up. However, most users will want the part to automatically power up when power is applied to the system. To that end there are a number of recommended solutions.

The most ideal sequencing method is to provide an RC time constant delay from DVDD to the Enable pin. A 10kohm resistor and a 0.1uF are all that is required. If the system needs to externally control the Enable pin as well, it is recommended that the Enable pin be pulled to ground using an open drain I/O. Using 3.3V active logic would back feed DVDD and exceed the maximum rated voltage of the pin.

For those using active 3.3V or 5V logic on the Enable pin an RC delay from VCCA to the Enable pin may be used. When using an RC delay from VCCA, attention must be paid to the amount of bypass capacitance loading AVDD since it will delay the time it takes for AVDD to power up and regulate. The AVDD and DVDD pins do not require more than 2.2uF for proper bypassing. See Figure 17 for the recommended components for sequencing the Enable pin through an RC delay from VCCA. If more capacitance is added to AVDD and DVDD, the time constant must be increased. Once Enable is asserted, an internal CHIP_READY flag goes high and enables the I^2C to acknowledge the Host's serial commands. Channels that are configured as always-on channels are enabled. Channels that are configured to be enabled by GPIOs are also enabled if the respective GPIO is asserted.

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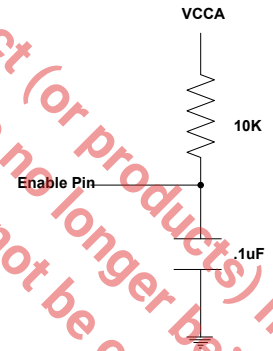


Fig. 17: RC Delay for Enable taken from VCCA

In almost all cases, a simple check will ensure proper sequencing has been achieved. VCCA regulates at approximately 4.6V when the Enable pin is logic level low and at 5.1V when Enable is asserted. VCCA will typically power up and regulate before AVDD and because the internal logic is not yet powered up there is no internal shutdown signal, it will regulate at 5.1V. Once AVDD has reached sufficient voltage (and Enable is low) it will assert the internal shutdown signal and VCCA will reduce its regulated voltage to 4.6V. When the Enable is asserted, the chip will power up and VCCA will regulate at 5.1V. If our device is sequenced properly, VCCA will achieve 5.1V then drop down to 4.6V and toggle back to 5.1V. See Figure 18 for an example.

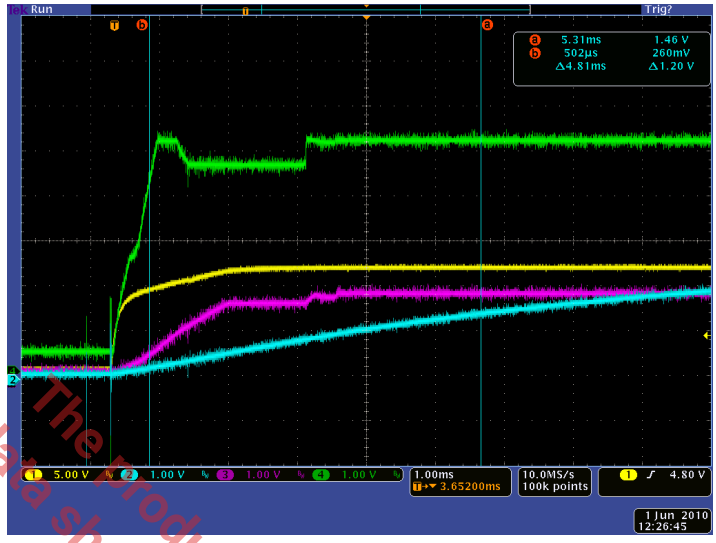


Fig. 18: VCCA (green) Startup Waveform

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STANDBY LOW DROP-OUT REGULATOR

This 100mA low drop-out regulator can be programmed as 3.3V or 5V in SET_STBLDO_EN_CONFIG register. Its output is seen on the LDOOUT Pin. This LDO is fully controllable via the Enable Pin (configured to turn on as soon as power is applied), a GPIO, and/or I^2C communication.

The standby LDO should be bypassed with a minimum of 2.2uF ceramic capacitor.

ENABLING, DISABLING AND RESET

The XRP7740 is enabled via raising the ENABLE Pin high. The chip can then be disabled by lowering the same ENABLE Pin. There is also the capability for resetting the Chip via an I^2C SOFTRESET Command.

For enabling a specific channel, there are several ways that this can be achieved. The chip can be configured to enable a channel at start-up as the default configuration residing in the non-volatile configuration memory of the IC. The channels can also be enabled using GPIO pins and/or an I^2C Bus serial command. The registers that control the channel enable functions are the SET_EN_CONFIG and SET_CH_EN_I2C.

INTERNAL GATE DRIVERS

The XRP7740 integrates Internal Gate Drivers for all 4 PWM channels. These drivers are optimized to drive both high-side and low side N-MOSFETs for synchronous operation. Both high side and low side drivers have the capability of driving 1 nF load with 30 ns rise and fall time. The drivers have built-in non-overlapping circuitry to prevent simultaneous conduction of the two MOSFETs.

FAULT HANDLING

While the chip is operating there are four different types of fault handling:

- **Under Voltage Lockout (UVLO)** monitors the input voltage to the chip, and the chip will shutdown all channels if the voltage drops to critical levels.
- **Over Temperature Protection (OTP)** monitors the temperature of the chip, and the chip will shutdown all channels if the temperature rises to critical levels.
- **Over Voltage Protection (OVP)** monitors the voltage of channel and will shutdown the channel if it surpasses its voltage threshold.

- **Over Current Protection (OCP)** monitors the current of a channel, and will shutdown the channel if it surpasses its current threshold. The channel will be automatically restarted after a 200ms delay.

Under Voltage Lockout (UVLO)

There are two locations where the under voltage can be sensed: VIN1 and VIN2. The **SET_UVLO_WARN_VINx** register that sets the under voltage warning set point condition at 100mV increments. When the warning threshold is reached, the Host is informed via a GPIO or by reading the **READ_WARN_FLAG** register.

The **SET_UVLO_TARG_VINx** register that controls the under voltage fault set point condition at 100mV increments. This fault condition will be indicated in the **READ_FAULT_WARN** register.

When an under voltage fault condition occurs (either on VIN1 or VIN2), the fault flag register is set and all of the XRP7740 outputs are shut down. The measured input voltages can be read back using the **READ_VIN1** or **READ_VIN2** register, and both registers have a resolution of 100mV per LSB. When the UVLO condition clears (voltage rises above the UVLO Warning Threshold), the chip can be configured to automatically restart.

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VIN1

This is a multi-function pin that provides power to both the Standby Linear Regulator and internal linear regulators to generate VCCA, VDD, and the Standby LDO (LDOUT).

It is also used as a UVLO detection pin. If Vin1 falls below its user programmed limit, all channels are shut down.

VIN2

VIN2 is required to be tied to VIN1 pin. It can be used as a UVLO detection pin. If VIN2 falls below its user programmed limit, all channels are shut down.

Temperature Monitoring and Over Temperature Protection (OTP)

- Reading the junction temperature

This register allows the user to read back the temperature of the IC. The temperature is expressed in Kelvin with a maximum range of 520K, a minimum of 200K, and an LSB of 5 degrees K. The temperature can be accessed by reading the READ_VTJ register.

- Over Temperature Warning

There are also warning and fault flags that get set in the READ_OVV_UVLO_OVT_FLAG register. The warning threshold is configurable to 5 or 10 Degrees C below the fault threshold. When the junction temperature reaches 5 or 10 Degrees C below the user defined set point, the over-temperature warning bit [*OTPW*] gets set in the READ_OVV_UVLO_OVT_FLAG register to warn the user that the IC might go into an over temperature condition (and shutdown all of the regulators).

- Over Temperature Fault

If the over temperature condition occurs both the *OTP* and *OTPW* bits will be set in the READ_OVV_UVLO_OVT_FLAG register and the IC will shut down all channels (but I^2C will remain operational). The actual over temperature threshold can be set by the user by using a 7bit SET_THERMAL_SHDN register with an LSB of 5K.

If the over temperature fault condition clears, then the IC can be set to restart the chip automatically. The restart temperature threshold can be set by the SET_THERMAL_RESTART register.

OUTPUT VOLTAGE SETTING AND MONITORING

The Output Voltage setting is controlled by the SET_VOUT_TARGET_CHx register. This register allows the user to set the output voltage with a resolution of 50mV for output voltages between 0 and 2.5V and with a resolution of 100mV for output voltages between 2.6V and 5.1V. Output voltages higher than 5.1V can be achieved by adding an external voltage divider network. The output voltage of a particular channel can be read back using the READ_VOUTx register.

Output Voltage from 0.9V to 5.1V

Per the equation below, for values between 0.9V and 5.1V the output voltage is equal to the binary number stored in the SET_VOUT_TARGET_CHx register multiplied by 50mV. When programming an output voltage from 2.6V to 5.1V, odd binary values should be avoided. As a result, the set resolution for an output voltage higher than 2.5V is 100mV.

$$V_{OUT} = SET_VOUT_TARGET_CHX \times 50mV$$

Output VOUT Higher Than 5.1V

To set the output voltage higher than 5.1V, the user needs to add an external voltage divider. The resistors used in the voltage divider should be below 10kΩ. The SET_VOUT_TARGET_CHx register should be set to 0x32 which is equivalent to an output voltage of 2.5V without the external divider network. The output voltage regulation in this case might exceed 2% due to extra error from the resistor divider. *R*1 and *R*2 follows the definition below.

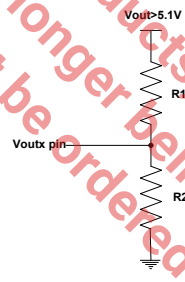


Fig.19: External divider network for high output voltage

$$V_{OUT} = \left(\frac{R_1}{R_2} + 1\right) \times SET_VOUT_TARGET_CHX \times 50mV$$

Output Voltage Lower Than 0.9V

The XRP7740 can be programmed to regulate an output voltage lower than 0.9V. However, in this case the specification of +-2% output voltage accuracy may be exceeded.

OVER-VOLTAGE PROTECTION (OVP)

The Over-Voltage Protection (OVP) SET_OVVP_REGISTER sets the over-voltage condition in predefined steps per channel. The over-voltage protection is always active even during soft-start condition. When the over-voltage condition is tripped, the controller will shut down the channel. When the channel is shut down the controller will then set corresponding OVP Fault bits in the READ_OVV_UVLO_OVT_FLAG register.

The VOUT OVP Threshold is 150mV to 300mV above nominal VOUT for a Voltage Target of 2.5V or less. For the Voltage Target of 2.6V to 5.1V, the VOUT OVP Threshold is 300mV to 600mV.

Once the over-voltage Channel is disabled, the controller will check the SET_FAULT_RESP_CONFIG_LB and SET_FAULT_RESP_CONFIG_HB to determine whether there are any "following" channels that need to be shut down. Any following channel will be disabled when

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the channel with the Over Voltage Fault is disabled. The channel(s) will remain disabled, until the Host takes action to enable the channel(s).

Any of the fault and warning conditions can also be configured to be represented using the general purpose input output pins (GPIO) to use as an interface with non I^2C compatible devices. For further information on this topic see the "GPIO Pins" Section.

During OVP fault shutdown of the channel, the customer has the option to choose two types of shutdown for each channel. The first shutdown is 'passive shutdown' where the IC merely stops outputting pulses. The second shutdown is a 'brute force' shutdown where the GL remains on as the channel reaches its discharged voltage. Note that if the 'brute force' method is chosen, then GL will permanently remain high until the channel is re-enabled.

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OUTPUT CURRENT SETTING AND MONITORING

XRP7740 utilizes a low side MOSFET Rdson current sensing technique. The voltage drop on Rdson is measured by dedicated current ADC. The ADC results are compared to a maximum current threshold and an over-current warning threshold to generate the fault and warning flags.

Maximum Output Current

The maximum output current is set by the SET_VIOUT_MAX_CHx register and SET_ISENSE_PARAM_CHx register. The SET_VIOUT_MAX_CHx register is an 8 bit register. Bits [5:0] set the maximum current threshold and bits [7:6] set the over-current warning threshold. The LSB for the current limit register is 5 mV and the allowed voltage range is between 0 and 315mV. To calculate the maximum current limit, the user needs to provide the MOSFET Rdson. The maximum current can be calculated as:

$$IOUTMAX = \frac{Vsense}{Rdson \times Kt}$$

Where Kt is the temperature coefficient of the MOSFET Rdson; Vsense is the voltage across Rdson; IOUTMAX is the maximum output current.

Over-Current Warning

The XRP7740 also offers an Over-Current warning flag. This warning flag resides in the READ_OVC_FLAG register. The warning flag bit will be set when the output current gets to within a specified value of the output current limit threshold enabling the host to reduce power consumption. The SET_VIOUT_MAX_CHx register allows the warning flag threshold to be set 10mV, 20mV, 30mV or 40mV below VIOUT_MAX. The warning flag will be automatically cleared when the current drops below the warning threshold.

Over-Current Fault Handling

When an over-current condition occurs, PWM drivers in the corresponding channels are disabled. After a 200ms timeout, the controller is re-powered and soft-start is initiated. When the over-current condition is reached the controller will check the SET_FAULT_RESP_CONFIG_LB and SET_FAULT_RESP_CONFIG_HB to determine whether there are any "following" channels that need to be similarly restarted. The controller will also set the fault flags in READ_OVC_FAULT_WARN register.

Typically the over-current fault threshold would be set to 130-140% of the maximum desirable output current. This will help avoid any over-current conditions caused by transients that would shut down the output channel.

CHIP OPERATION AND CONFIGURATION

SOFT-START

The SET_SS_RISE_CHx register is a 16 bit register which specifies the soft-start delay and the ramp characteristics for a specific channel. This register allows the customer to program the channel with a 250us step resolution and up to a maximum 16ms delay.

Bits [15:10] specify the delay after enabling a channel but before outputting pulses; where each bit represents 250us steps. Bits [9:0] specify the rise time of the channel; these 10 bits define the number of microseconds for each 50mV increment to reach the target voltage. The status of the soft-start operation is indicated in the POWER_GOOD_SOFT_START_FLAG register by bits [3:0] which correspond to channels 4 though 1 respectively. A value of 1 signifies that a soft start is in operation on a given channel.

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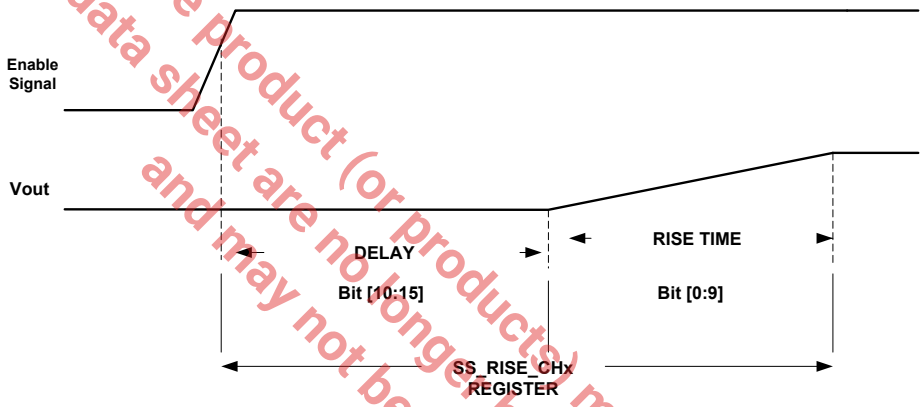


Fig. 20: Channel Power Up Sequence

SOFT-STOP

The SET_PD_FALL_CHx register is a 16 bit register. This register specifies the soft-stop delay and ramp (fall-time) characteristics for when the chip receives a channel disable indication from the Host to shutdown the channel.

Bits [15:10] specify the delay after disabling a channel but before starting the shutdown of the channel; where each bit represents 250us steps. Bits [9:0] specify the fall time of the channel; these 10 bits define the number of microseconds for each 50mV increment to reach the discharge threshold.

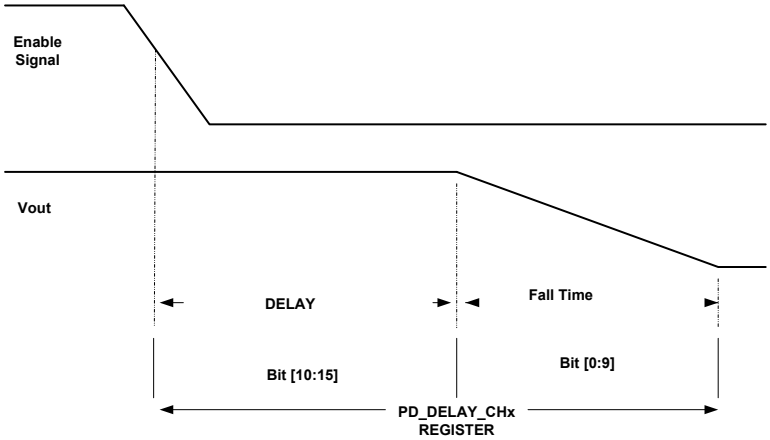


Fig. 21: Channel Soft-Stop Sequence

POWER GOOD FLAG

The XRP7740 allows the user to set the upper and lower bound for a power good signal per channel. The SET_PWRG_TARG_MAX_CHx register sets the upper bound, the SET_PWRG_TARG_MIN_CHx register sets the lower bound. Each register has a 20mV LSB resolution. When the output voltage is within bounds the power good signal is asserted high. Typically the upper bound should be lower than the over-voltage threshold. In addition, the power good signal can be delayed by a programmable amount set in the SET_PWRGD_DLY_CHx register. The power good delay is only set after the soft-start period is finished. If the channel has a pre-charged condition that falls into the power good region, a power good flag is not set until the soft-start is finished.

PWM SWITCHING FREQUENCY

The PWM switching frequency is set by choosing the corresponding oscillator frequency and clock divider ratio in the SET_SW_FREQUENCY register. Bits [6:4] set the oscillator frequency and bits [2:0] set the clock divider. The tables below summarize the available Main Oscillator and PWM switching frequency settings in the XRP7740.

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Main Oscillator Frequency

SET_SW_FREQUENCY[6:4]	000	001	010	011	100	101	110	111
Main Oscillator Frequency	48MHz	44.8MHz	41.6MHz	38.4MHz	35.2MHz	32MHz	28.8Mhz	25.6MHz
Ts	20.8ns	22.3ns	24ns	26ns	28.4ns	31.25ns	34.7ns	39ns

PWM Switching Frequency

	SET_SW_FREQUENCY[6:4]							
SET_SW_FREQUENCY[2:0]	000	001	010	011	100	101	110	111
000	NA	NA	NA	NA	NA	NA	NA	NA
001	1.5MHz	1.4MHz	1.3MHz	1.2MHz	1.1MHz	1.0MHz	900KHz	800KHz
010	1.0MHz	933KHz	867KHz	800KHz	733KHz	667KHz	600KHz	533KHz
011	750KHz	700KHz	650KHz	600KHz	550KHz	500KHz	450KHz	400KHz
100	600KHZ	560KHz	520KHz	480KHz	440KHz	400KHz	360KHz	320KHz
101	500KHz	467KHZ	433KHz	400KHz	367KHz	333KHz	300KHz	NA
110	429KHZ	400KHZ	370KHz	343KHz	314KHz	NA	NA	NA
111	375KHz	350KHz	325KHz	300KHz	NA	NA	NA	NA

There are a number of options that could result in similar PWM switching frequency as shown above. In general, the chip consumes less power at lower oscillator frequency. When synchronization to external clock is needed, the user can choose the oscillator frequency to be within ±5% of the external clock frequency. A higher Main Oscillator frequency will not improve accuracy or any performance efficiency.

PWM SWITCHING FREQUENCY CONSIDERATIONS

There are several considerations when choosing the PWM switching frequency.

Minimum On Time

Minimum on time determines the minimum duty cycle at the specific switching frequency. The minimum on time for the XRP7740 is 40ns.

$$Minimum\ Duty\ Cycle\% = Minimum\ ontime \times PWM\ Frequency \times 100$$

As an example the minimum duty cycle is 4% for 1MHz PWM frequency. This is important since the minimum on time dictates the maximum conversion ratio that the PWM controller can achieve.

$$Minimum\ Duty\ Cycle\% > \frac{Vout}{Vinmax}$$

Maximum Duty Cycle

The maximum duty cycle is dictated by the minimum required time to sample the current when the low side MOSFET is on. For the XRP7740, the minimum required sampling time is about 16 clock cycles at the main oscillator frequency. When calculating maximum duty cycle, the sampling time needs to be subtracted using the below equation. For example, if operating at 1MHz using the 32MHz main oscillator frequency, the maximum duty cycle would be:

$$Maximum\ Duty\ Cycle\% = \left(1 - \left(\frac{16}{clock\ frequency} \times PWM\ frequency - 0.03\right)\right) \times 100 \approx 47\%$$

On the other hand, if the 48MHz main oscillator frequency was chosen for the 1MHz PWM frequency, the maximum duty cycle would be:

$$Maximum\ Duty\ Cycle\% = \left(1 - \left(\frac{16}{clock\ frequency} \times PWM\ frequency - 0.03\right)\right) \times 100 \approx 64\%$$

Therefore, it is best to choose the highest main oscillator frequency for a particular PWM frequency if duty cycle limit might be encountered. The maximum duty cycle for any PWM frequency can easily be determined using the following table:

	Main Oscillator Frequency							
Maximum Duty Cycle	48MHz	44.8MHz	41.6MHz	38.4MHz	35.2MHz	32MHz	28.8Mhz	25.6MHz
47%	1.5MHz	1.4MHz	1.3MHz	1.2MHz	1.1MHz	1.0MHz	900KHz	800KHz
64%	1.0MHz	933KHz	867KHz	800KHz	733KHz	667KHz	600KHz	533KHz
72%	750KHz	700KHz	650KHz	600KHz	550KHz	500KHz	450KHz	400KHz
77%	600KHZ	560KHz	520KHz	480KHz	440KHz	400KHz	360KHz	320KHz
80%	500KHz	467KHZ	433KHz	400KHz	367KHz	333KHz	300KHz	NA
83%	429KHZ	400KHZ	370KHz	343KHz	314KHz	NA	NA	NA
85%	375KHz	350KHz	325KHz	300KHz	NA	NA	NA	NA

Fig. 22: PWM Frequency

It is highly recommended that the maximum duty cycle obtained from the table above be programmed into each of the channels using the SET_DUTY_LIMITER_CHx register. This ensures that under all conditions (including faults), there will always be sufficient sampling time to measure the output current. When the duty cycle limit is reached, the output voltage will no longer regulate and will be clamped based on the maximum duty cycle limit setting.

Efficiency

The PWM Switching frequency plays an important role on overall power conversion efficiency. As the switching frequency increase, the switching losses also increase. Please see the APPLICATION INFORMATION, Typical Performance Data for further examples.

Component Selection and Frequency

Typically the components become smaller as the frequency increases, as long as the ripple requirements remain constant. At higher frequency the inductor can be smaller in value and have a smaller footprint while still maintaining the same current rating.

FREQUENCY SYNCHRONIZATION FUNCTION AND EXTERNAL CLOCK

The user of the XRP7740 can choose to use an external source as the primary clock for the XRP7740. This function can be configured using the SET_SYNC_MODE_CONFIG register. This

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register sets the operation of the XRP7740 when an external clock is required. By selecting the appropriate bit combination the user can configure the IC to function as a master or a slave when two or more XRP7740s are used to convert power in a system. Automatic clock selection is also provided to allow operation even if the external clock fails by switching the IC back to an internal clock.

External Clock Synchronization

Even when configured to use an external clock, the chip initially powers up with its internal clock. The user can set the percent target that the frequency detector will use when comparing the internal clock with the clock frequency input on the GPIO pin. If the external clock frequency is detected to be within the window specified by the user, then a switchover will occur to the external clock. If the IC does not find a clock in the specified frequency target range then the external clock will not be used and the IC will run on the internal clock that was specified by the user. If the external clock fails the user can chose to have the internal clock take over, using the automatic switch back mode in the SET_SYNC_MODE_CONFIG register.

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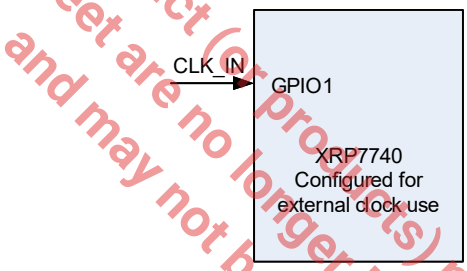


Fig. 23: XRP7740 Configured For External Clock Use

Synchronized Operation as a Master and Slave Unit

Two XRP7740s can be synchronized together. This Master-Slave configuration is described below.

- Master

When the XRP7740 powers up as a master unit after the internal configuration memory is loaded the unit will send CLK_OUT and SYNC_OUT signals to the slave on the preconfigured GPIO pins.

- Slave

When powering in sync mode the slave unit will initially power up with its internal clock to transfer the configuration memory. Once this transfer occurs, then the unit is set to function as a slave unit. In turn the unit will take the external clock provided by the master to run as its main internal clock.

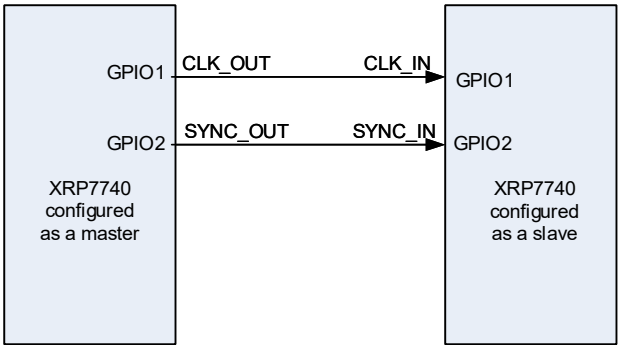


Fig. 24: Master/Slave Configuration of the XRP7740

External Clock Synchronization Master Slave combination

When an external clock is used, the user will need to setup the master to also have an external clock in function. All of the same rules apply as in the External clock synchronization, Synchronized operation as a Slave unit section of this document. There are two ways of synchronizing this, either the external clock going to both Master/Slave CLK_IN, or CLK_IN can go to the Master, and the Master can synchronize SYNC_OUT and CLK_OUT to the Slave.

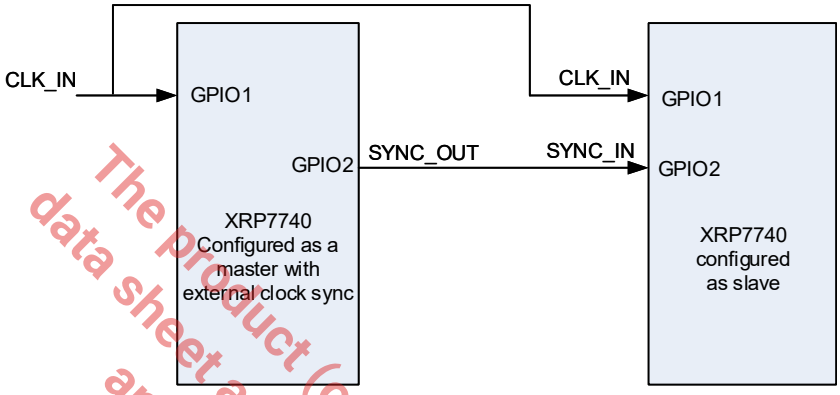


Fig. 25: External Clock Synchronization Master Slave Combination

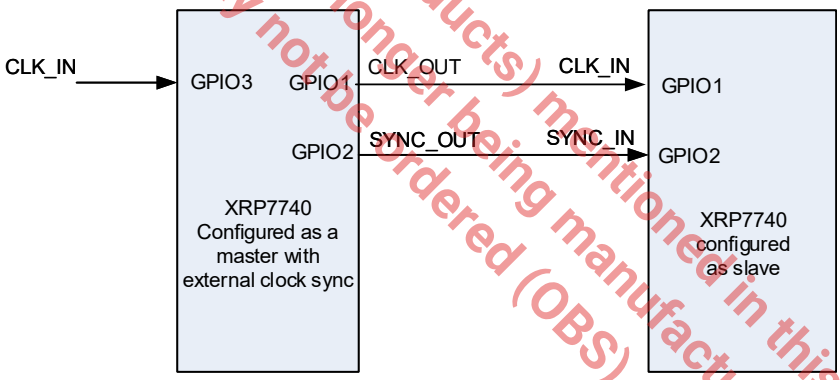


Fig. 26: Alternative External clock synchronization Master Slave combination

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PHASE SHIFT

Each switching channel can be programmed to a phase shift of the multiples of 90 degrees [for a 4 phase configuration] or 120 degrees [for a 3 phase configuration]. Two or more of the channels can use the same phase shift, however, it is preferable to run each channel at separate phases.

GPIO PINS

The General Purpose Input Output (GPIO) Pins are the basic interface between the XRP7740 and the system. Although all of the stored data within the IC can be read back using the I^2C bus it is sometimes convenient to have some of those internal register to be displayed and or controlled by a single data pin. Besides simple input output functions the GPIO pins can be configured to serve as external clock inputs. These pins can be programmed using OTP bits or can be programmed using the I^2C bus. This GPIO_CONFIG register allows the user close to 100 different configuration functions that the GPIO can be programmed to do.

NOTE: the GPIO Pins (and all I/Os) should NOT be driven without a 10K resistor when VIN is not being applied to the IC.

GPIO Pins Polarity

The polarity of the GPIO pin can be set by using the GPIO_ACT_POL register. This register allows any GPIO pin whether configured as an input or output to change polarity. Bits [5:0] are used to set the polarity of GPIO 0 though 5. If the IC operates in I²C mode, then the commands for Bits [5:4] are ignored.

Supply Rail Enable

Each GPIO can be configured to enable a specific power rail for the system. The GPIOx_CFG register allows a GPIO to enable/disable any of the following rails controlled by the chip:

- A single buck power controller
- The Standby LDO
- Any mix of the Standby LDO and power controller(s)

When the configured GPIO is asserted externally, the corresponding rails will be enabled, and they will be similarly disabled when the GPIO is de-asserted. This supply enabling/disabling can also be controlled through the I²C interface.

Power Good Indicator

The GPIO pins can be configured as Power Good indicators for one or more rails. The GPIO pin is asserted when all rails configured for this specific IO are within specified limits for regulation. This information can also be found in the READ_PWRGD_SS_FLAG status register.

Fault and Warning Indication

The GPIOs can be configured to signal Fault or Warning conditions when they occur in the chip. Each GPIO can be configured to signal one of the following:

- OCP Fault on Channel 1 - 4
- OCP Warning on Channel 1 - 4
- OVP Fault on Channel 1 - 4
- UVLO Fault on VIN1 or VIN2
- UVLO Warning on VIN1 or VIN2
- Over Temperature Fault or Warning

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I²C COMMUNICATION

The I²C communication is standard 2-wire communication available between the Host and the IC. This interface allows for the full control, monitoring, and reconfiguration of the semiconductor.

Each device in an I²C-bus system is activated by sending a valid address to the device. The address always has to be sent as the first byte after the start condition in the I²C -bus protocol

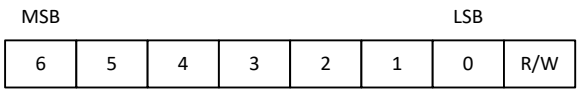


Fig. 27: Alignment of I²C address in 8 bit byte

There is one address byte required since 7-bit addresses are used. The last bit of the address byte is the read/write-bit and should always be set according to the required operation. This 7-bit I²C address is stored in the NVM. One can program a blank device with the 7-bit Slave address or select one of the preprogrammed options. The 7-bit address plus the R/W bit create an 8-bit data value that is sent on the bus.

The XRP7740ILB-0X18-F has an I²C address of 0x18. The internal registers are written by sending a data value of 0x30 and read by sending a data value of 0x31. This reflects the address being shifted one bit to the left and the least significant bit being set to reflect a read or write operation in order to stuff the byte correctly.

The second byte sent to the device is the location of a specific register.

Using GPIO3 to select I²C Address

GPIO3 may be used to change the LSB of the 7-bit address. This option can be enabled within the PowerArchitect™ software by checking the "Use GPIO3 to control LSB of I2C address" box at the top right of the "Digital Design" tab. More about the use of this option and other methods of changing the default I2C address of the part are available in ANP-31 "PowerXR Configuration and Programming".

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EXTERNAL COMPONENT SELECTION

Inductor Selection

Select the Inductor for inductance L and saturation current Isat. Select an inductor with Isat higher than the programmed over current limit. Calculate inductance from:

$$L = \frac{(Vin - Vout) \times Vout}{Vin} \times \frac{1}{fs} \times \frac{1}{Irip}$$

Where:

Vin is the converter input voltage

Vout is the converter output voltage

fs is the switching frequency

Irip is the inductor peak-to-peak current ripple (nominally set to 30% of Iout)

Keep in mind that a higher Irip results in a smaller inductance value which has the advantages of smaller size, lower DC equivalent resistance (DCR), and allows the use of a lower output capacitance to meet a given step load transient. A higher Irip, however, increases the output voltage ripple, requires higher saturation current limit, and increases critical conduction. Notice that this critical conduction current is half of Irip.

Capacitor Selection

- Output Capacitor Selection

Select the output capacitor for voltage rating, capacitance and Equivalent Series Resistance (ESR). Nominally the voltage rating is selected to be at least twice as large as the output voltage. Select the capacitance to satisfy the specification for output voltage overshoot/undershoot caused by the current step load. A sudden decrease in the load current forces the energy surplus in the inductor to be absorbed by Cout. This causes an overshoot in output voltage that is corrected by power switch reduced duty cycle. Use the following equation to calculate Cout:

$$C = L \times \frac{(I_2 - I_1)^2}{{V_{OS}}^2 - {V_{OUT}}^2}$$

Where:

L is the output inductance

I2 is the step load high current

I1 is the step load low current

Vos is output voltage including the overshoot

Vout is the steady state output voltage

Or it can be expressed approximately by

$$C = L \times \frac{(I_2 - I_1)^2}{2 \times Vout - \Delta V}$$

Here, $\Delta V = V_{os} - V_{out}$ is the overshoot voltage deviation.

Select ESR such that output voltage ripple (Vrip) specification is met. There are two components in Vrip. First component arises from the charge transferred to and from Cout during each cycle. The second component of Vrip is due to the inductor ripple current flowing through the output capacitor's ESR. It can be calculated for Vrip:

$$Vrip = Irip \times \sqrt{ESR^2 + \left(\frac{1}{8 \times Cout \times fs}\right)}$$

Where:

Irip is the inductor ripple current

fs is the switching frequency

Cout is the output capacitance

Note that a smaller inductor results in a higher Irip, therefore requiring a larger Cout and/or lower ESR in order to meet Vrip.

- Input Capacitor Selection

Select the input capacitor for Voltage, Capacitance, ripple current, ESR and ESL. Voltage rating is nominally selected to be at least twice the input voltage. The RMS value of input capacitor current, assuming a low inductor ripple current, can be approximated as:

$$Iin = Iout \times \sqrt{D \times (1 - D)}$$

Where:

Iin is the RMS input current

Iout is the DC output current

D is the duty cycle

In general, the total input voltage ripple should be kept below 1.5% of VIN. The input voltage ripple also has two major components: the voltage drop on the main capacitor ΔV_{Cin} and the voltage drop due to ESR - ΔV_{ESR}. The contribution to Input voltage ripple by each term can be calculated from:

$$\Delta V_{Cin} = \frac{I_{out} V_{out} (V_{in} - V_{out})}{f_s C_{in} V_{in}^2}$$

$$\Delta V_{ESR} = ESR \cdot (I_{out} + 0.5 I_{rip})$$

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Total input voltage ripple is the sum of the above:

$$\Delta V_{Tot} = \Delta V_{Cin} + \Delta V_{ESR}$$

Power MOSFETs Selection

Selecting MOSFETs with lower *Rdson* reduces conduction losses at the expense of increased switching losses. A simplified expression for conduction losses is given by:

$$P_{cond} = I_{out}^{\ 2} \cdot R_{dson} \cdot \frac{V_{out}}{V_{in}}$$

MOSFET's junction temperature can be estimated from:

$$T_j = 2P_{cond}R_{thja} + T_{ambient}$$

This assumes that the switching loss is the same as the conduction loss. R_{thja} is the total MOSFET thermal resistance from junction to ambient.

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LAYOUT GUIDELINES

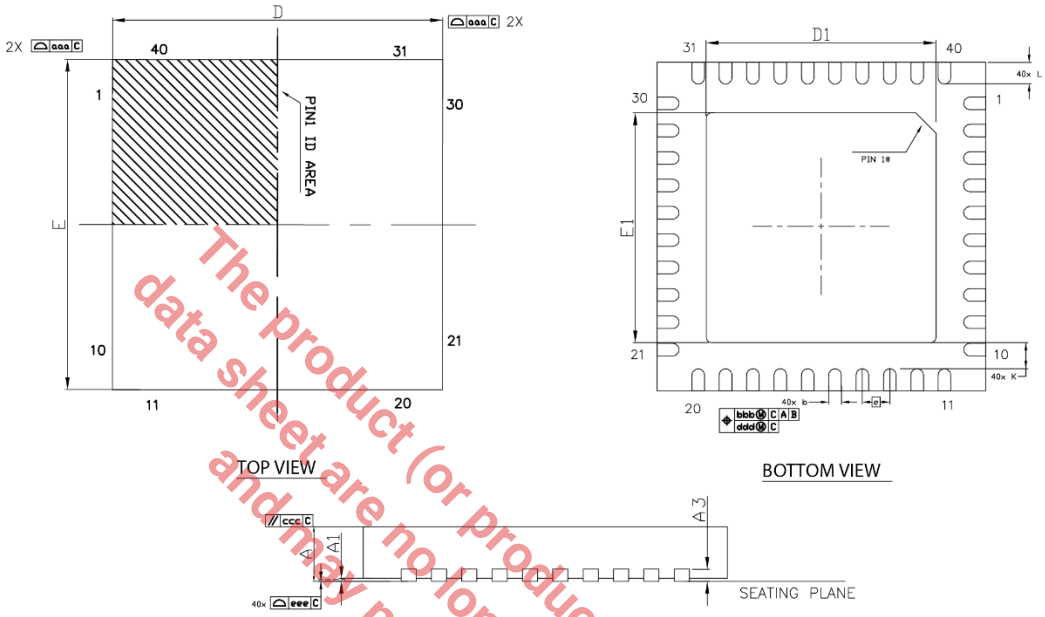
Refer to application note ANP-32 "Practical Layout Guidelines for Power^{XR} Designs" and ANP-35 "XRP77XX: Extending the MOSFET Gate Drive Conductors".

REGISTER MAP

See ANP-31 "PowerXR Configuration and Programming" for details of the register map and other programming information.

MECHANICAL DIMENSIONS

40-PIN 6mmX6mm TQFN



DIMENSION TABLE			
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	---	0.20Ref	---
b	0.20	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
D1	4.40	4.50	4.60
E1	4.40	4.50	4.60
L	0.30	0.40	0.50
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
N		40	

TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

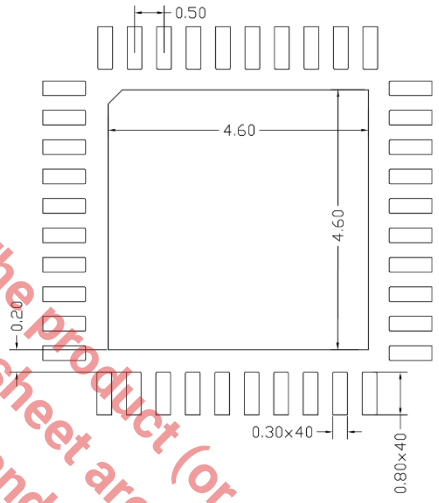
Drawing No.: POD- 00000137

Revision: A

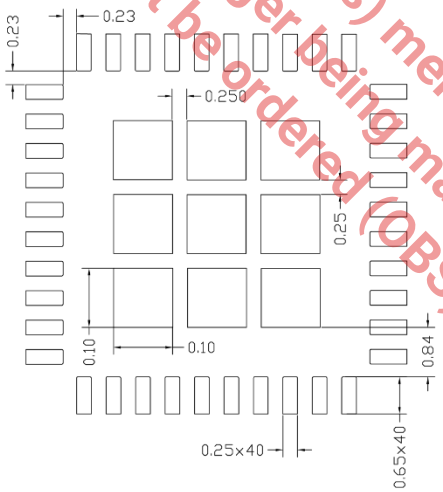
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RECOMMENDED LAND PATTERN AND STENCIL

40-PIN 6mmX6mm TQFN



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD- 00000137

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REVISION HISTORY

Revision	Date	Description
1.0.2	02/01/2010	Approved and first release of data sheet
1.0.3	02/02/2010	Minor edits
1.2.0	04/14/2010	Combined XRP7708 Rev 1.0.3 and XRP7740 Rev 1.1.0 into one document. Added I2C information. Added enable pin sequencing information. Updated gate drive resistance information. Corrected package thermal resistance. Added part to order information table
1.2.1	12/5/2011	Added information on soft-start flag. Added new ANP-35 reference and ANP-31 reference. Changed logo color. More emphasis on the connection of PGND pins.
1.2.2	04/20/2012	Corrected typographical errors. First page, change exposed pad designation from DGND to AGND Pin description table; GL1 corrected from pin "34" to "35", LX3 and LX4 corrected from pins "23,18" to "18,23"
1.3.0	02/24/2020	Updated to MaxLinear logo. Updated format and Ordering Information. Changed PGND1-4 to GL_RTN1-4. Removed obsolete XRP7708. Corrected Figure numbers.

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