GENERAL DESCRIPTION

The XRA1201/1201P is a 16-bit GPIO expander with an I²C/SMBus interface. After power-up, the XRA1201 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled. The XRA1201P has the internal pull-up resistors enabled upon power-up in case it is necessary for the inputs to be in a known state.

In addition, the GPIOs on the XRA1201/1201P can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt can be programmed for different behaviors. The interrupts can be programmed to generate an interrupt on the rising edge, falling edge or on both edges. The interrupt can be cleared if the input changes back to its original state or by reading the current state of the inputs.

The XRA1201/1201P are enhanced versions of other 16-bit GPIO expanders with an I²C/SMBus interface. The XRA1201 is pin and software compatible with the PCA9535, TCA9535 and MAX7312. The XRA1201P is pin and software compatible with the CAT9555, PCA9555, TCA9555, MAX7311 and MAX7318.

The XRA1201/1201P are available in 24-pin QFN and 24-pin TSSOP packages.

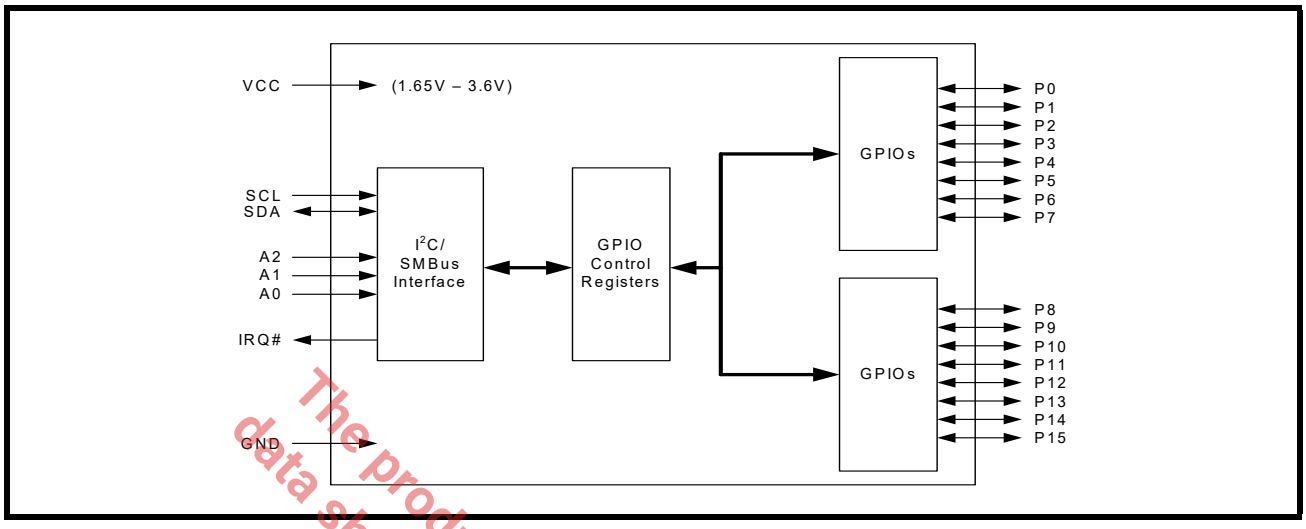
FEATURES

- 1.65V to 3.6V operating voltage
- 16 General Purpose I/Os (GPIOs)
- 5V tolerant inputs
- Maximum stand-by current of 1uA at +1.8V
- I²C/SMBus bus interface
- I²C clock frequency up to 400kHz
- Noise filter on SDA and SCL inputs
- Up to 32 I²C Slave Addresses
- Individually programmable inputs
- Internal pull-up resistors
- Polarity inversion
- Individual interrupt enable
- Rising edge and/or Falling edge interrupt
- Input filter
- Individually programmable outputs
- Output Level Control
- Output Three-State Control
- Open-drain active low interrupt output
- Pin and software compatible with PCA9535, TCA9535, MAX7312 (XRA1201)
- Pin and software compatible with CAT9555, PCA9555, TCA9555, MAX7311 and MAX7318 (XRA1201P)
- 3kV HBM ESD protection per JESD22-A114F
- 200mA latch-up performance per JESD78B

APPLICATIONS

- Personal Digital Assistants (PDA)
- Cellular Phones/Data Devices
- Battery-Operated Devices
- Global Positioning System (GPS)
- Bluetooth

FIGURE 1. XRA1201 BLOCK DIAGRAM

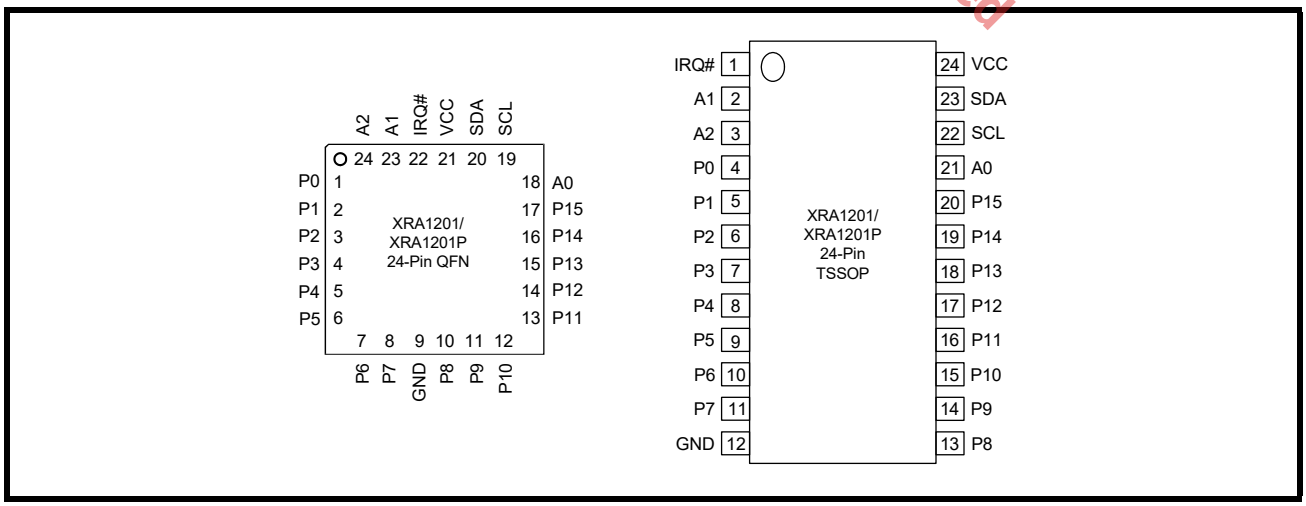


ORDERING INFORMATION

PART NUMBER	NUMBER OF GPIOS	OPERATING TEMPERATURE RANGE	PACKAGE	PACKAGE METHOD	LEAD-FREE
XRA1201IL24TR-F	16	-40°C to +85°C	QFN-24	Tape and Reel	Yes
XRA1201PIL24-F	16	-40°C to +85°C	QFN-24	Tray	Yes
XRA1201IG24TR-F	16	-40°C to +85°C	TSSOP-24	Tape and Reel	Yes
XRA1201PIG24TR-F	16	-40°C to +85°C	TSSOP-24	Tape and Reel	Yes
XRA1201IL24-0A-EB	XRA1201IL24TR-F Evaluation Board				
XRA1201IG24-0A-EB	XRA1201IG24TR-F Evaluation Board				
XRA1201PIL24-0A-EB	XRA1201PIL24-F Evaluation Board				
XRA1201PIG24-0A-EB	XRA1201PIG24TR-F Evaluation Board				

NOTE: *For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/XRA1201 and www.maxlinear.com/XRA1201P.*

FIGURE 2. PIN OUT ASSIGNMENTS



PIN DESCRIPTIONS

Pin Description

NAME	QFN-24 PIN#	TSSOP-24 PIN#	TYPE	DESCRIPTION
I²C INTERFACE				
SDA	20	23	I/O	I²C-bus data input/output (open-drain).
SCL	19	22	I	I²C-bus serial input clock.
IRQ#	22	1	OD	Interrupt output (open-drain, active LOW).
A0	18	21	I	These pins select the I²C slave address. See Table 1.
A1	23	2	I	
A2	24	3	I	
GPIOs				
P0	1	4	I/O	General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up. After power-up, the internal pull-up resistors are enabled for the XRA1201P. The internal pull-up resistors are disabled for the XRA1201.
P1	2	5	I/O	
P2	3	6	I/O	
P3	4	7	I/O	
P4	5	8	I/O	
P5	6	9	I/O	
P6	7	10	I/O	
P7	8	11	I/O	
P8	10	13	I/O	General purpose I/O P8-P15. All GPIOs are configured as inputs upon power-up. After power-up, the internal pull-up resistors are enabled for the XRA1201P. The internal pull-up resistors are disabled for the XRA1201.
P9	11	14	I/O	
P10	12	15	I/O	
P11	13	16	I/O	
P12	14	17	I/O	
P13	15	18	I/O	
P14	16	19	I/O	
P15	17	20	I/O	
ANCILLARY SIGNALS				
VCC	21	24	Pwr	1.65V to 3.6V VCC supply voltage.
GND	9	12	Pwr	Power supply common, ground.
GND	Center Pad	-	Pwr	The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 FUNCTIONAL DESCRIPTIONS

1.1 I²C-bus Interface

The I²C-bus interface is compliant with the Standard-mode and Fast-mode I²C-bus specifications. The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the Standard-mode, the serial clock and serial data can go up to 100 kbps and in the Fast-mode, the serial clock and serial data can go up to 400 kbps.

The first byte sent by an I²C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The XRA120x responds to each write with an acknowledge (SDA driven LOW by XRA1201/1201P for one clock cycle when SCL is HIGH). The last byte sent by an I²C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See Figures 3 - 5 below. For complete details, see the I²C-bus specifications.

FIGURE 3. I²C START AND STOP CONDITIONS

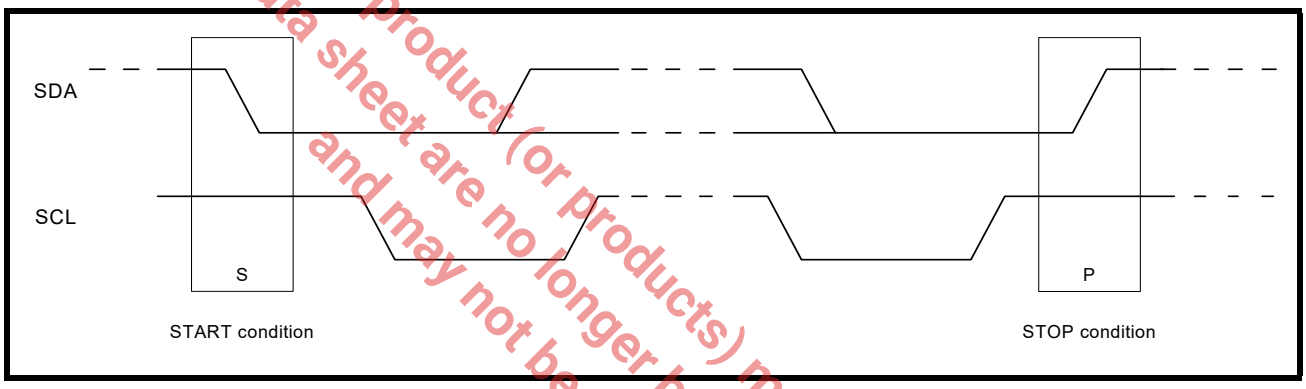


FIGURE 4. MASTER WRITES TO SLAVE

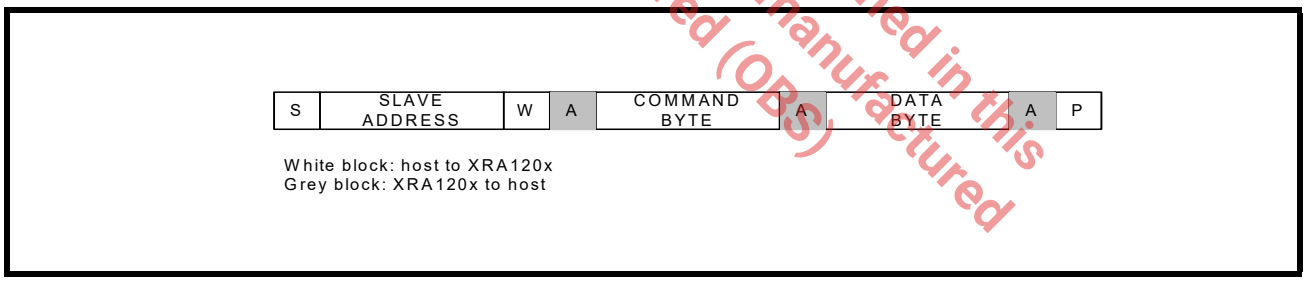
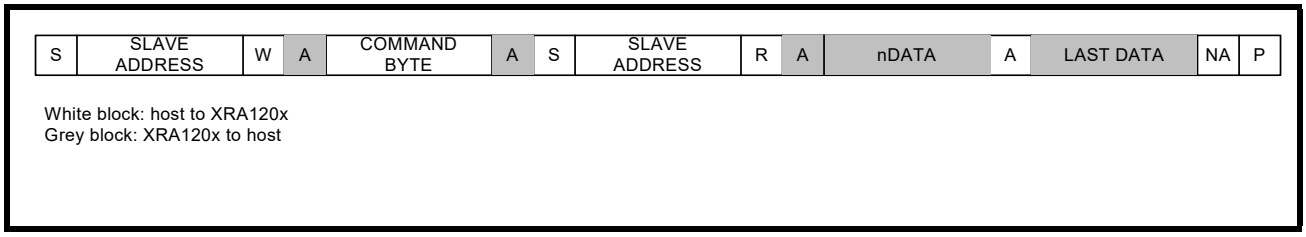


FIGURE 5. MASTER READS FROM SLAVE



1.1.1 I²C-bus Addressing

There could be many devices on the I²C-bus. To distinguish itself from the other devices on the I²C-bus, the XRA1201/1201P has up to 32 I²C slave addresses using the A2-A0 address lines. Table 1 below shows the different addresses that can be selected.

TABLE 1: I²C ADDRESS MAP

A2	A1	A0	I²C ADDRESS
GND	SCL	GND	0x20 (0010 000X)
GND	SCL	VCC	0x22 (0010 001X)
GND	SDA	GND	0x24 (0010 010X)
GND	SDA	VCC	0x26 (0010 011X)
VCC	SCL	GND	0x28 (0010 100X)
VCC	SCL	VCC	0x2A (0010 101X)
VCC	SDA	GND	0x2C (0010 110X)
VCC	SDA	VCC	0x2E (0010 111X)
GND	SCL	SCL	0x30 (0011 000X)
GND	SCL	SDA	0x32 (0011 001X)
GND	SDA	SCL	0x34 (0011 010X)
GND	SDA	SDA	0x36 (0011 011X)
VCC	SCL	SCL	0x38 (0011 100X)
VCC	SCL	SDA	0x3A (0011 101X)
VCC	SDA	SCL	0x3C (0011 110X)
VCC	SDA	SDA	0x3E (0011 111X)
GND	GND	GND	0x40 (0100 000X)
GND	GND	VCC	0x42 (0100 001X)
GND	VCC	GND	0x44 (0100 010X)
GND	VCC	VCC	0x46 (0100 011X)
VCC	GND	GND	0x48 (0100 100X)
VCC	GND	VCC	0x4A (0100 101X)
VCC	VCC	GND	0x4C (0100 110X)
VCC	VCC	VCC	0x4E (0100 111X)
GND	GND	SCL	0x50 (0101 000X)
GND	GND	SDA	0x52 (0101 001X)
GND	VCC	SCL	0x54 (0101 010X)
GND	VCC	SDA	0x56 (0101 011X)
VCC	GND	SCL	0x58 (0101 100X)
VCC	GND	SDA	0x5A (0101 101X)
VCC	VCC	SCL	0x5C (0101 110X)
VCC	VCC	SDA	0x5E (0101 111X)

1.1.2 I²C Read and Write

A read or write transaction is determined by bit-0 of the slave address. If bit-0 is '0', then it is a write transaction. If bit-0 is '1', then it is a read transaction.

1.1.3 I²C Command Byte

An I²C command byte is sent by the I²C master following the slave address. The command byte indicates the address offset of the register that will be accessed. Table 2 below lists the command bytes for each register.

TABLE 2: I²C COMMAND BYTE (REGISTER ADDRESS)

COMMAND BYTE	REGISTER NAME DESCRIPTION	READ/WRITE	DEFAULT VALUES
0x00	GSR1 - GPIO State for P0-P7	Read-Only	0xXX
0x01	GSR2 - GPIO State for P8-P15	Read-Only	0xXX
0x02	OCR1 - Output Control for P0-P7	Read/Write	0xFF
0x03	OCR2 - Output Control for P8-P15	Read/Write	0xFF
0x04	PIR1 - Input Polarity Inversion for P0-P7	Read/Write	0x00
0x05	PIR2 - Input Polarity Inversion for P8-P15	Read/Write	0x00
0x06	GCR1 - GPIO Configuration for P0-P7	Read/Write	0xFF
0x07	GCR2 - GPIO Configuration for P8-P15	Read/Write	0xFF
0x08	PUR1 - Input Internal Pull-up Resistor Enable/Disable for P0-P7	Read/Write	0x00 (XRA1201) 0xFF (XRA1201P)
0x09	PUR2 - Input Internal Pull-up Resistor Enable/Disable for P8-P15	Read/Write	0x00 (XRA1201) 0xFF (XRA1201P)
0x0A	IER1 - Input Interrupt Enable for P0-P7	Read/Write	0x00
0x0B	IER2 - Input Interrupt Enable for P8-P15	Read/Write	0x00
0x0C	TSCR1 - Output Three-State Control for P0-P7	Read/Write	0x00
0x0D	TSCR2 - Output Three-State Control for P8-P15	Read/Write	0x00
0x0E	ISR1 - Input Interrupt Status for P0-P7	Read	0x00
0x0F	ISR2 - Input Interrupt Status for P8-P15	Read	0x00
0x10	REIR1 - Input Rising Edge Interrupt Enable for P0-P7	Read/Write	0x00
0x11	REIR2 - Input Rising Edge Interrupt Enable for P8-P15	Read/Write	0x00
0x12	FEIR1 - Input Falling Edge Interrupt Enable for P0-P7	Read/Write	0x00
0x13	FEIR2 - Input Falling Edge Interrupt Enable for P8-P15	Read/Write	0x00
0x14	IFR1 - Input Filter Enable/Disable for P0-P7	Read/Write	0xFF
0x15	IFR2 - Input Filter Enable/Disable for P8-P15	Read/Write	0xFF

1.2 Interrupts

The table below summarizes the interrupt behavior of the different register settings for the XRA1201/1201P.

TABLE 3: INTERRUPT GENERATION AND CLEARING

GCR BIT	IER BIT	REIR BIT	FEIR BIT	IFR BIT	INTERRUPT GENERATED BY:	INTERRUPT CLEARED BY:
1	0	X	X	X	No interrupts enabled (default)	N/A
1	1	0	0	0	A rising or falling edge on the input	Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR)
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns	
1	1	1	0	0	A rising edge on the input	Reading the GSR register
				1	A rising edge on the input and remains high for more than 1075ns	
1	1	0	1	0	A falling edge on the input	Reading the GSR register
				1	A falling edge on the input and remains low for more than 1075ns	
1	1	1	1	0	A rising or falling edge on the input	Reading the GSR register
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns	
0	x	x	x	x	No interrupts in output mode	N/A

2.0 REGISTER DESCRIPTION

2.1 GPIO State Register 1 (GSR1) - Read-Only

The status of P7 - P0 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.2 GPIO State Register 2 (GSR2) - Read-Only

The status of P15 - P8 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.3 Output Control Register 1 (OCR1) - Read/Write

When P7 - P0 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.4 Output Control Register 2 (OCR2) - Read/Write

When P15 - P8 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.5 Input Polarity Inversion Register 1 (PIR1) - Read/Write

When P7 - P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.6 Input Polarity Inversion Register 2 (PIR2) - Read/Write

When P15 - P8 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.7 GPIO Configuration Register 1 (GCR1) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.8 GPIO Configuration Register 2 (GCR2) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.9 Input Internal Pull-up Enable/Disable Register 1 (PUR1) - Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up, the internal pull-up resistors are disabled for the XRA1201. Writing a '1' to these bits will enable the internal pull-up resistors. After power-up, the internal pull-up resistors are enabled for the XRA1201P. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.10 Input Internal Pull-up Enable/Disable Register 2 (PUR2) - Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up, the internal pull-up resistors are disabled for the XRA1201. Writing a '1' to these bits will enable the internal pull-up resistors. After power-up, the internal pull-up resistors are enabled for the XRA1201P. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.11 Input Interrupt Enable Register 1 (IER1) - Read/Write

This register enables/disables the interrupts for an input. After power-up, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See Table 3 for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.12 Input Interrupt Enable Register 2 (IER2) - Read/Write

This register enables/disables the interrupts for an input. After power-up, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See Table 3 for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.13 Output Three-State Control Register 1 (TSCR1) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.14 Output Three-State Control Register 2 (TSCR2) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.15 Input Interrupt Status Register 1 (ISR1) - Read-Only

This register reports the input pins that have generated an interrupt. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.16 Input Interrupt Status Register 2 (ISR2) - Read-Only

This register reports the input pins that have generated an interrupt. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.17 Input Rising Edge Interrupt Enable Register 1 (REIR1) - Read/Write

Writing a ’1’ to these bits will enable the corresponding input to generate an interrupt on the rising edge. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.18 Input Rising Edge Interrupt Enable Register 2 (REIR2) - Read/Write

Writing a ’1’ to these bits will enable the corresponding input to generate an interrupt on the rising edge. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.19 Input Falling Edge Interrupt Enable Register 1 (FEIR1) - Read/Write

Writing a ’1’ to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a ’1’ to these bits will make that input generate an interrupt on the rising edge only. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.20 Input Falling Edge Interrupt Enable Register 2 (FEIR2) - Read/Write

Writing a ’1’ to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a ’1’ to these bits will make that input generate an interrupt on the rising edge only. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

2.21 Input Filter Enable Register 1 (IFR1) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a ’0’ to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

2.22 Input Filter Enable Register 2 (IFR2) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a ’0’ to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P15 and the LSB of this register corresponds with P8.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	3.6 Volts
Supply current	160 mA
Ground current	200 mA
External current limit of each GPIO	25 mA
Total current limit for GPIO[15:8] and GPIO[7:0]	100 mA
Total current limit for GPIO[15:0]	200 mA
Total supply current sourced by all GPIOs	160 mA
Operating Temperature	-40° to +85°C
Storage Temperature	-65° to +150°C
Power Dissipation	200 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (24-QFN)	theta-ja = 38°C/W, theta-jc = 26°C/W
Thermal Resistance (24-TSSOP)	theta-ja = 84°C/W, theta-jc = 16°C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC IS 1.65V TO 3.6V

SYMBOL	PARAMETER	LIMITS 1.8V ± 10% MIN	LIMITS 1.8V ± 10% MAX	LIMITS 2.5V ± 10% MIN	LIMITS 2.5V ± 10% MAX	LIMITS 3.3V ± 10% MIN	LIMITS 3.3V ± 10% MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	-0.3	0.3VCC	-0.3	0.3VCC	-0.3	0.3VCC	V	Note 1
V_{IL}	Input Low Voltage	-0.3	0.2	-0.3	0.5	-0.3	0.8	V	Note 2
V_{IH}	Input High Voltage	1.3	VCC	1.8	VCC	2.3	VCC	V	Note 1
V_{IH}	Input High Voltage	1.4	5.5	1.8	5.5	2.0	5.5	V	Note 2
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V V V	I_{OL} = 3 mA I_{OL} = 3 mA I_{OL} = 3 mA Note 3
V_{OL}	Output Low Voltage		0.5		0.5		0.5	V	I_{OL} = 8 mA Note 4
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V V V	I_{OL} = 6 mA I_{OL} = 4 mA I_{OL} = 1.5 mA Note 5
V_{OH}	Output High Voltage	1.2		1.8		2.6		V V V	I_{OH} = -8 mA I_{OH} = -8 mA I_{OH} = -8 mA Note 4
I_{IL}	Input Low Leakage Current		±10		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10		±10	uA	
C_{IN}	Input Pin Capacitance		5		5		5	pF	
I_{CC}	Power Supply Current		50		100		200	uA	Test 1
I_{CC}	Power Supply Current		150		250		500	uA	Test 2
I_{CCS}	Standby Current		1		2		5	uA	Test 3
R_{GPIO}	GPIO pull-up resistance	60	140	60	140	60	140	kΩ	100kΩ ± 40%

NOTES:

1. *For I²C input signals (SDA, SCL);*
2. *For GPIOs, A0, A1 and A2 signals;*
3. *For I²C output signal SDA;*
4. *For GPIOs;*
5. *For IRQ# signal;*

Test 1: SCL frequency is 400 KHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.
Test 2: SCL frequency is 400 KHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.
Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. All GPIOs are configured as inputs. SCL and SDA are at VCC. Outputs are left floating or in tri-state mode.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise noted: TA=-40° to +85°C, Vcc=1.65V - 3.6V

Symbol	Parameter	Standard Mode I²C-Bus		Fast Mode I²C-Bus		Unit
		Min	Max	Min	Max	
f_{SCL}	Operating frequency	0	100	0	400	kHz
T_{BUF}	Bus free time between STOP and START	4.7		1.3		µs
$T_{HD;STA}$	START condition hold time	4.0		0.6		µs
$T_{SU;STA}$	START condition setup time	4.7		0.6		µs
$T_{HD;DAT}$	Data hold time	0		0		ns
$T_{VD;ACK}$	Data valid acknowledge		0.6		0.6	µs
$T_{VD;DAT}$	SCL LOW to data out valid		0.6		0.6	ns
$T_{SU;DAT}$	Data setup time	250		150		ns
T_{LOW}	Clock LOW period	4.7		1.3		µs
T_{HIGH}	Clock HIGH period	4.0		0.6		µs
T_F	Clock/data fall time		300		300	ns
T_R	Clock/data rise time		1000		300	ns
T_{SP}	Pulse width of spikes tolerance	50		50		ns
T_{D1}	I²C-bus GPIO output valid		0.2		0.2	µs
T_{D4}	I²C input pin interrupt valid		4		4	µs
T_{D5}	I²C input pin interrupt clear		4		4	µs
T_{D15}	SCL delay after reset	3		3		µs

FIGURE 6. I²C-BUS TIMING DIAGRAM

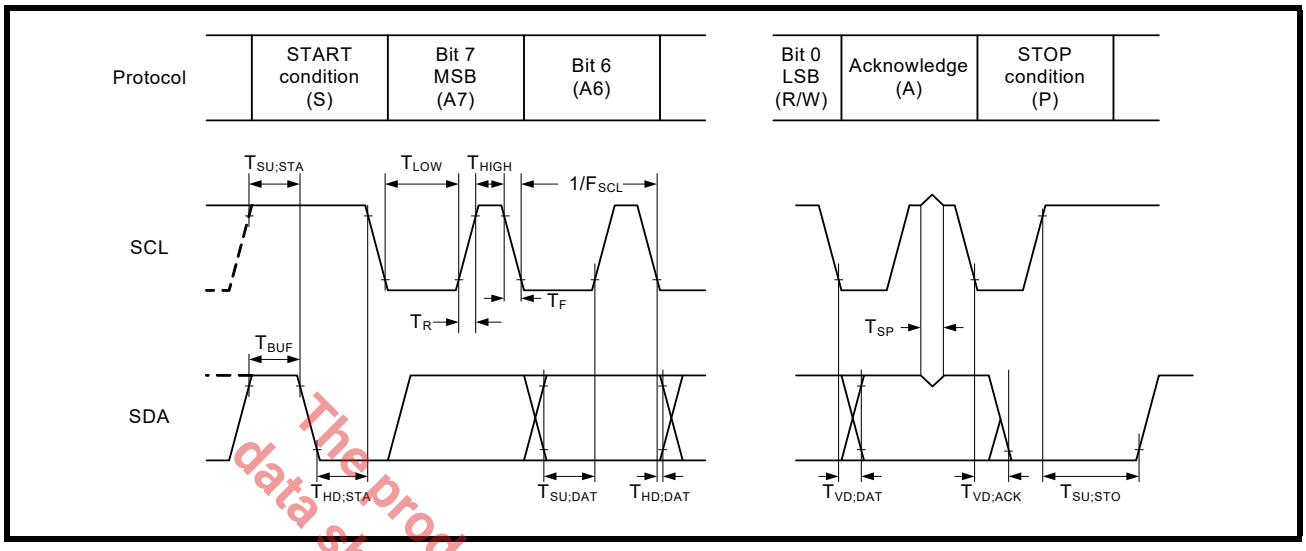


FIGURE 7. WRITE TO OUTPUT

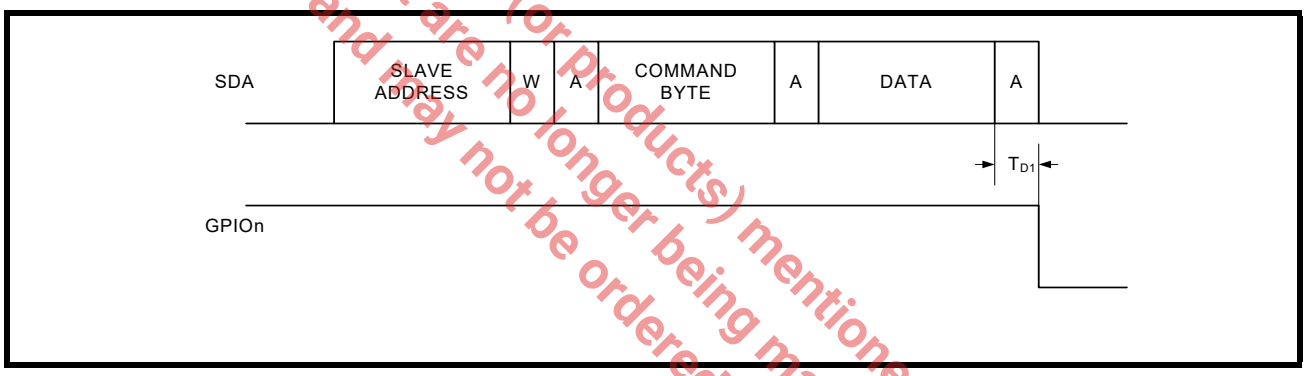
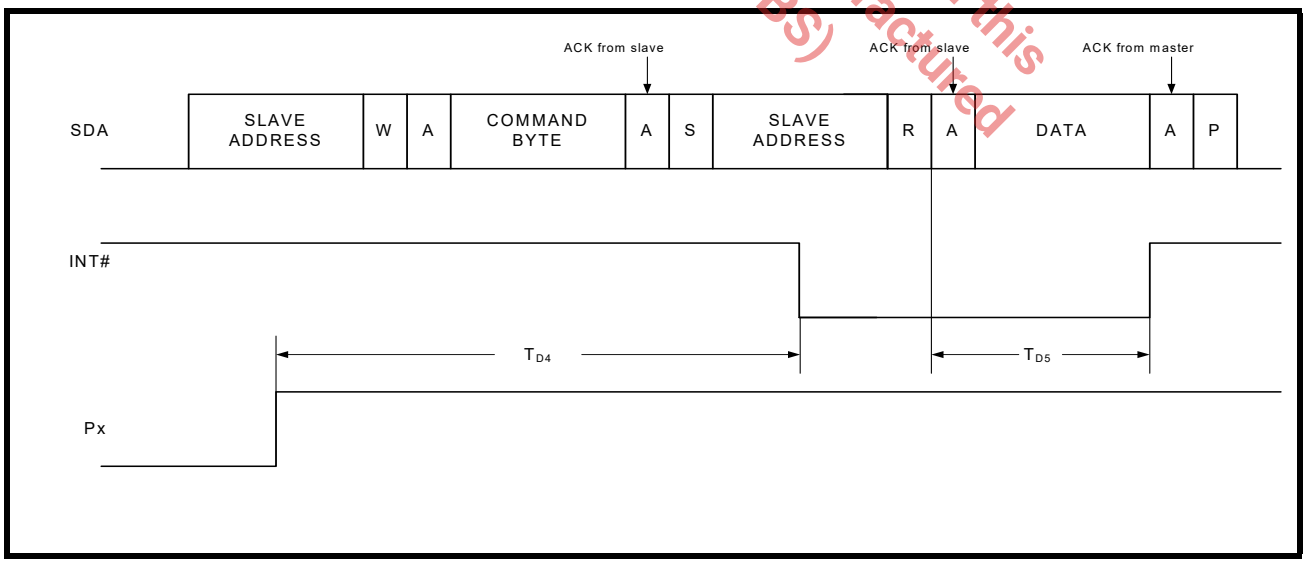
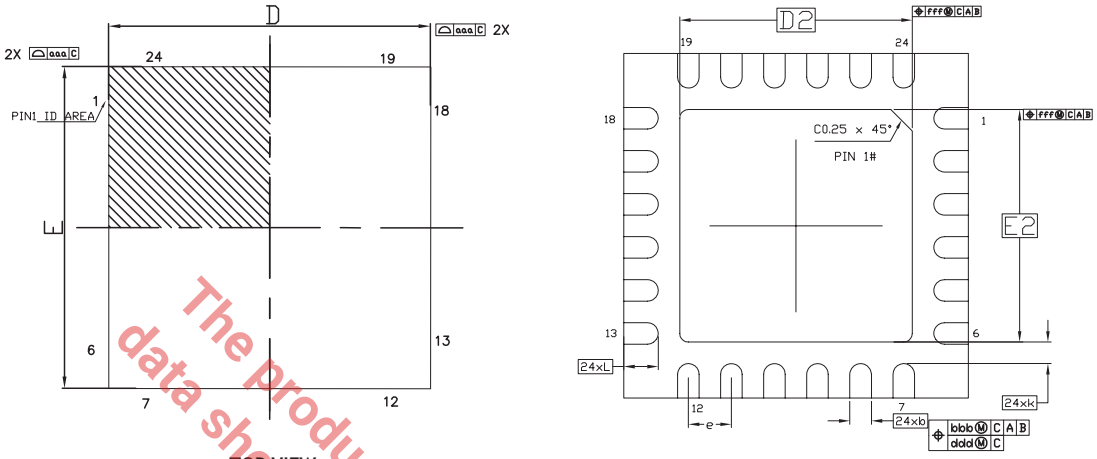
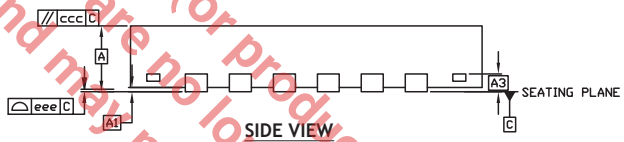


FIGURE 8. GPIO PIN INTERRUPT



MECHANICAL DIMENSIONS (24 PIN QFN - 4 X 4 X 0.9 mm)





DIM / SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	–	0.203Ref	–
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.20	2.40	2.60
E2	2.20	2.40	2.60
L	0.35	0.40	0.45
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		24	

TERMINAL DETAILS

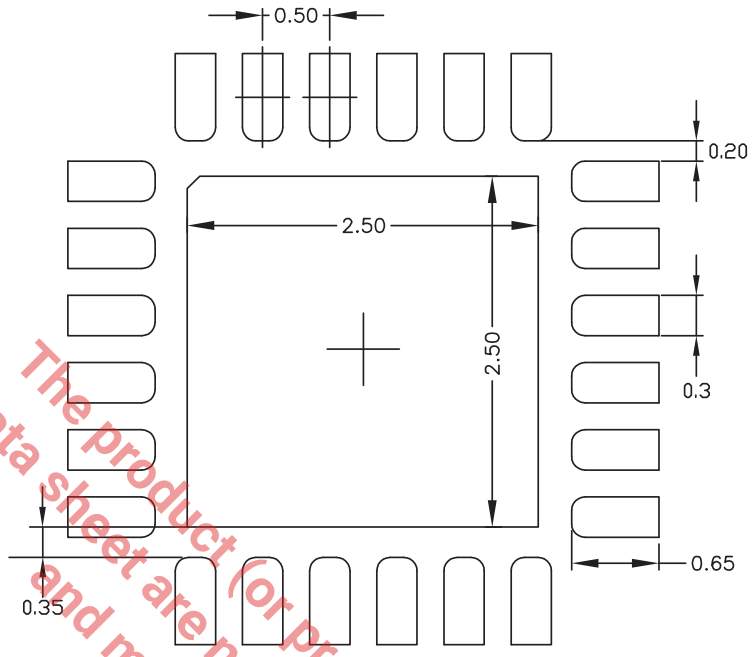
- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

Drawing No.: POD-00000 142

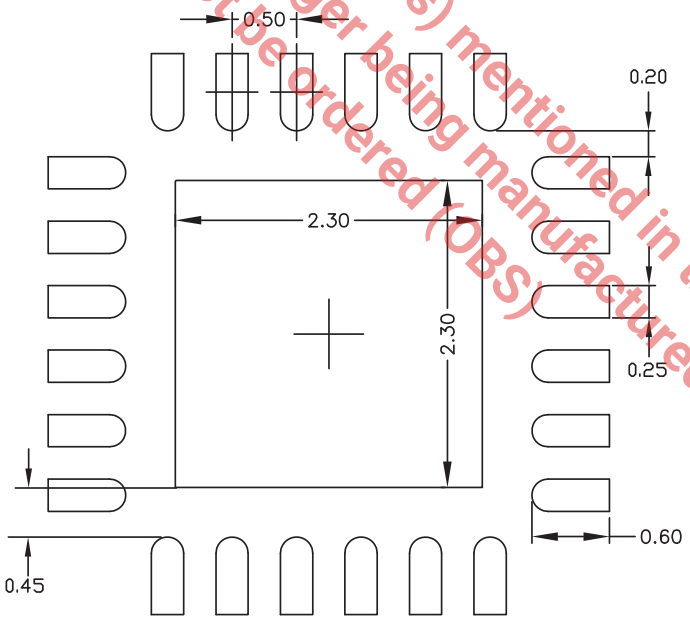
Revision: A

Note: The control dimension is in millimeter.

RECOMMENDED LAND PATTERN AND STENCIL (24 PIN QFN - 4 X 4 X 0.9 mm)



TYPICAL RECOMMENDED LAND PATTERN



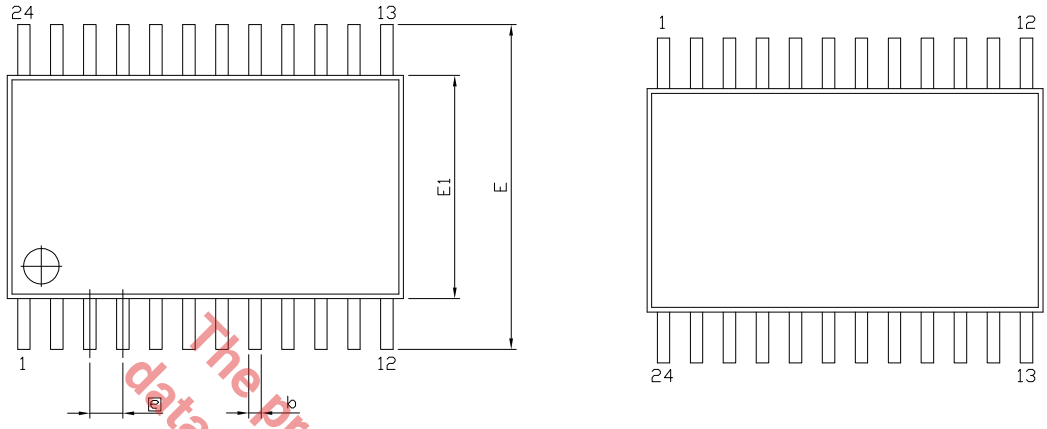
TYPICAL RECOMMENDED STENCIL

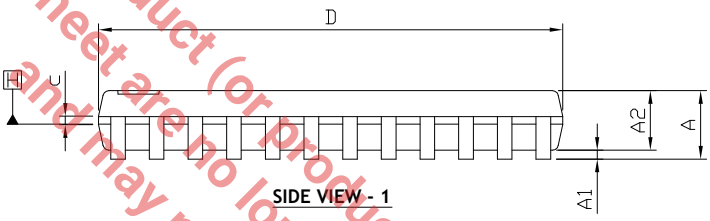
Drawing No.: POD-00000 142

Revision: A

Note: The control dimension is in millimeter.

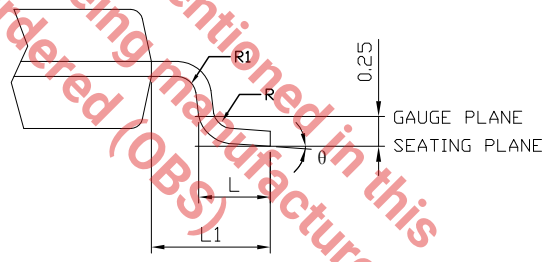
MECHANICAL DIMENSIONS (24 PIN TSSOP - 4.4 mm)





DIM / SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	7.70	7.80	7.90
E	6.40 BSC		
e	0.65 BSC		
E1	4.30	4.40	4.50
c	0.09	–	0.20
L	0.45	0.60	0.75
L1	1.0 REF		
θ	0	–	8
R	0.09	–	–
R1	0.09	–	–
N		24	

TERMINAL DETAILS



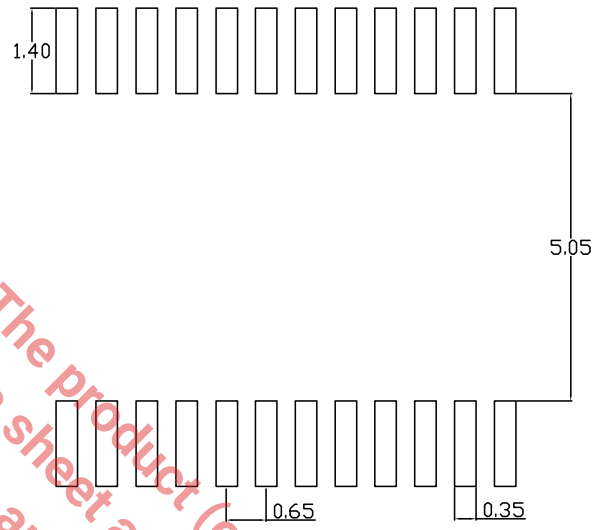
- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-153.

Drawing No.: POD-00000058

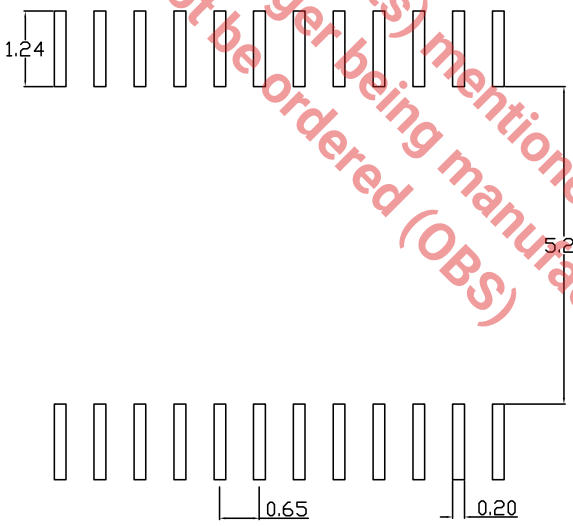
Revision: D

Note: The control dimension is in millimeter.

RECOMMENDED LAND PATTERN AND STENCIL (24 PIN TSSOP - 4 X 4 mm)



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000058

Revision: D

Note: The control dimension is in millimeter.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
September 2011	1.0.0	Final Datasheet.
August 2020	1.0.1	Update to MaxLinear logo. Update Ordering Information.
February 2, 2022	1.0.2	**Updated:** ■ In the "TSSOP-16 versions available, QFN-16 versions obsolete" table, GPIOs parameter description. ■ "GPIO Configuration Register 1 (GCR1) - Read/Write" section. ■ "GPIO Configuration Register 2 (GCR2) - Read/Write" section. ■ "Input Internal Pull-up Enable/Disable Register 1 (PUR1) - Read/Write" section. ■ "Input Interrupt Enable Register 1 (IER1) - Read/Write" section. ■ "Input Interrupt Enable Register 2 (IER2) - Read/Write" section. ■ "Input Interrupt Enable Register (IER) - Read/Write" section. ■ "Mechanical Dimensions (24 pin QFN)" figure. ■ "Recommended and Pattern and Stencil (24 pin QFN)" figure. ■ "Mechanical Dimensions (24 pin TSSOP)" figure. ■ "Recommended Land Pattern and Stencil (24 pin QFN)" figure.

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