XRP7720

Quad Output Universal Customizable PMIC with PFM

January 2014 Rev. 1.0.0

GENERAL DESCRIPTION

The XRP7720 is a quad output universal customizable PMIC comprised of a quad channel Digital Pulse Width Modulated (DPWM) Step down (buck) controller and 5V LDO. A wide 4.75V to 5.5V and 5.5V to 18V input voltage dual range allows for single supply operation from standard power rails. It is pin compatible to the popular XRP7724 and provides full flexibility during the development phase while offering a cost effective option for high volume production units.

With integrated FET gate drivers, it can operate from 105kHz to 1.23MHz with independent channel-to-channel programmable operating frequency, the XRP7720 reduces overall component count and solution footprint while optimizing conversion efficiencies. A selectable digital Pulse Frequency Mode (DPFM) and low operating current result in better than 80% efficiency down to 10mA load provides support for portable and Energy Star compliant applications. Each XRP7720 output channel is individually programmable down to a minimum 0.6V with a resolution of 2.5mV, and configurable for precise soft start and soft stop sequencing, including delay and ramp control.

During development, the XRP7720ILB-DEV is configured using PowerArchitect™ 5.1 (PA 5.1) through an I²C interface, allowing for short development of the power system and short time to market for the entire system. Once development is completed and volume production is ready to commence, Exar will assign a unique part suffix and deliver a customized XRP7720.

Built-in independent output over voltage, over temperature, over-current and under voltage lockout protections ensure safe operation under abnormal operating conditions.

The XRP7720 is offered in a RoHS compliant, "green"/halogen free 44-pin TQFN package.

FEATURES

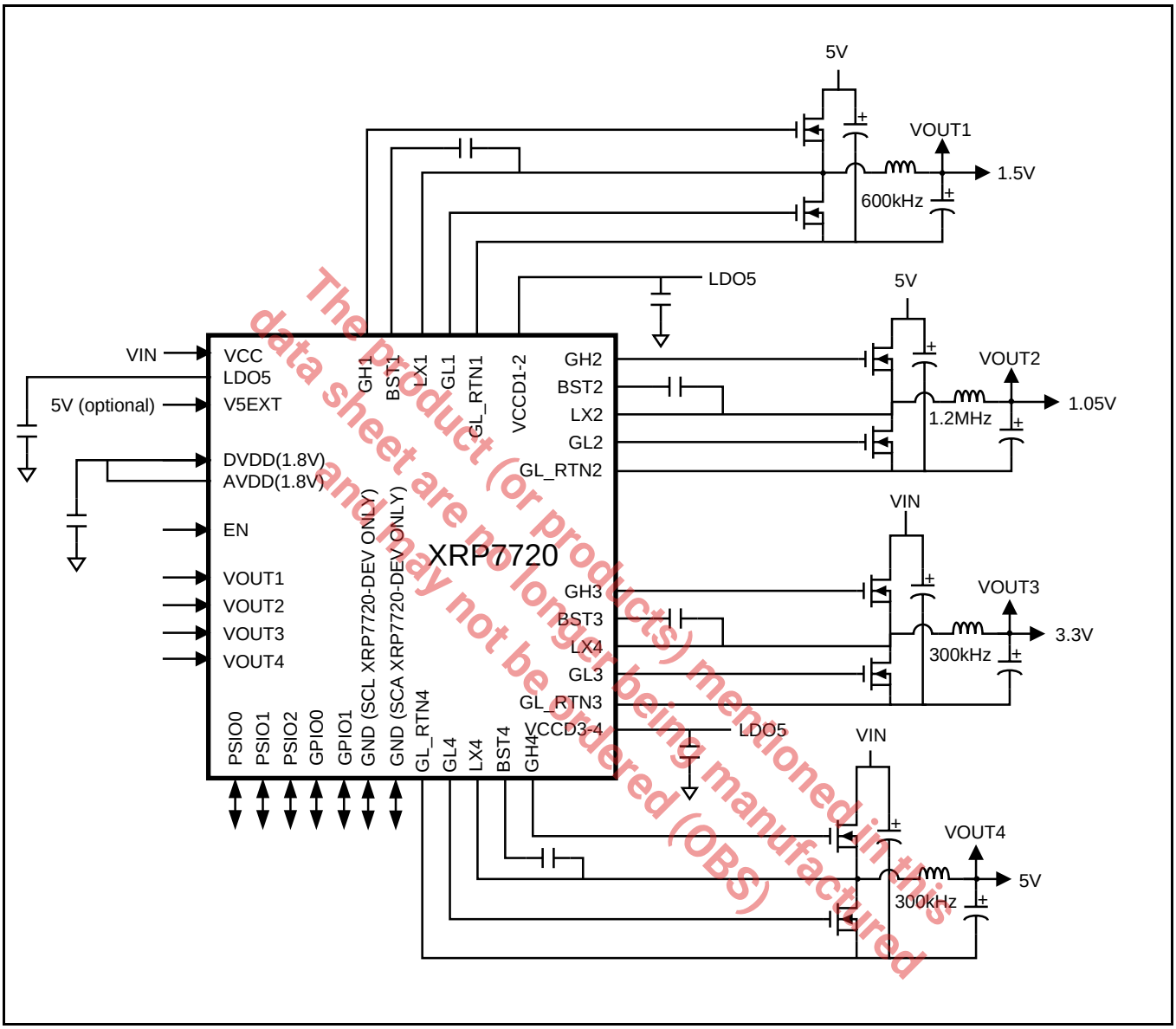
- **Pin Compatible to XRP7724**
  - SMBus Compliant I²C Interface available on XRP7720ILB-DEV Only
- **Supported by PowerArchitect™ 5.1**
  - XRP7720ILB-DEV Only
- **Quad Channel Step-down Controller**
  - Digital PWM 105kHz-1.23MHz Operation
  - Individual Channel Frequency Selection
  - Patented digital PFM with Ultrasonic Mode
  - Integrated MOSFET Drivers
  - Programmable 5 coefficient PID control
- **4.75V to 18V Input Voltage**
  - 4.75V-5.5 and 5.5V-18V Input Range
  - 0.6V to 5.5V Output voltage
- **3 x 15V Capable PSIOs + 2 x GPIOs**
- **Full Start/Stop Sequencing Support**
- **Built-in Thermal, Over-Current, UVLO and Output Over-Voltage Protections**
- **On Board 5V Standby LDO**
- **7x7mm TQFN44 Package**

APPLICATIONS

- **Blade Servers**
- **Micro Servers**
- **Network Adapter Cards**
- **Switches/Routers**
- **Video Surveillance Systems**

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TYPICAL APPLICATION DIAGRAM



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Figure 1 XRP7720 Application Diagram

FEATURES AND BENEFITS

Programmable Power Benefits

- **Fully Configurable**
  - Output set point
  - Feedback compensation
  - Frequency set point
  - Under voltage lock out
- **Reduced Development Time with XRP7720-DEV**
  - Configurable and re-configurable for different Vout, Iout, Cout, and Inductor values
  - No need to change external passives for a new output specification.
- **Higher integration and Reliability**
  - Many external circuits used in the past can be eliminated thereby significantly improving reliability.
- **Pin Compatible to XRP7724**
  - Provides easy migration path to a full featured programmable power management system with dynamic control and telemetry
- **PowerArchitect™ 5.1 Design and Configuration Software**
  - Wizard quickly generates a base design
  - Calculates all configuration registers
  - Projects can be saved and recalled
  - GPIOs can be configured easily and intuitively
  - "Dashboard" Interface can be used for real-time monitoring and debug (-DEV ONLY)

System Integration Capabilities

- **Single supply operation**
- **5 GPIO pins with a wide range of configurability**
  - Fault reporting (including UVLO Warn/Fault, OCP Warn/Fault, OVP, Temperature, Soft-Start in progress, Power Good, System Reset)
  - Allows a Logic Level interface with other ICs or as logic inputs to other devices
  - Selectable switching frequency between 105kHz and 1.2MHz
- **Internal MOSFET Drivers**
  - Internal FET drivers (4Ω/2Ω) per channel
  - Built-In Automatic Dead-time adjustment
  - 30ns Rise and Fall times
- **4 Independent SMPS channels and Standby LDO in a 7x7mm TQFN**

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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

VCCD, LDO5, GLx, VOUTx ..... -0.3V to 7.0V
ENABLE, 5V_EXT ..... -0.3V to 7.0V
GPIO0/1, SCL, SDA 6.0V
PSIOs Inputs 18V
DVDD, AVDD 2.0V
V_{CC} 23V
LX# ..... -1V to 23V
BSTx, GHx ..... VLXx + 6V
Storage Temperature ..... -65°C to 150°C
Junction Temperature ..... 150°C
Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating (HBM - Human Body Model) 2kV

OPERATING RATINGS

Input Voltage Range V_{CC} ..... 5.5V to 18V
Input Voltage Range V_{CC} = LDO5 ..... 4.75V to 5.5V
VOUT1, 2, 3, 4 ..... 5.5V
Junction Temperature Range ..... -40°C to 125°C
JEDEC Thermal Resistance θ_{JA} ..... 30.2°C/W

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ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{CC} = 5.5V to 18V, 5V EXT open.

QUIESCENT CURRENT

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{CC} Supply Current in SHUTDOWN		10	20	µA		EN = 0V, V_{CC} = 12V
ENABLE Turn On Threshold	0.82		0.95	V		V_{CC} = 12V Enable Rising
ENABLE Pin Leakage Current			10	uA		EN=5V
	-10			uA		EN=0V
V_{CC} Supply Current in STANDBY		440	600	µA		all channels disabled GPIOs programmed as inputs V_{CC} =12V,EN = 5V
V_{CC} Supply Current 4ch PFM		4.0		mA		4 channels on set at 5V, VOUT forced to 5.1V, no load, non-switching, Ultra-sonic off, V_{CC}=12V, No I^2C activity.
V_{CC} Supply Current ON		18		mA		All channels enabled, Fsw=600kHz, gate drivers unloaded, No I^2C activity.

INPUT VOLTAGE RANGE AND UNDERVOLTAGE LOCKOUT

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{CC} Range	5.5		18	V	•	
	4.75		5.5	V	•	With V_{CC} connected to LDO5

VOLTAGE FEEDBACK ACCURACY AND OUTPUT VOLTAGE SET POINT RESOLUTION

Parameter	Min.	Typ.	Max.	Units		Conditions
VOUT Regulation Accuracy Low Output Range 0.6V to 1.6V PWM Operation	-5		5	mV		0.6 ≤ VOUT ≤ 1.6V
	-20		20	mV	•	
	-7.5		7.5	mV		0.6 ≤ VOUT ≤ 1.6V V_{CC}=LDO5
	-22.5		22.5	mV	•	
VOUT Regulation Accuracy Mid Output Range 0.6V to 3.2V PWM Operation	-15		15	mV		0.6 ≤ VOUT ≤ 3.2V
	-45		45	mV	•	
	-20		20	mV		0.6 ≤ VOUT ≤ 3.2V V_{CC}=LDO5
	-50		50	mV	•	
VOUT Regulation Accuracy High Output Range 0.6V to 5.5V PWM Operation	-30		30	mV		0.6 ≤ VOUT ≤ 5.5V
	-90		90	mV	•	
	-40		40	mV		0.6 ≤ VOUT ≤ 4.2V V_{CC}=LDO5
	-100		100	mV	•	
VOUT Regulation Range	0.6		5.5	V	•	
VOUT Set Point Resolution[1]		2.5 5 10		mV		Low Range Mid Range High Range
VOUT Input Resistance		120 90 75		kΩ		Low Range Mid Range High Range
VOUT Input Resistance in PFM Operation		10 1 0.67		MΩ		Low Range Mid Range High Range
Power Good and OVP Set Point Range (from set point)	-155 -310 -620		157.5 315 630	mV		Low Range Mid Range High Range
Power Good and OVP Set Point Accuracy	-5 -10 -20		5 10 20	mV		Low Range Mid Range High Range

Note 1: Fine Set Point Resolution not available in PFM

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FAULTS AND WARNINGS

Parameter	Min.	Typ.	Max.	Units		Conditions
Current Limit Accuracy	-3.75	±1.25	3.75	mV		Low Range (≤120mV)
	-10		10	mV	•	-60mV applied
	-5	±2.5	5	mV		High Range (≤280mV)
	-12.5		+12.5	mV	•	-150mV applied
Current Limit Set Point Resolution		1.25		mV		Low Range (≤120mV)
		2.5		mV		High Range (≤280mV)
Current Limit Set Point Range	-120		20	mV		Low Range (≤120mV)
	-280		40			High Range (≤280mV)
V_{CC} UVLO Set Point Range	4.6		18	V		
V_{CC} UVLO Set Point Resolution		200		mV		
V_{CC} WARN and FAULT Set Point Accuracy	-400		400	mV		
V_{CC} UVLO WARN (Note 2)	4.4		4.72	V		UVLO WARN set point 4.6V, V_{CC}=LDO5
Over Temperature Set Point Resolution		5		°C		
Over Temperature Set Point Accuracy	-10		10	°C		

Note 2: This test is only performed when WARN is programmed to 4.6V.

LINEAR REGULATOR

Parameter	Min.	Typ.	Max.	Units		Conditions
LDO5 Output Voltage	4.85	5.0	5.15	V	•	5.5V ≤ V_{CC} ≤ 18V 0mA < $I_{LDO5OUT}$ < 130mA, LDO3_3 Off
LDO5 Current Limit	105	125	150	mA	•	LDO5 Fault Set
LDO5 UVLO	4.74			V	•	V_{CC} Rising
LDO5 PGOOD Hysteresis		375		mV		V_{CC} Falling
LDO5 Bypass Switch Resistance		1.1	1.5	Ω		
Bypass Switch Activation Threshold	2.5		2.5	%	•	V5EXT Rising, % of threshold setting
Bypass Switch Activation Hysteresis		150		mV		V5EXT Falling
Maximum total LDO loading during ENABLE start-up			30	mA		ENABLE transition from logic low to high. Once LDO5 in regulation above limits apply.

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PWM Generators and Oscillator

Parameter	Min.	Typ.	Max.	Units		Conditions
Switching Frequency (fsw) Range	105		1230	kHz		Steps defined in table
fsw Accuracy	–5		5	%		

GPIOs[3]

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level			0.8	V		
Input Pin High Level	2.0			V		
Input Pin Leakage Current			1	µA		
Output Pin Low Level			0.4	V		I_{SINK} = 1mA
Output Pin High Level	2.4			V		I_{SOURCE} = 1mA
Output Pin High Level		3.3	3.6	V		I_{SOURCE} = 0mA
Output Pin High-Z leakage Current (GPIO pins only)			10	µA		
Maximum Sink Current			1	mA		Open Drain Mode
I/O Frequency			30	MHz		

Note 3: 3.3V CMOS logic compatible, 5V tolerant.

PSIOs[4]

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level			0.8	V		
Input Pin High Level	2.0			V		
Input Pin Leakage Current			1	µA		
Output Pin Low Level			0.4	V		I_{SINK} = 3mA
Output Pin High Level			15	V		Open Drain. External pull-up resistor to user supply
Output Pin High-Z leakage Current (PSIO pins only)			10	µA		
I/O Frequency			5	MHz		

Note 4: 3.3V/5.0V CMOS logic compatible, maximum rating of 15.0V

Gate Drivers

Parameter	Min.	Typ.	Max.	Units		Conditions
GH, GL Rise Time		17		ns		At 10-90% of full scale, 1nF C_{load}
GH, GL Fall Time		11		ns		
GH, GL Pull-Up On-State Output Resistance		4	5	Ω		
GH, GL Pull-Down On-State Output Resistance		2	2.5	Ω		
GH, GL Pull-Down Resistance in Off-Mode		50		kΩ		V_{CC} = VCCD = 0V.
Bootstrap diode forward resistance		9		Ω		@ 10mA
Minimum On Time		50		ns		1nF of gate capacitance
Minimum Off Time		125		ns		1nF of gate capacitance

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BLOCK DIAGRAM

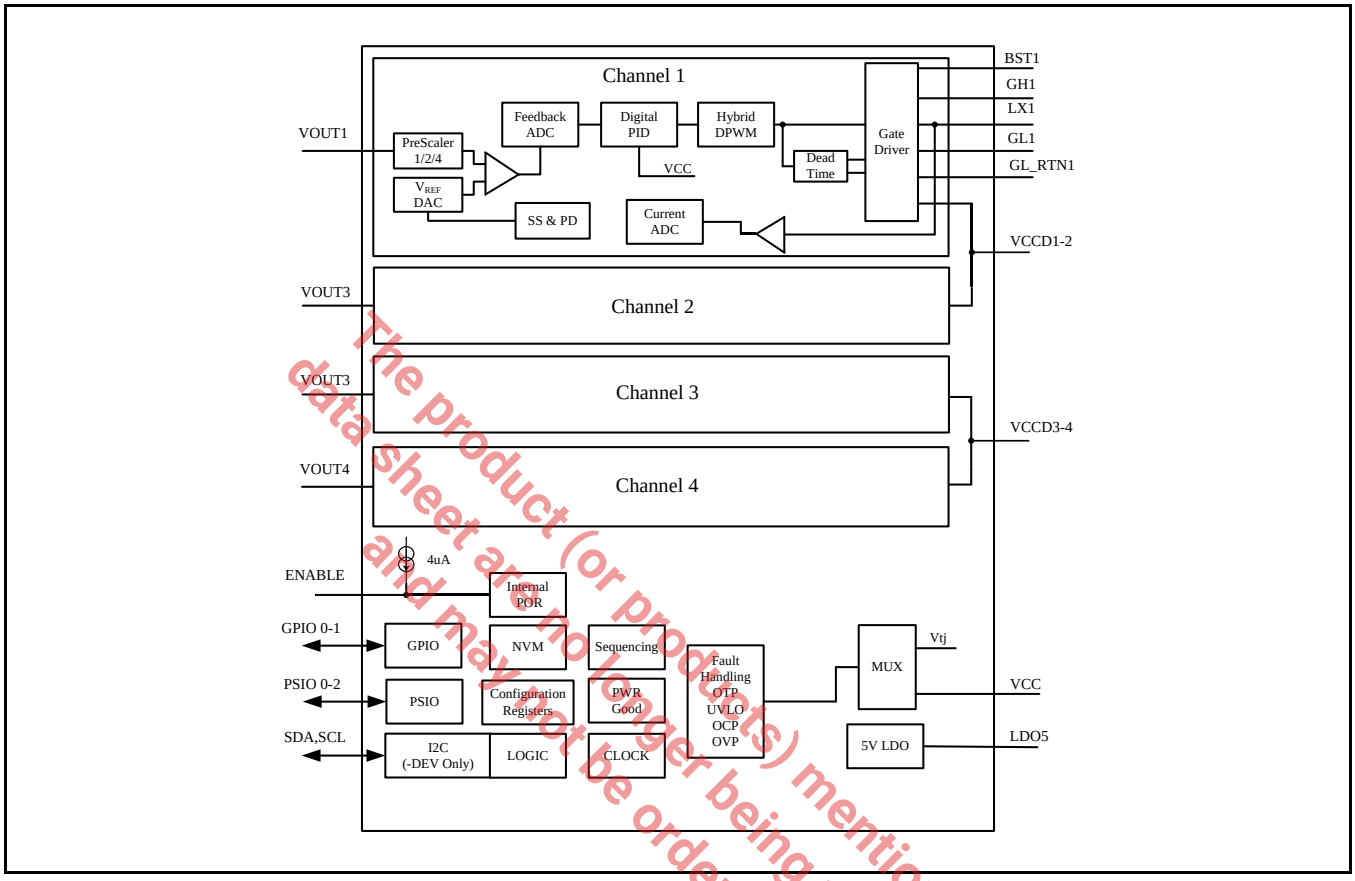


Figure 2 XRP7720 Block Diagram

LDO BLOCK DIAGRAM

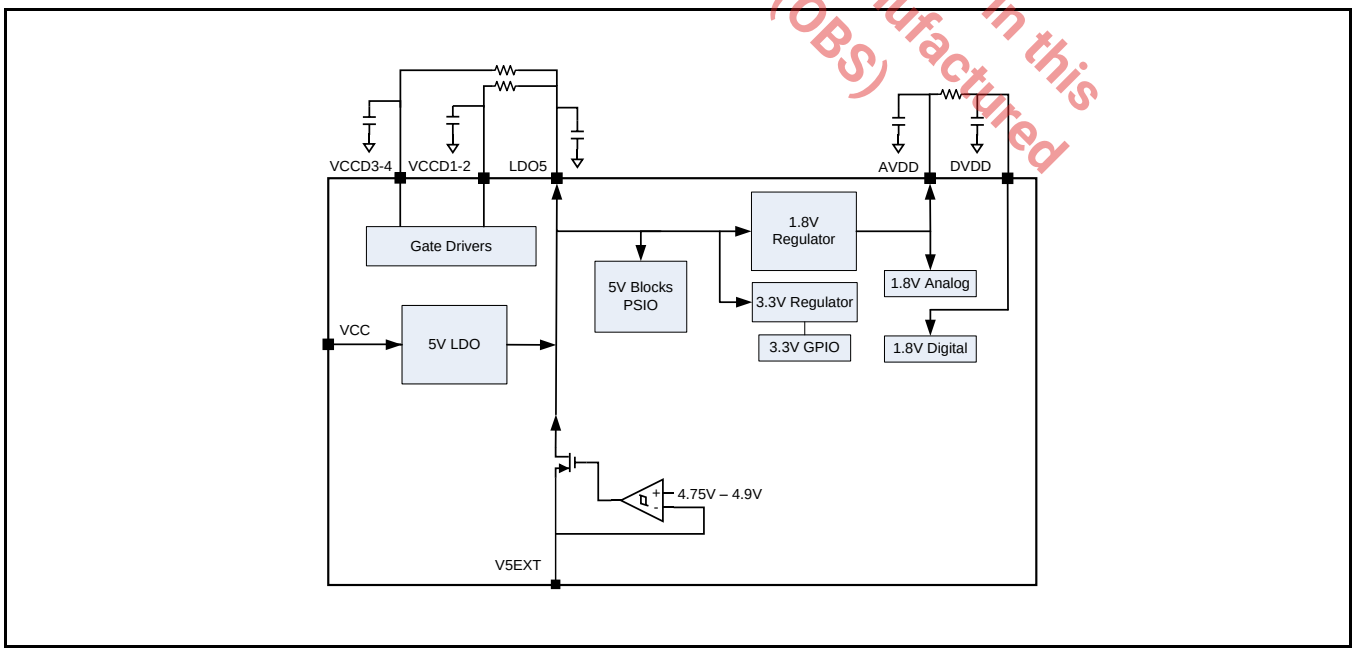
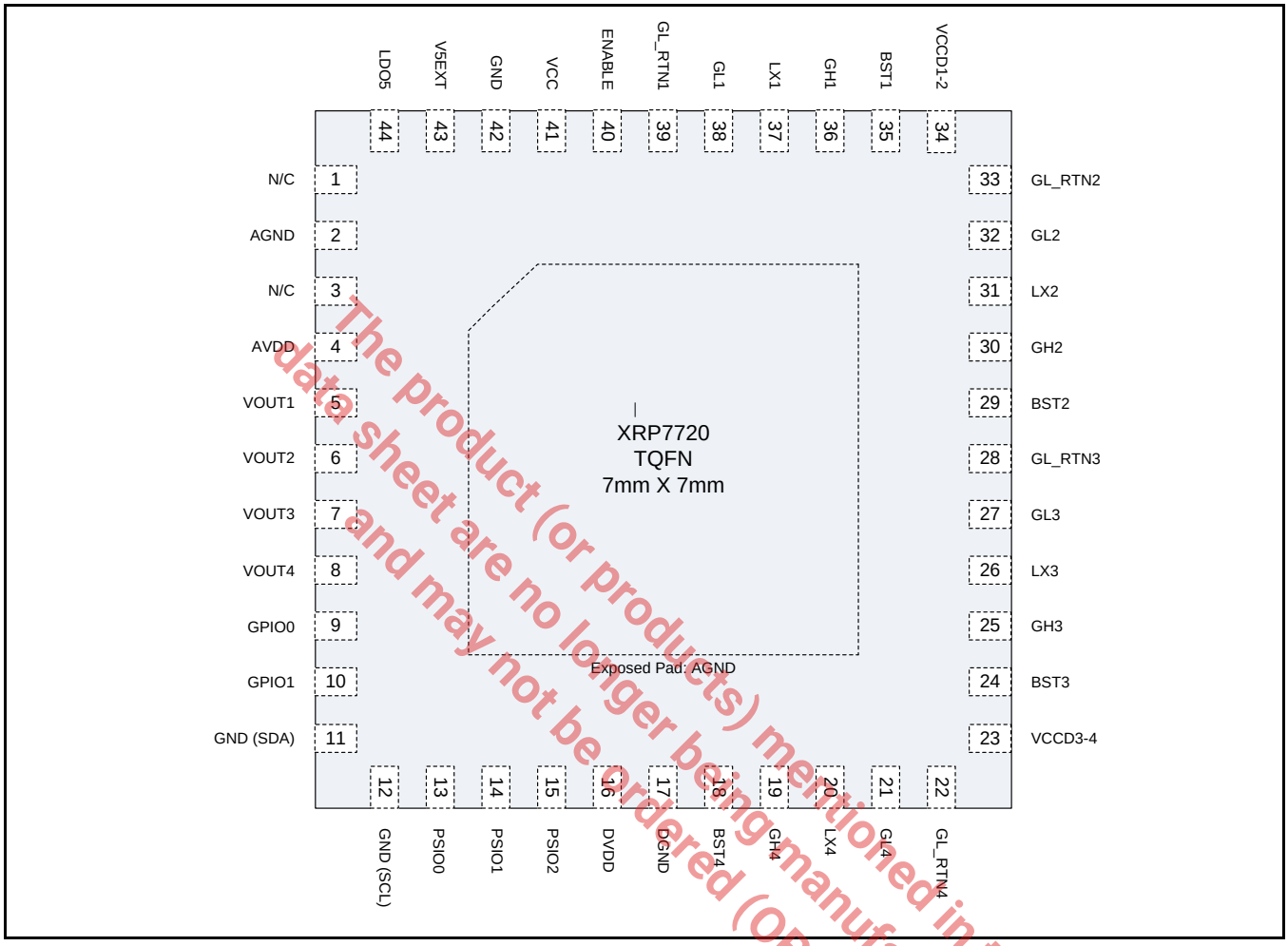


Figure 3 XRP7720 LDO Block Diagram

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PIN ASSIGNMENT



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Figure 4 XRP7720 Pin Assignment (-DEV ONLY)

PIN DESCRIPTION

Name	Pin Number	Description
V_{CC}	41	Input voltage. Place a decoupling capacitor close to the controller IC. This input is used in UVLO fault generation.
DVDD	16	1.8V supply input for digital circuitry. Connect pin to AVDD. Place a decoupling capacitor close to the controller IC.
VCCD1-2 VCCD3-4	23,34	Gate Drive supply. Two independent gate drive supply pins where pin 34 supplies drivers 1 and 2 and pin 23 supplies drivers 3 & 5. One of the two pins must be connected to the LDO5 pin to enable two power rails initially. It is recommended that the other VCCD pin be connected to the output of a 5V switching rail (for improved efficiency or for driving larger external FETs), if available, otherwise this pin may also be connected to the LDO5 pin. A bypass capacitor (>1uF) to PAD is recommended for each VCCD pin with the pin(s) connected to LDO5 with shortest possible length of etch.
AGND	2	Analog ground pin. This is the small signal ground connection.
GL_RTN1-4	39,33, 28,22	Ground connection for the low side gate driver. This should be routed as a signal trace with GL. Connect to the source of the low side MOSFET.
GL1-GL4	38,32, 27,21	Output pin of the low side gate driver. Connect directly to the gate of an external N-channel MOSFET.

Name	Pin Number	Description
GH1-GH4	36,30, 25,19	Output pin of the high side gate driver. Connect directly to the gate of an external N-channel MOSFET.
LX1-LX4	37,31, 26,20	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFETs and the inductor. These pins are also used to measure voltage drop across bottom MOSFETs in order to provide output current information to the control engine.
BST1-BST4	35,29, 24,18	High side driver supply pin(s). Connect BST to the external capacitor as shown in the Typical Application Circuit on page 2. The high side driver is connected between the BST pin and LX pin and delivers the BST pin voltage to the high side FET gate each cycle.
GPI0-GPIO1	9,10	These pins may be configured as inputs or outputs to implement custom flags, power good signals, enable/disable controls and synchronization to an external clock.
PSIO0-PSIO2	13,14,15	Open drain, these pins may be used to control external power MOSFETs to switch loads on and off, shedding the load for fine-grained power management. They may also be configured as standard logic outputs or inputs just as any of the GPIOs can be configured, but as open drains they will require an external pull-up when configured as outputs.
GND	11, 12	XRP7720ILB-XXXX-F. These pins should be tied to ground.
SDA, SCL	11,12	**XRP7720ILB-DEV-F Only.** SMBus/I^{2}C serial interface communication pins for communication to PowerArchitect™ 5.1 using XRP77XXEVB-XCM (Exar Configuration Module). Accommodation should be made in the board layout to tie these pins to ground for production.
VOUT1-VOUT4	5,6,7,8	Connect to the output of the corresponding power stage. The output is sampled at least once every switching cycle.
LDO5	44	Output of a 5V LDO. This is a micro power LDO that can remain active while the rest of the IC is in standby mode. This LDO is also used to power the internal Analog Blocks.
ENABLE	40	If ENABLE is pulled high or allowed to float high, the chip is powered up (logic is reset, registers configuration loaded, etc.). The pin must be held low for the XRP7720 to be placed into shutdown.
DGND	17	Digital ground pin. This is the logic ground connection, and should be connected to the ground plane close to the PAD.
V5EXT	43	External 5V that can be provided. If one of the output channels is configured for 5V, then this voltage can be fed back to this pin for reduced operating current of the chip and improved efficiency.
AVDD	4	Output of the internal 1.8V LDO. A decoupling capacitor should be placed between AVDD and AGND close to the chip.
PAD	45	This is the die attach paddle, which is exposed on the bottom of the part. Connect externally to the ground plane.
N/C	1,3,42	No Connect

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ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1
XRP7720ILB-DEV-F	-40°C≤T_J≤+125°C	XRP7720ILB YYWW Lot#	44-pin TQFN	Tray	Halogen Free
XRP7720ILBTR-XXXX-F*	-40°C≤T_J≤+125°C	XRP7720ILB YYWW Lot#		2.5K/Tape & Reel	Halogen Free
XRP7720EVB-DEMO-1	XRP7720EVB Power Board Only				
XRP7720EVB-DEMO-1-KIT	XRP7720EVB Power Board, USB Stick, XRP77XXEVB-XCM, USB Cable, Ribbon Connector				

"YY" = Year – "WW" = Work Week

*Minimum order requirements apply; please contact your Exar representative.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{CC} = 12V, T_J = T_A = 25°C, unless otherwise specified - Schematic and BOM from XRP7724EVB. See XRP7724EVB-DEMO-1 Manual.

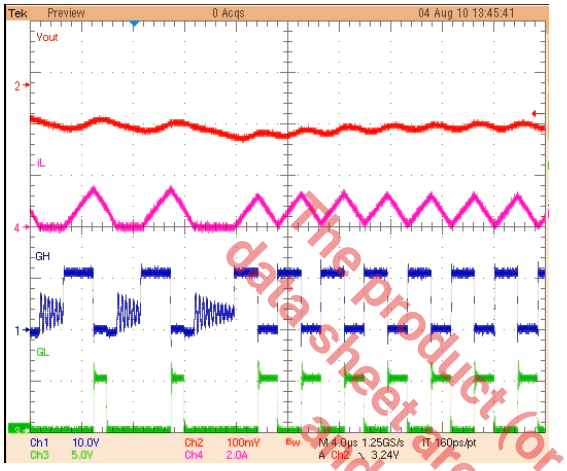


Figure 1 PFM to PWM Transition

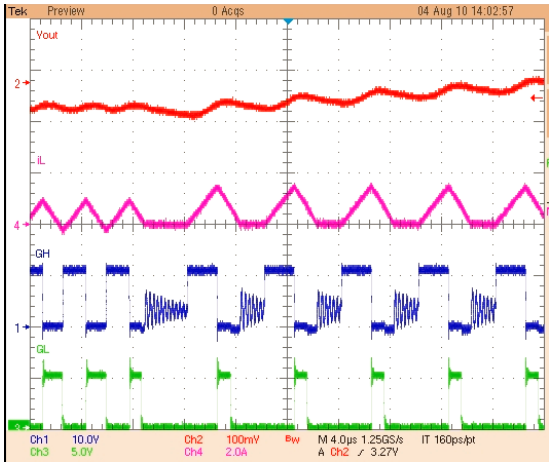


Figure 2 PWM to PFM Transition

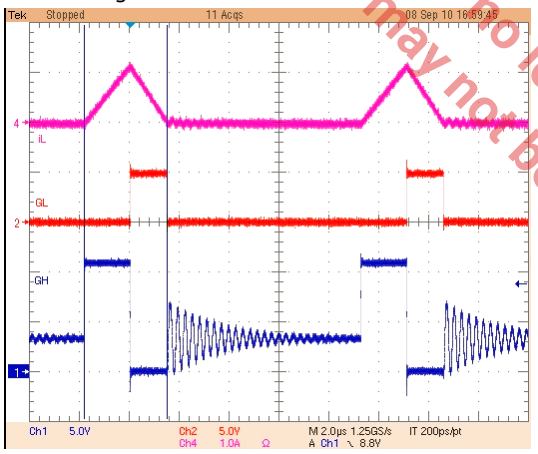


Figure 3 PFM Zero Current Accuracy

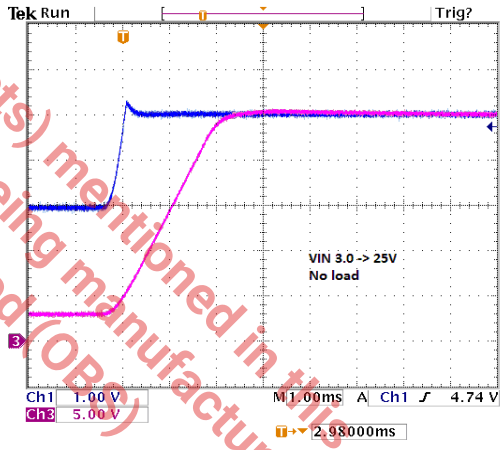


Figure 4 LDO5 Brown Out Recovery, No Load

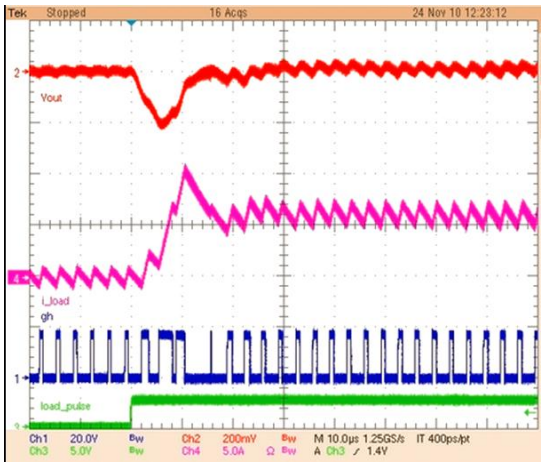


Figure 5 0-6A Transient 300kHz

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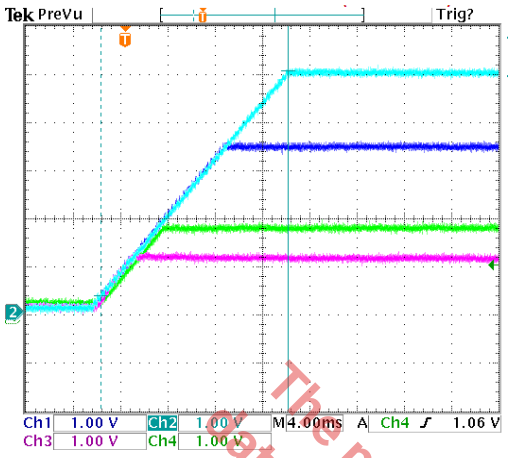


Figure 6 Simultaneous Start-up

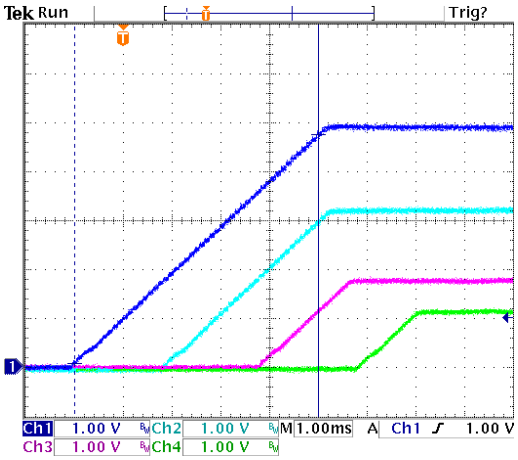


Figure 7 Sequential Start-up

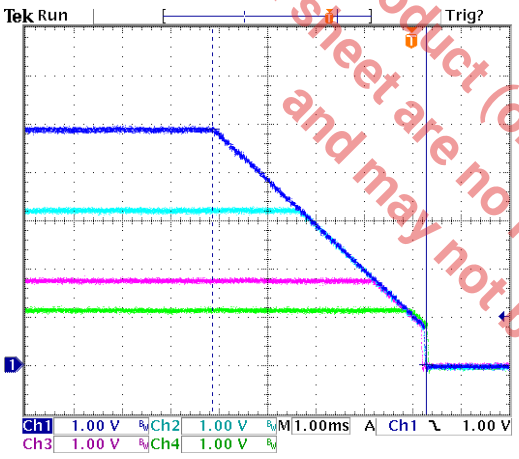


Figure 8 Simultaneous Shut Down

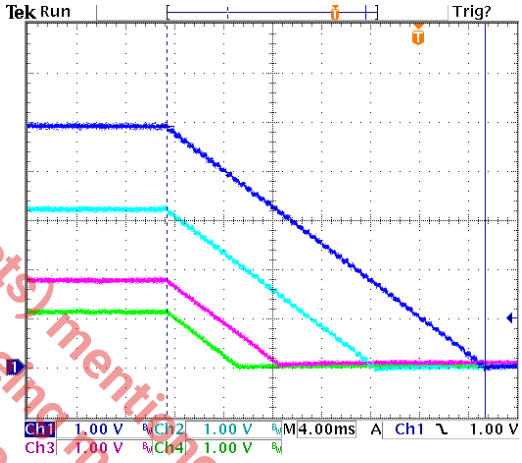


Figure 9 Sequential Shut Down

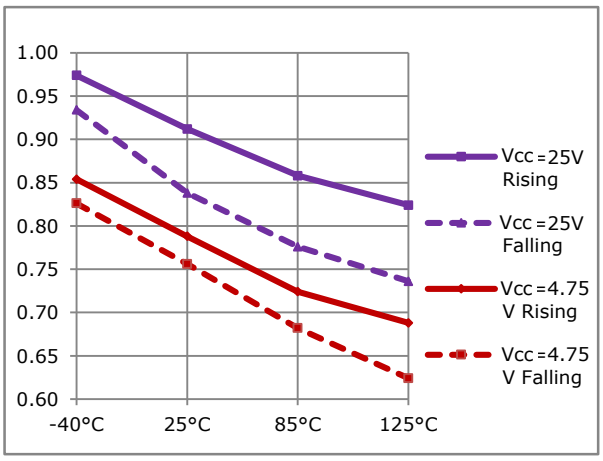


Figure 10 Enable Threshold Over Temp

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FUNCTIONAL OVERVIEW

The XRP7720 is a quad-output digital pulse width modulation (DPWM) controller with integrated gate drivers for use with synchronous buck switching regulators. Each output voltage can be programmed from 0.6V to 5.5V without the need for an external voltage divider. The wide range of programmable DPWM switching frequency (from 105 kHz to 1.2 MHz) enables the user to optimize for efficiency or component sizes. Since the digital regulation loop requires no external passive components, loop performance is not compromised due to external component variation or operating condition.

The XRP7720 provides a number of critical safety features, such as Over-Current Protection (OCP), Over-Voltage Protection (OVP), Over Temperature Protection (OTP) plus input Under Voltage Lockout (UVLO). In addition, a number of key health monitoring features including warning level flags for the safety functions and various Power Good (PGOOD) functions which may be configured to the GPIOs for hardware monitoring. The above are all programmable during the development phase through PA 5.1 when using the XRP7720ILB-DEV.

For hardware communication, the XRP7720 has two logic level General Purpose Input-Output (GPIO) pins, three 15V, open drain, Power System Input-Output (PSIO) pins, and an ENABLE pin. Two pins are dedicated to the SMBus data (SDA) and clock (SCL) which are available in the XRP7720ILB-DEV but are eliminated in the production version. If full dynamic control and telemetry are desired in the production system, the pin compatible XRP7724 is available.

In addition to providing four switching outputs, the XRP7720 also provides a stand-by linear regulator that produce 5V for a total of 5 customer usable supplies in a single device.

The 5V LDO is used for internal power and is also optionally available to power external circuitry. There is also a 1.8V linear regulator which is for internal use only and should not be used externally.

A key feature of the XRP7720 is its powerful power management and time to market capabilities through the use of the XRP7720ILB-DEV. During development, all four outputs are independently programmable which provides full control of the delay, ramp, and sequence during power up and power down. Additionally, this programmability allows control of the interaction of the outputs and power down in the event of a fault, including active ramp down of the output voltages to remove an output voltage as quickly as possible. The outputs may also be defined and controlled as groups.

The XRP7720ILB-DEV and standard XRP7720ILB-XXXX-F provide two different types of programmable memory. The XRP7720ILB-DEV has a rewritable Non-Volatile Flash Memory (NVFM) that allows multiple re-configurations during development. In production, the XRP7720ILB-XXXX-F is factory programmed in a one-time programmable memory.

The XRP7720 brings an extremely high level of functionality and performance to a programmable power system. Ever decreasing product budgets require the designer to quickly make good cost/performance tradeoffs to be truly successful. By incorporating four switching channels, an LDO, and internal gate drivers in a single package, the XRP7720 allows for extremely cost effective power system designs. The key cost factor to consider in cost tradeoffs is the flexibility of the XRP7720ILB-DEV during systems reliability testing. The programmable versatility of the XRP7720ILB-DEV along with the lack of hard wired and on board configuration components allows for minor and major changes during development to be made in circuit and on the board, by simply reprogramming with PA 5.1.

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THEORY OF OPERATION

CHIP ARCHITECTURE

REGULATION LOOPS

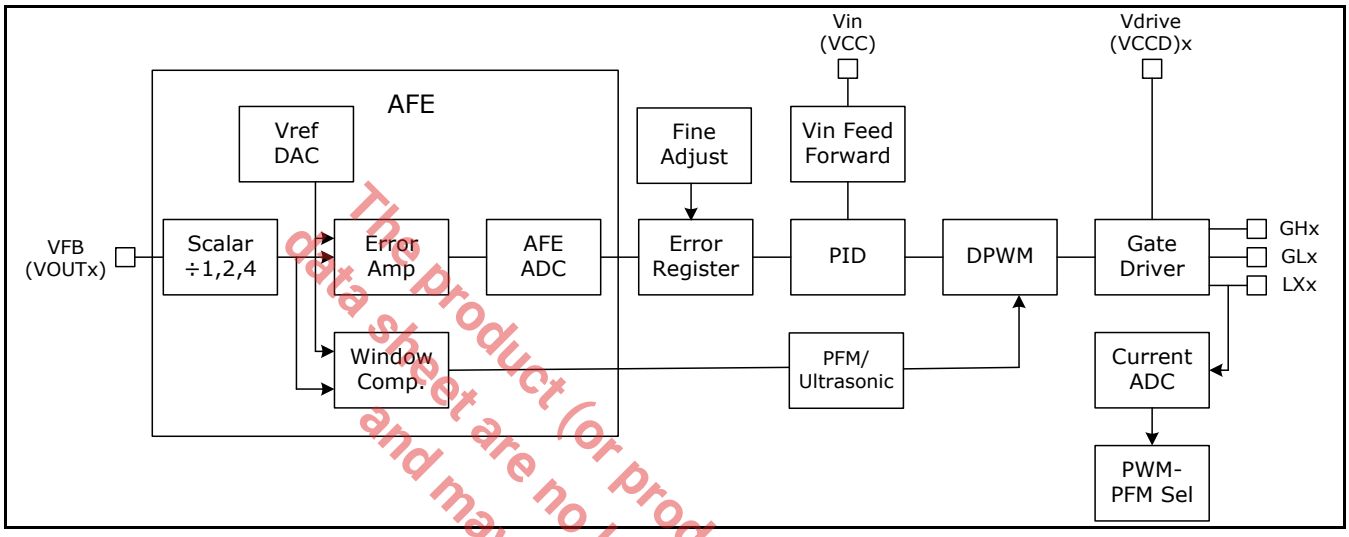


Figure 11 XRP7720 Regulation Loops

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Figure 11 shows a simplified functional block diagram of the regulation loops for one output channel of the XRP7720. There are 3 separate parallel control loops; Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), and Ultrasonic. Each of these loops is fed by the Analog Front End (AFE) as shown at the left of the diagram. The AFE consist of an input voltage scalar, a programmable Voltage Reference (Vref) DAC, Error Amplifier, and a window comparator. Some of the function blocks are common and shared by each channel by means of a multiplexer.

PWM Loop

The PWM loop operates in Voltage Control Mode (VCM) with optional Vin feed forward based on the voltage at the V_{CC} pin. The reference voltage (Vref) for the error amp is created by a 0.15V to 1.6V DAC that has 12.5mV resolution. In order to get a 0.6V to 5.5V output voltage range an input scalar is used to reduce feedback voltages for higher output voltages to bring them within the 0.15V to 1.6V control range. For output voltages up to 1.6V (low range) the scalar has a gain of 1. For output voltages from 1.6V to 3.2V (mid range) the scalar gain is 1/2 and for voltages greater than 3.2V (high range) the gain is 1/4. This results in the low range having an output voltage resolution of 12.5mV, mid range of 25mV and the high range having a resolution of 50mV. The error amp has a gain of 4 and compares the output voltage of the scalar to Vref to create an error voltage on its output. This is converted to a digital error term by the AFE ADC which is stored in the error register. The error register has a fine adjust function that can be used to improve the output voltage set point resolution by a factor of 5 resulting in a low range resolution of 2.5mV, mid range resolution of 5mV and a high range resolution of 10mV. The output of the error register is then used by the Proportional Integral Derivative (PID) controller to manage the loop dynamics.

The XRP7720 PID is a 17-bit five coefficient control engine that calculates the correct duty cycle under the various operating conditions and feeds it to the Digital Pulse Width Modulator (DPWM). Besides the normal coefficients, the PID also uses the Vin voltage to provide a feed forward function.

The XRP7720 DPWM includes a special delay timing loop that gives a timing resolution that is 16 times the master oscillator frequency (103MHz) for a timing resolution of 607ps for both the driver pulse width and dead time delays. The DWPM creates and drives the Gate High (GH) and Gate Low (GL) signals. The maximum and minimum on times and dead time delays are programmable by configuration resisters.

PFM mode loop

The XRP7724 has a PFM loop that can be enabled to improve efficiency at light loads. By reducing switching frequency and operating in the discontinuous conduction mode (DCM), both switching and I^2R losses are minimized.

Figure 12 shows a functional diagram of the PFM logic.

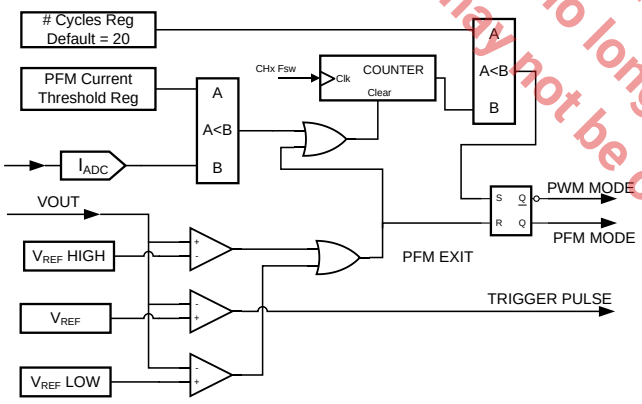


Figure 12 PFM Enter/Exit Functional Diagram

The PFM loop works in conjunction with the PWM loop and is entered when the output current falls below a programmed threshold level for a programmed number of cycles. When PFM mode is entered, the PWM loop is disabled and instead, the scaled output voltage is compared to Vref with a window comparator. The window comparator has three thresholds; normal (Vref), high (Vref + %high) and low (Vref - %low). The %high and %low values are programmable and track Vref.

In PFM mode, the normal comparator is used to regulate the output voltage. If the output voltage falls below the Vref level, the comparator is activated and triggers the DPWM to start a switching cycle. When the high side FET is turned on, the inductor current ramps up which charges up the output capacitors and increasing their voltage. After the completion of the high side and low side on-times, the lower FET is turned off to inhibit any inductor reverse current flow. The load current then discharges the output capacitors until the output voltage falls below Vref and the normal comparator is activated this then triggers the DPWM to start the next switching cycle. The time from the end of the switching cycle to the next trigger is referred to as the dead zone.

When PFM mode is initially entered the switching duty cycle is the same that it was in PWM mode. The result is the inductor ripple current will remain the same as it was in PWM mode. During operation the PFM duty cycle is calculated based on the ratio of the output voltage to V_{CC}. This method ensures that the output voltage ripple is well controlled and is much lower than in other architectures which use a "burst" methodology.

If the output voltage ever goes outside the high/low windows, PFM mode is exited and the PWM loop is reactivated.

Although the PFM mode does a good job in improving efficiency at light load, at very light loads the dead zone time can increase to the point where the switching frequency can enter the audio hearing range. When this happens some components, like the output inductor and ceramic capacitors, can emit audible noise. The amplitude of the noise depends mostly on the board design and on the manufacturer and construction details of the components. Proper selection of components can reduce the sound to very low levels. In general Ultrasonic Mode is not used unless required as it reduces light load efficiency.

Ultrasonic Mode

Ultrasonic mode is an extension of PFM to ensure that the switching frequency never enters the audible range. When this mode is entered, the switching frequency is set to 30kHz and the duty cycle of the upper and lower FETs, which are fixed in PFM mode, are decreased as required to keep the output

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voltage in regulation while maintaining the 30kHz switching frequency.

Under extremely light or zero load currents, the GH on time pulse width can decrease to its minimum width. When this happens, the lower FET on time is increased slightly to allow a small amount of reverse inductor to flow back into Vin to keep the output voltage in regulation while maintaining the switching frequency above the audio range.

INTERNAL DRIVERS

The internal high and low gate drivers use totem pole FETs for high drive capability. They are powered by two external 5V power pins (VCCD1-2) and (VCCD3-4), VCCD1-2 powers the drivers for channels 1 and 2 and VCCD3-4 powers channels 3 and 4. The drivers can be powered by the internal 5V LDO by connecting their power pins to the LDO5 output through an RC filter to avoid conducted noise back into the analog circuitry.

To minimize power dissipation in the 5V LDO, it is recommended to power the drivers from an external 5V power source either directly or by using the V5EXT input. Good quality 1uF to 4.7uF capacitors should be connected directly between the power pins to ground to optimize driver performance and minimize noise coupling to the 5V LDO supply.

The driver outputs should be connected directly to their corresponding output switching FETs, with the Lx output connected to the drain of the lower FET for the best current monitoring accuracy.

See ANP-32 "Practical Layout Guidelines for Power^{XR} Designs"

LDOs

The XRP7720 has an internal Low Drop Out (LDO) linear regulator that generates 5.0V (LDO5) for both internal and external use. Additionally it has a 1.8V regulator that supplies power for the XRP7720 internal circuits. Figure 3 shows a block diagram of the linear power supplies. LDO5 is the main power input to the device and is supplied by an external 5.5V to 18V (V_{CC}) supply. The output of LDO5 should be bypassed by a good quality capacitor connected between the pin and ground close to the device. The 5V output is used by the XRP7720 as a standby power supply and is also used to power the 3.3V and 1.8V linear regulators inside the chip and can also supply power to the 5V gate drivers. The total output current that the 5V LDO can provide is 100mA. The XRP7720 consumes approximately 20mA and the rest can be used by the gate drive currents. *During initial power up, the maximum external load should be limited to 30mA.*

The AVDD pin is the 1.8V regulator output and needs to be connected externally to the DVDD pin on the device. A good quality capacitor should be connected between this pin and ground close to the package.

For operation with a V_{CC} of 4.75V to 5.5V, the LDO5 output needs to be connected directly to V_{CC} on the board.

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CLOCKS AND TIMING

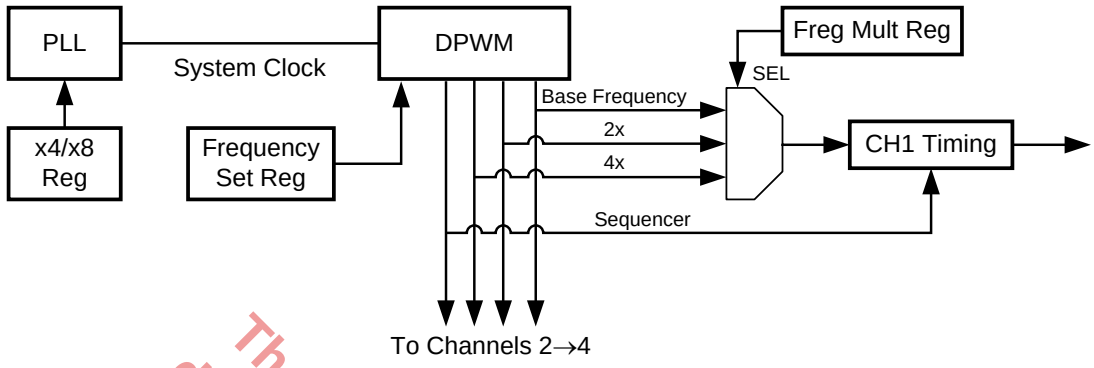


Figure 13 XRP7720 Timing Block Diagram

Figure 13 shows a simplified block diagram of the XRP7720 timings. Again, please note that the function blocks and signal names used are chosen for ease of understanding and do not necessarily reflect the actual design.

The system timings are generated by a 103MHz internal system clock (Sys_Clk). The basic timing architecture is to divide the Sys_Clk down to create a fundamental switching frequency (Fsw_Fund) for all the output channels that is settable from 105kHz to 306kHz. The switching frequency for a channel (Fsw_CHx) can then be selected as 1 times, 2 times or 4 times the fundamental switching frequency.

To set the base frequency for the output channels a "Fsw_Set" value representing the base frequency shown in Table 1, is entered into the switching frequency configuration register. Note that the Fsw_Set value is basically equal to the Sys_Clk divided by the base frequency. The system timings are then created by dividing down Sys_Clk to produce a base frequency clock, 2X and 4X times the base frequency clocks, and sequencing timing to position the output channels relative to each other. Each output channel then has its own frequency multiplier register that is used to select its final output switching frequency.

Table 1 shows the available channel switching frequencies for the XRP7720 device. In practice the PA 5.1 design tool handles all the details and the user only has to enter the fundamental switching frequency and the 1x, 2x, 4x frequency multiplier for each channel.

Base Frequency kHz	Available 2x Frequencies kHz	Available 4x Frequencies kHz
105.5	211.1	422.1
107.3	214.6	429.2
109.1	218.2	436.4
111.0	222.0	444.0
112.9	225.9	451.8
115.0	229.9	459.8
117.0	234.1	468.2
119.2	238.4	476.9
121.5	242.9	485.8
123.8	247.6	495.2
126.2	252.5	504.9
128.8	257.5	515.0
131.4	262.8	525.5
134.1	268.2	536.5
137.0	273.9	547.9
139.9	279.9	559.8
143.1	286.1	572.2
146.3	292.6	585.2
149.7	299.4	598.8
153.3	306.5	613.1
157.0	314.0	628.0
160.9	321.9	643.8
165.1	330.1	660.3
169.4	338.8	677.6
174.0	348.0	695.9
178.8	357.6	715.3
183.9	367.9	735.7
189.3	378.7	757.4
195.1	390.2	780.3
201.2	402.3	804.7
207.7	415.3	830.6
214.6	429.2	858.3
222.0	444.0	887.9
229.9	459.8	919.6
238.4	476.9	953.7
247.6	495.2	990.4
257.5	515.0	1030.0
268.2	536.5	1072.9
279.9	559.8	1119.6
292.6	585.2	1170.5
306.5	613.1	1226.2

Table 1

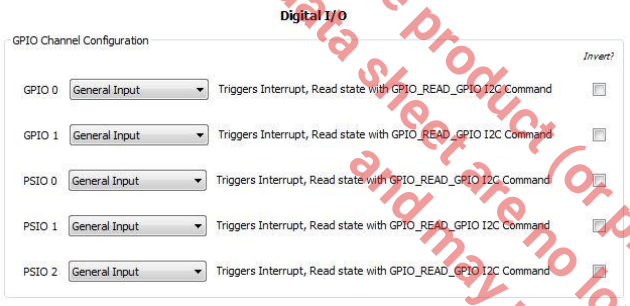
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SUPERVISORY AND CONTROL

Power system design with XRP7720 is accomplished using PowerArchitect™ design tool version 5.1 (PA 5.1). All figures referenced in the following sections are taken from PA 5.1.

DIGITAL I/O

XRP7720 has two General Purpose Input Output (GPIO) and three Power System Input Output (PSIO) user configurable pins.

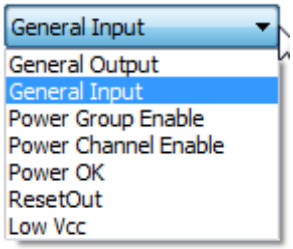


- GPIOs are 3.3V CMOS logic compatible and 5V tolerant.
- PSIO configured as outputs are open drain and require external pull-up resistor. These I/Os are 3.3V and 5V CMOS logic compatible, and up to 15V capable.

The polarity of the GPIO/PSIO pins is set in PA 5.1.

Configuring GPIO/PSIOs

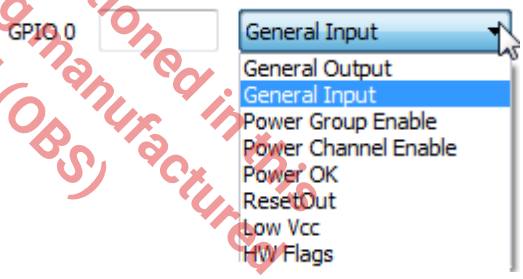
The following functions can be controlled from or forwarded to any GPIO/PSIO:



- **Power Group Enable** – controls enabling and disabling of Group 1 and Group 2
- **Power Channel Enable** – controls enabling and disabling of an individual channel.
- **Power OK** – indicates that selected channels have reached their target levels and have not faulted. Multiple channel selection is available in which case the resulting signal is the AND logic function of all channels selected
- **ResetOut** – is delayed Power OK. Delay is programmable in 1msec increments with the range of 0 to 255 msec
- **Low Vcc** – indicates when Vcc has fallen below the UVLO fault threshold and when the UVLO condition clears (Vcc voltage rises above the UVLO warning level)

Low Vcc, Power OK and ResetOut signals can only be forwarded to a single GPIO/PSIO.

In addition, the following are functions that are unique to GPIO0 and GPIO1.

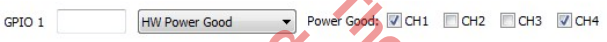


HW Flags – these are hardware monitoring functions forwarded to GPIO0 only. The functions include Under-Voltage Warning, Over- Temperature Warning, Over-Voltage Fault, Over-Current Fault and Over -Current Warning for every channel. Multiple selections will be combined using the OR logic function.

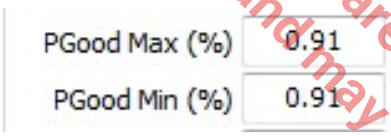


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- **HW Power Good** – the Power Good hardware monitoring function. It can only be forwarded to GPIO1. It is an output voltage monitoring function that is a hardware comparison of channel output voltage against its user defined Power Good threshold limits (Power Good minimum and maximum levels). It has no hysteresis. Multiple channel selections will be combined using the AND logic function of all channels selected.



- The Power Good minimum and maximum levels are expressed as percentages of the target voltage.



- "PGood Max" is the upper window and "PGood Min" is the lower window. The minimum and maximum for each of these values can be calculated with the following equation:

$$PGOOD(\%) = \frac{N * LSB(mV) * 10^5}{Vtarget\ (V)}$$

- Where N =1 to 63 for the PGOOD Max value and N=1 to 62 for the PGOOD Min value. For example, with the target voltage of 1.5V and set point resolution of 2.5mV (LSB), the Power Good min and max values can range from 0.17% to 10.3% and 0.17% to 10.5% respectively. A user can effectively double the range by changing to the next higher output voltage range setting, but at the expense of reduced set point resolution.

FAULT HANDLING

There are seven different types of fault handling:

- **Under Voltage Lockout (UVLO)** monitors voltage supplied to the Vcc pin and will cause the controller to shutdown all channels if the supply drops to critical levels.
- **Over Temperature Protection (OTP)** monitors temperature of the chip and will cause the controller to shutdown all channels if temperature rises to critical levels.
- **Over Voltage Protection (OVP)** monitors regulated voltage of a channel and will cause the controller to react in a user specified way if the regulated voltage surpasses threshold level.
- **Over Current Protection (OCP)** monitors current of a channel and will cause the controller to react in a user specified way if the current level surpasses threshold level.
- **Start-up Time-out Fault** monitors whether a channel gets into regulation in a user defined time period
- **LDO5 Over Current Protection (LDO5 OCP)** monitors current drawn from the regulator and will cause the controller to be reset if the current exceeds LDO5 limit (155mA typical)

UVLO

Both UVLO warning and fault levels are user programmable and set at 200mV increments in PA 5.1.



When the warning level is reached the controller will generate a flag if GPIO0 is so configured (see the Digital I/O section).

When an under voltage fault condition occurs the XRP7720 outputs are shut down. In addition, the host can be informed by forwarding the Low Vcc signal to any GPIO/PSIO (see the Digital I/O section). This signal transitions when the UVLO fault occurs.

Once the UVLO condition clears (Vcc voltage rises above or to the user-defined UVLO warning level) the Low Vcc signal will transition and the controller will be reset.

Special attention needs to be paid in the case when Vcc = LDO5 = 4.75V to 5.5V. Since the input voltage ADC resolution is 200mV the UVLO warning and fault set points are coarse

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for a 5V input. Therefore, setting the warning level at 4.8V and the fault level at 4.6V may result in the outputs not being re-enabled until a full 5.0V is reached on Vcc. Setting the warning level to 4.6V and the fault level at 4.4V will allow UVLO handing as desired. However, at a fault level below 4.6V, the device has a hardware UVLO on LDO5 to ensure proper shutdown of the internal circuitry of the controller. This means the 4.4V UVLO fault level will never occur.

OTP

User defined OTP warning, fault and restart levels are set at 5°C increments in PA 5.1.



When the warning level is reached the controller will assert HW Flags on GPIO0 (see the Digital I/O section).

When an OTP fault condition occurs, the XRP7720 outputs are shut down.

Once temperature reaches a user defined OTP Restart Threshold level, the controller will reset.

OVP

A user defined OVP fault level is set in PA 5.1 and is expressed in percentages of a regulated target voltage.



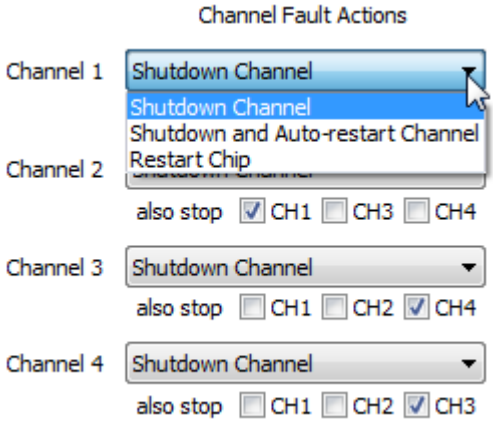
Resolution is the same as for the target voltage (expressed in percentages). The OVP minimum and maximum values are calculated by the following equation where the range for N is 1 to 63:

$$OVP(\%) = \frac{N * LSB(mV) * 10^5}{Vtarget\ (V)}$$

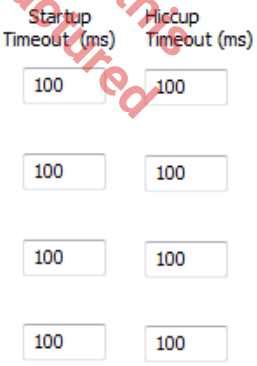
When the OVP level is reached and the fault is generated, it can be monitored through GPIO0.

A user can choose one of three options on how to react to an OVP event: to shutdown the faulting channel, to shut down faulting channel and perform auto-restart of the channel, or to restart the chip.

WARNING: Choosing the "Restart Chip" option during development is NOT recommended as it makes debug efforts difficult.



In the case of shutting down the faulting channel and auto-restarting, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 msec increments with a maximum value of 255 msec.



Note: The Channel Fault Action response is the same for either the OVP or OCP event.

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OCP

A user defined OCP fault level is set with 10mA increments in PA 5.1. PA 5.1 uses calculations to give the user the approximate DC output current entered in the current limit field. However the actual current limit trip value programmed into the part is limited to 280mV as defined in the electrical characteristics. The maximum value the user can program is limited by Rdson of the synchronous Power FET and current monitoring ADC range. For example, using a synchronous FET with Rdson of 30mΩ and wider ADC range the maximum current limit programmed would be:

$$OCP\ Max(A) = \frac{280mV}{30m\Omega} = 9.33A$$

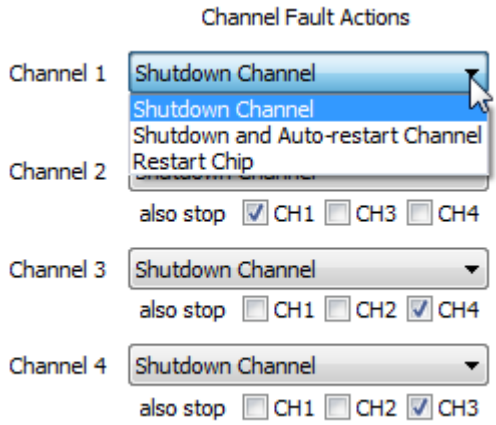
The current is sampled approximately 30ns before the low side MOSFET turns off so the actual measured DC output current in this example would be 9.33A plus approximately half the inductor ripple.

An OCP Fault is considered to have occurred only if the fault threshold has been tripped in four consecutive switching cycles. When the switching frequency is set to the 4x multiplier the current is sampled every other cycle. As a result it can take as many as 8 switching cycles for an over current event to be detected. When operating in 4x mode an inductor with a soft saturation characteristic is recommended.

In addition, OCP fault can be monitored through HW Flags on GPIO0. The OCP warning level is calculated by PA 5.1 as 85% of the OCP fault level.

A user can choose one of three options in response to an OCP event: shut down the faulting channel, shut down faulting channel and perform auto-restart of the channel, or restart the chip.

The output current reported by the XRP7720 is processed through a 7 sample median filter in order to reduce noise. The OCP limit is compared against unfiltered ADC output.



In the case of Shutdown and Auto-restart Channel the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 msec increments with a maximum value of 255 msec.

Note: The Channel Fault Action response is the same for either the OVP or OCP event.

Start-up Time-out Fault

A channel will be at Start-up Time-out Fault if it does not come-up in a time period specified in the "Startup Timeout" box. In addition a channel is at Start-up Timeout Fault if its pre-bias configuration voltage is within a defined value too close to the target.

LDO5 OCP

When current is drawn from the LDO5 that exceeds the LDO5 current limit the controller will be reset.

V5EXT SWITCHOVER

The V5EXT gives the user an opportunity to supply an external 5 Volt rail to the controller in order to reduce the controller's power dissipation. The 5 Volt rail can be an independent power rail present in a system or any of 7720 channels regulated to 5 Volts and routed back to the V5EXT pin. It is important to note that voltage to Vcc must be applied all the time even after the switchover, in which

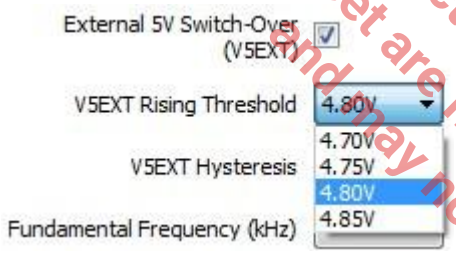
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case the current drawn from Vcc supply will be minimal.

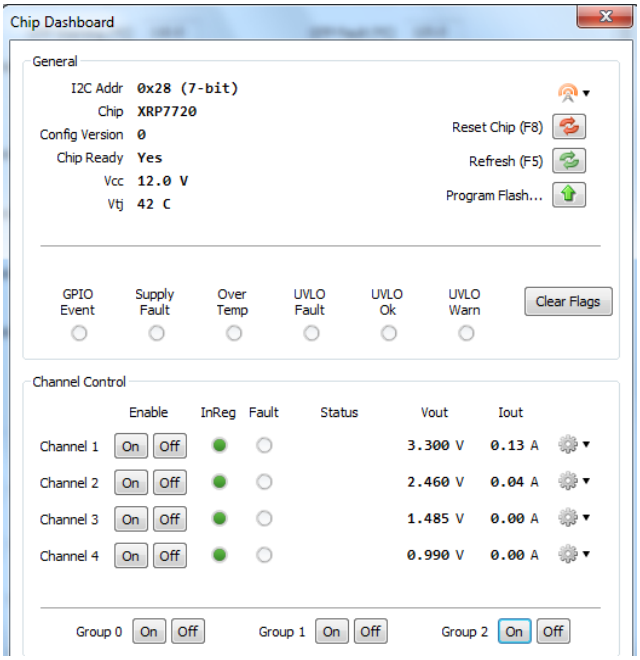
If the function is not used, it is recommended that the pin either be grounded or left floating. in conjunction, the function must be disabled through register settings.

V5EXT switchover control

The V5EXT function is enabled in PA 5.1. The switchover thresholds are programmable in 50mV steps with a total range of 200mV. The V5EXT switchover has a 150mV hysteresis. LDO5 automatically turns off when the external voltage is switched in and turns on when the external voltage drops below the lower threshold.



CHANNEL CONTROL



Channels can be controlled independently by any GPIO/PSIO. Channels will start-up or shut-down following transitions of signals applied to GPIO/PSIOs set to control the channels. In development, using the XRP7720ILB-DEV and PA 5.1, control can always be overridden.

Regardless of whether the channels are controlled independently or are in a group the ramp rates will be followed as specified (see the Power Sequencing section).

POWER SEQUENCING

All four channels can be grouped together and will start-up and shut-down in a user defined sequence.

Selecting none means channel(s) will not be assigned to any group and therefore will be controlled independently.

Group Selection



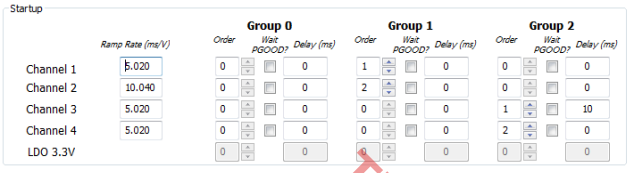
There are three groups:

- **Group 0** – is controlled by the chip ENABLE. Channels assigned to this group will come up with the ENABLE signal being high (plus an additional delay needed to load configuration from Flash to runtime registers), and will go down with the ENABLE signal being low.
  Since it is recommended to leave the ENABLE pin floating in the applications when Vcc = LDO5 = 4.75V to 5.5V, please contact Exar for how to configure the channels to come up at the power up in this scenario.
- **Group 1** – can be controlled by any GPIO/PSIO. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group.
- **Group** 2 – can be controlled by any GPIO/PSIO. Channels assigned to this group will start-up or shut-down following

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transitions of a signal applied to the GPIO/PSIO set to control the group.

Start-up



For each channel within a group a user can specify the following start-up characteristics:

- **Ramp Rate** – expressed in milliseconds per Volt.
- **Order** –position of a channel to come-up within the group
- **Wait PGOOD**? – selecting this option for a channel means the next channel in the order will not start ramping-up until this channel reaches the target level and its Power Good flag is asserted.
- **Delay** – an additional time delay a user can specify to postpone a channel start-up with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0 msec to 255 msec.

Shut-down



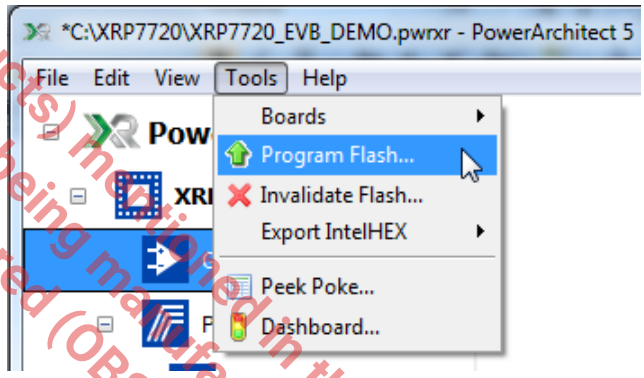
For each channel within a group a user can specify the following shut-down characteristics:

- **Ramp Rate** – expressed in milliseconds per Volt.
- **Order** –position of a channel to come-down within the group
- **Wait Stop Thresh**? – selecting this option for a channel means the next channel in the order will not start ramping-down until this channel reaches the Stop Threshold level. The stop threshold level is fixed at 600mV.
- **Delay** – additional time delay a user can specify to postpone a channel shut-down with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0 msec to 255 msec.

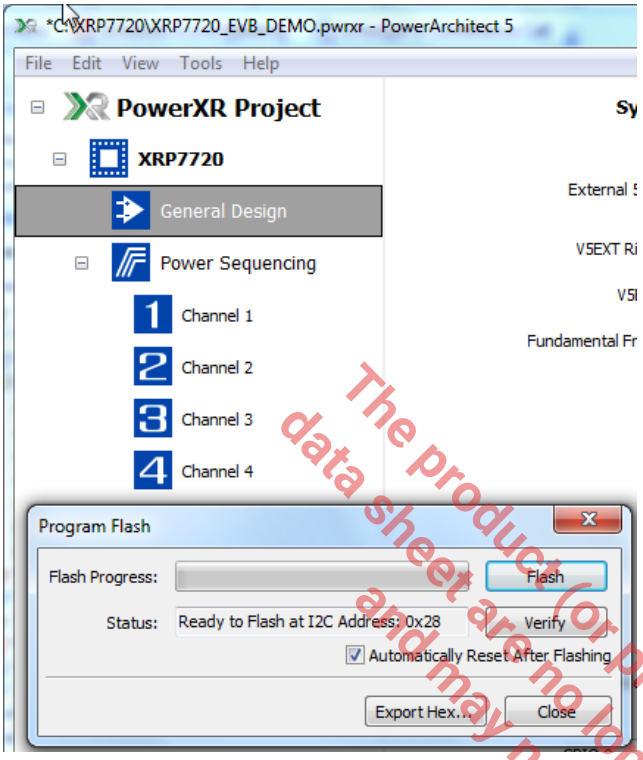
PROGRAMMING XRP7720

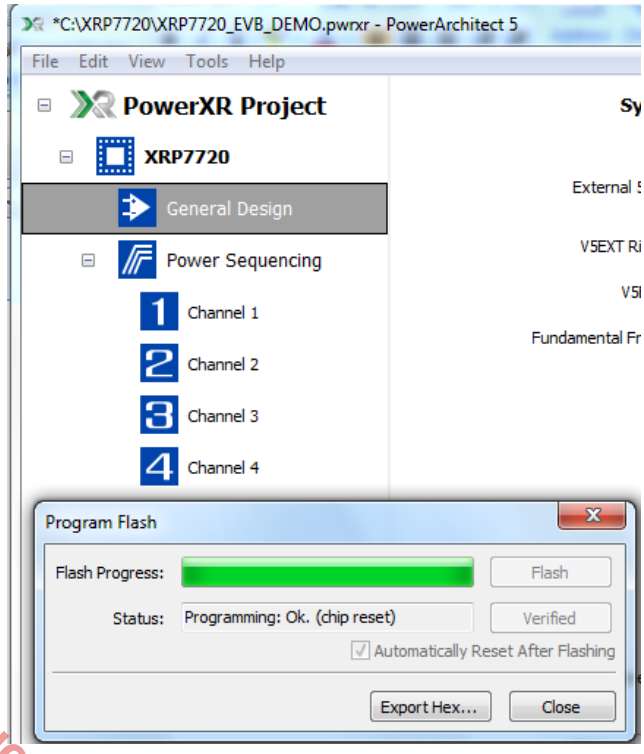
XRP7720ILB-DEV is a FLASH based device which means its configuration can be programmed into FLASH NVM and re-programmed a number of times. The purpose of this feature is to provide a means to fast development times.

Programming of FLASH NVM is done through PA 5.1.



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By clicking on the Flash button the user will start programming sequence of the design configuration into the Flash NVM. After the programming sequence completes the chip will reset (if automatically reset After Flashing box is checked) and boot the design configuration from the Flash.

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ENABLING XRP7720

XRP7720 has a weak internal pull-up ensuring it gets enabled as soon as internal voltage supplies have ramped up and are in regulation.

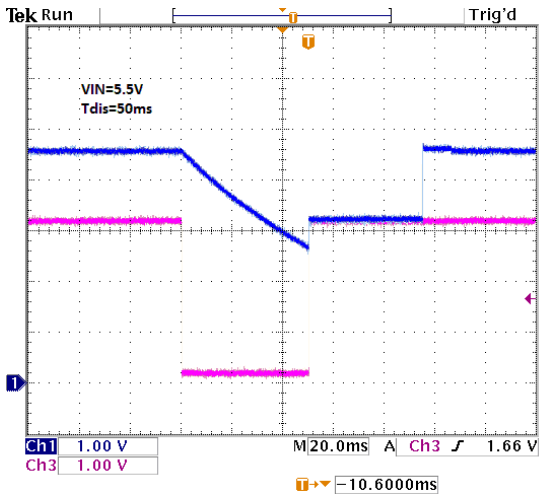
Driving the Enable pin low externally will keep the controller in the shut-down mode. A simple open drain pull down is the recommended way to shut the XRP7720 down.

If the Enable pin is driven high externally to control the XRP7720 coming out of the shut-down mode care must be taken to ensure the Enable pin is driven high after Vcc gets supplied to the controller.

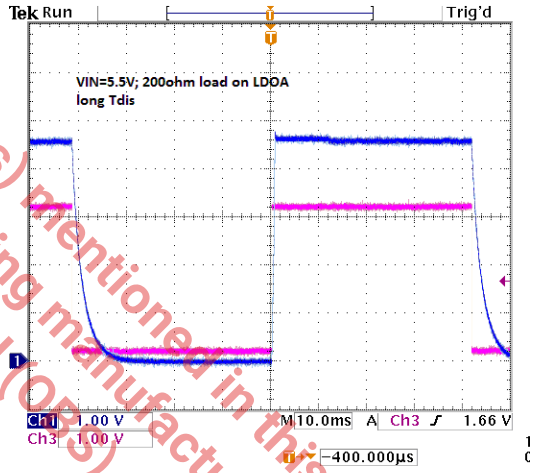
In the configuration, when Vcc = LDO5 = 4.75V to 5.5V, disabling the device by grounding the Enable pin is not recommended. It is recommended to leave the Enable pin floating and place the controller in the "Standby Mode" instead in this scenario. The standby mode is defined as the state when all switching channels are disabled, all GPIO/PSIOs are programmed as inputs, and system clock is disabled. In this state chip consumes 440uA typical.

Short duration Enable pin toggled low

Short duration shutdown pulses to the ENABLE pin of the XRP7720, which does not provide sufficient time for the LDO5 voltage to fall below 3.5V, can result in significant delay in re-enabling of the device. Some examples below show LDO5 and ENABLE pins:



No load on LDO5, blue trace. Recovery time after ENABLE logic high is approximately 40ms.



Adding a 200 ohm load on LDO5 pulls voltage below 3.5V and restart is short.

Note that as V_{CC} increases, the restart time falls as well. 5.5V input is shown as the worst case.

Since the ENABLE pin has an internal current source, a simple open drain pull down is the recommended way to shut down the XRP7720. A diode in series with a resistor between the LDO5 and ENABLE pins may offer a way to more quickly pull down the LDO5 output when the ENABLE pin is pulled low.

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APPLICATION INFORMATION

THERMAL DESIGN

As a 4 channel controller with internal MOSFET drivers and 5V gate drive supply all in one 7x7mm 44pin TQFN package, there is the potential for the power dissipation to exceed the package thermal limitations. The XRP7720 has an internal LDO which supplies 5V to the internal circuitry and MOSFET drivers during startup. It is generally expected that either one of the switching regulator outputs is 5V or another 5V rail is available in the system and connected to the 5VEXT pin. If there is no 5V available in the system, then the power loss will increase significantly and proper thermal design becomes critical. For lower power levels using properly sized MOSFETs and the use of the internal 5V regulator as a gate drive supply is considered appropriate.

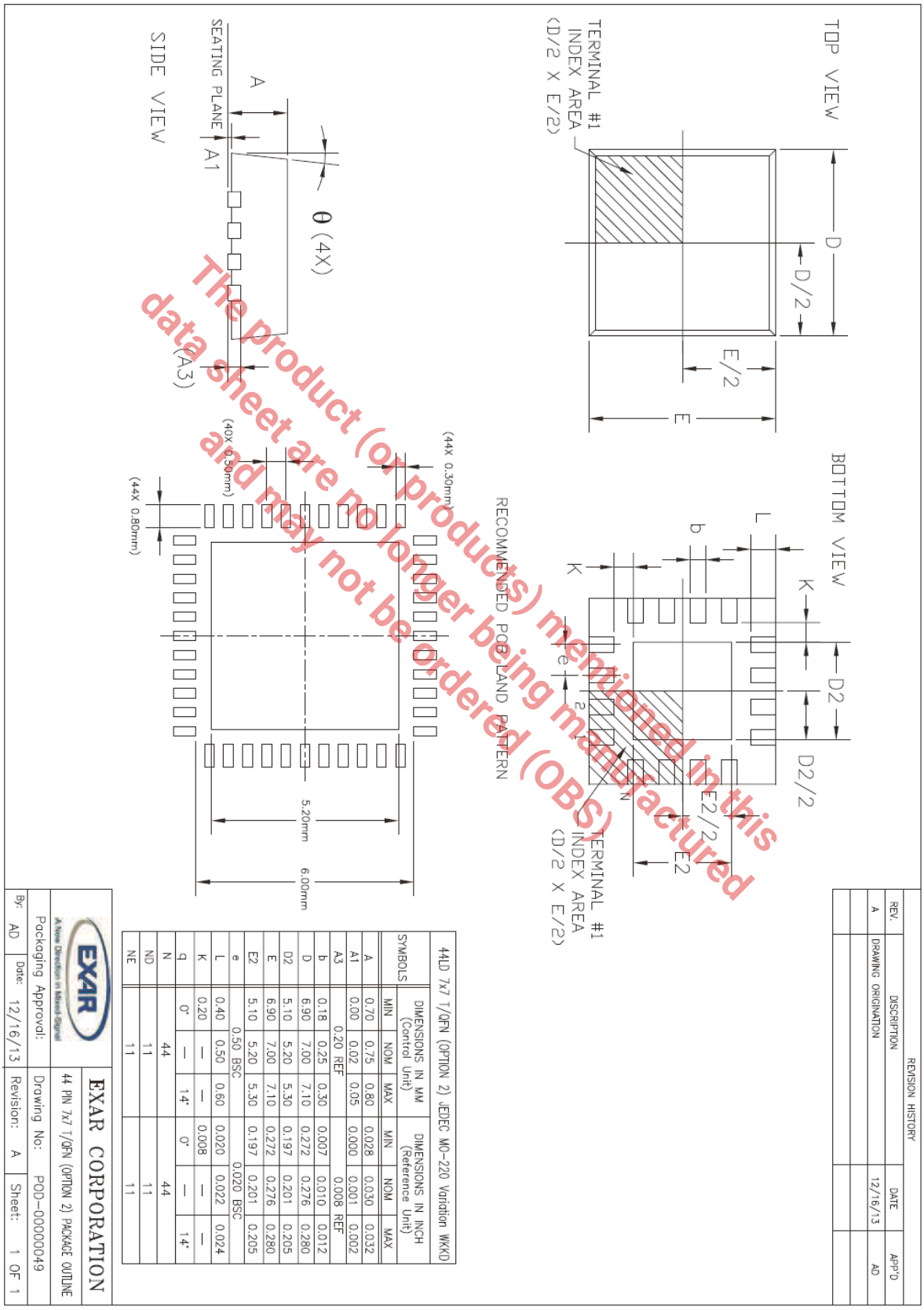
LAYOUT GUIDELINES

Refer to application note ANP-32 "Practical Layout Guidelines for Power^{XR} Designs", as well as ANP-35 for routing long distance gate drive traces.

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PACKAGE SPECIFICATION

44-PIN 7X7MM TQFN



44LD 7x7 T/QFN (OPTION 2) JEDEC MO-220 Variation WKKD

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	6.90	7.00	7.10	0.272	0.276	0.280
D2	5.10	5.20	5.30	0.197	0.201	0.205
E	6.90	7.00	7.10	0.272	0.276	0.280
E2	5.10	5.20	5.30	0.197	0.201	0.205
e		0.50 BSC			0.020 BSC	
L	0.40	0.50	0.60	0.020	0.022	0.024
K	0.20	—	—	0.008	—	—
q	0°	—	14°	0°	—	14°
N		44			44	
ND		11			11	
NE		11			11	

EXAR CORPORATION

44 PIN 7x7 T/QFN (OPTION 2) PACKAGE OUTLINE

Packaging Approval:		Drawing No:	POD-00000049	
By: AD	Date: 12/16/13	Revision: A	Sheet: 1	OF 1

ECN: 1351-12 12/17/2013

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REVISION HISTORY

Revision	Date	Description
1.0.0	01/31/2014	Initial Release [ECN: 1406-02]

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