MxL7080

URX800/URX600 Power Manager
Data Sheet

General Description

The MxL7080 is a power manager specifically designed to interface with the MaxLinear's AnyWAN™ SoC URX800/600 series and PUMA™ 8 DOCSIS 4.0 SoC. The I²C interface and sideband signals to the SoC enable all required power system controls and adaptive power management. The MxL7080 device also handles all start-up sequencing and fault management including three fault flag outputs to control system regulators during cold reset and fault events.

The MxL7080 controls four MxL76500 regulators to provide the CPU0, CPU1, ADP, and ROC power rails for the SoC. The interface to the MxL76500 regulators controls sequencing, output voltage, and fault monitoring. DVS control is achieved through four DAC outputs driving the reference inputs of the regulators which range from 0.6V to 1.0V with a resolution of 5mV.

The MxL7080 operates from a nominal 3.3V rail. Fault detection features include MxL76500 regulator monitoring, DAC short circuit, and input undervoltage lockout (UVLO). The MxL7080 is available in a 4mm × 4mm 32-pin QFN package.

Features

- Input voltage from 3V to 3.6V
- Four DAC outputs
- Output voltage from 0.6V to 1.0V
- 1% DAC accuracy
- Dynamic voltage scaling
- Power Good indicator
- SoC serial interface
- SoC sideband signals
- Input undervoltage lockout
- DAC short circuit detection
- 4mm × 4mm QFN package

Applications

- DOCSIS 4.0 modems and gateways
- Fiber optics home gateway unit (HGU)
- Ethernet Wi-Fi home router
- DSL/G.fast home gateway
- Fixed wireless access (FWA) home gateway

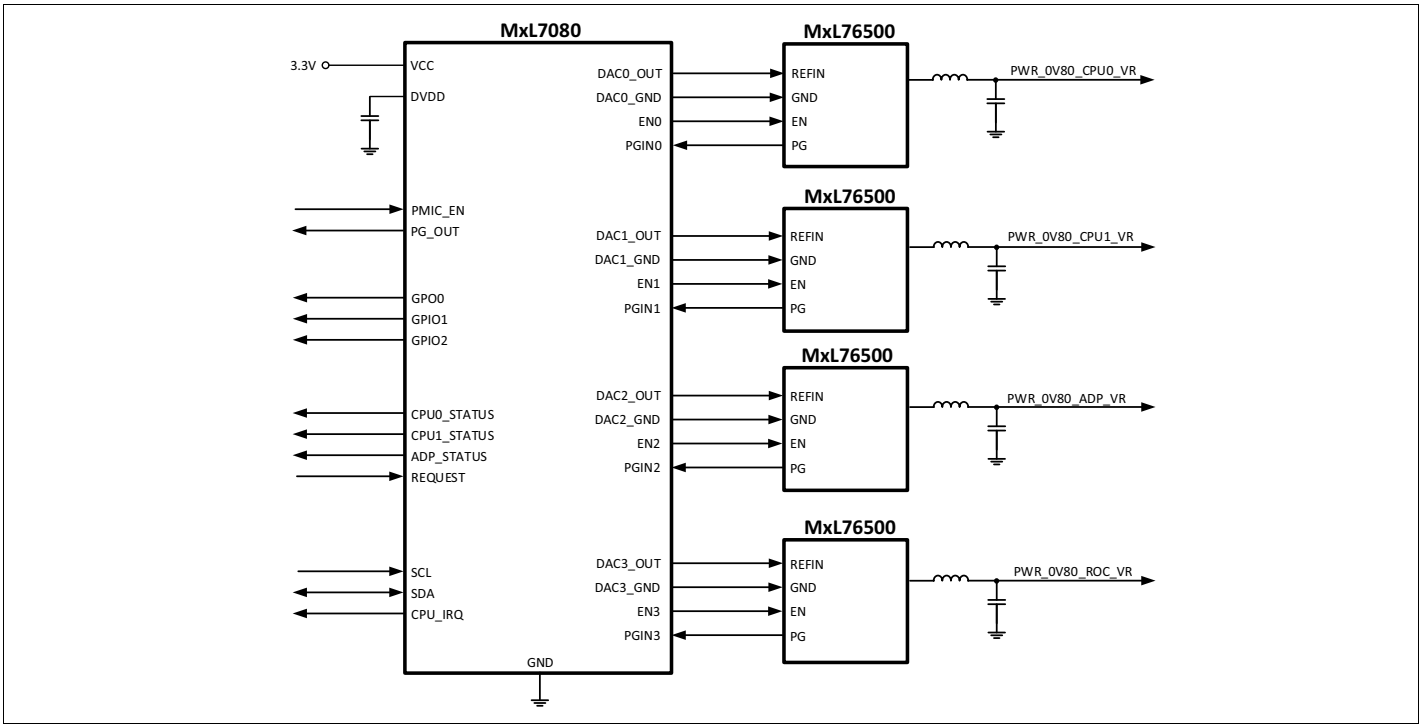

Figure 1: Typical Application Schematic

Revision History

Document No.	Release Date	Change Description
257DSR02	October 23, 2025	**Updated:** ■ MxL7670 replaced with MxL76500. ■ "General Description" section. ■ "Features" section. ■ "Typical Application Schematic" figure. ■ "Absolute Maximum Ratings" table. ■ "Operating Conditions" table. ■ "Electrical Characteristics" table. ■ "Pin Information" section. ■ "Top Level Block Diagram" figure. ■ "Functional Description" section. ■ "Routing Recommendations from MxL7080 to MxL7670 to SoC" figure. ■ "Ordering Information" section. **Added:** ■ "OTP Default Configuration" section. ■ "I^2C Interface" section. ■ "Register Map" section.
257DSR01	February 27, 2024	Initial final release.

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Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under Table 1 may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under Table 1 or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above what is listed under Table 2 for extended periods of time may affect device reliability. The solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard. The thermal resistance profile is based on the *JEDEC EIA /JESD51- (2A, 8, 29)* standards.

Table 1: Absolute Maximum Ratings

Parameters	Conditions	Minimum	Maximum	Units
V_{CC} Supply Voltage	-	–0.3	4	V
DVDD Pin Voltage	Apply no external voltage	–0.3	1.7	V
DACx_OUT	-	–0.3	2	V
ENx, FAULT0, FAULT1, FAULT2, CPU0_STATUS, CPU1_STATUS, ADP_STATUS, CPU_IRQ, REQUEST	-	–0.3	4	V
SCL, SDA, PMIC_EN	-	–0.3	4	V
Storage Temperature	-	-	150	°C
Junction Temperature	Storage temperature	–40	150	°C

ESD Ratings

Table 2: ESD Ratings

Parameter	Value	Units
Human Body Model (HBM)	±2000	V
Charged Device Model (CDM)	±500	V

Operating Conditions

Table 3: Operating Conditions

Parameter	Minimum	Maximum	Units
V_{CC} Supply Voltage	3.0	3.6	V
DACx_OUT	0	1.0	V
ENx, FAULT0, FAULT1, FAULT2, CPU0_STATUS, CPU1_STATUS, ADP_STATUS, CPU_IRQ, REQUEST	0	3.6	V
Ambient Temperature Range (T_a)	–40	85	°C

Electrical Characteristics

Specifications are for operating ambient temperature T_a = 25°C only. Limits applying over the full operating temperature of T_a = –40°C to 85°C are denoted by a "•". Unless otherwise noted, V_{CC} = 3.3V.

Table 4: Electrical Characteristics

Symbol	Parameter	Conditions	Temp	Min	Typ	Max	Units
Input Supply							
V_{CC}	VCC Input Voltage Range	-	•	3.0	-	3.6	V
I_Q	VCC Quiescent Currrent	PMIC_EN = 3.3V	•		450	600	µA
I_{Q_SD}	Shutdown Input Supply Current	PMIC_EN = 0V		-	200	-	µA
V_{DVDD}	DVDD Output Voltage	-		-	1.5	-	V
UVLO and Over Voltage Detection							
V_{CC_UVLO}	VCC Input Under Voltage Rising Threshold	-		-	2.5	-	V
$UVLO_{HYST}$	Input Under Voltage Hysteresis	-		-	100	-	mV
V_{VCC_OV}	VCC Over Voltage Detection	-		-	4	-	V
DAC Outputs							
V_{DAC}	DAC Voltage Range	-	•	0	-	1.0	V
$VDAC_{ACC}$	DAC Output Voltage DC Accuracy	-	•	–1	-	1	%
VID_{res}	VID Step Resolution	-			5	-	mV
MAX_VID	DAC Maximum VID	-		600	-	1000	mV
Slew Rate_SS	Slew Rate during Soft Start	-	-	2.5	-	20	mV/µs
$I_{LEAKAGE\_DAC}$	DAC Output Leakage Current	-		-	100	-	nA
I_{DAC_SC}	DAC Short Circuit Current	-		-	-	10	mA
Input and Output Pin Characteristics							
$V_{IH\_PMIC\_EN}$	PMIC_EN Input High Voltage	-		3.0	-	-	V
$V_{IL\_PMIC\_EN}$	PMIC_EN Input Low Voltage	-		-	-	0.7	V
$V_{IH\_REQUEST}$	REQUEST Input High Voltage	-		3.0	-	-	V
$V_{IL\_REQUEST}$	REQUEST Input Low Voltage	-		-	-	0.7	V
V_{OH}	CPU0_STATUS, CPU1_STATUS, ADP_STATUS, CPU_IRQ Output High Voltage	-		3.0	-	-	V
V_{OL}	CPU0_STATUS, CPU1_STATUS, ADP_STATUS, CPU_IRQ Output Low Voltage	-		-	-	0.7	V
V_{OL_PG}	PG Output Low Voltage	Sink current = 1mA		-	-	0.4	V
V_{OL_FAULTx}	FAULT0, FAULT1, FAULT2 Output Low Voltage	Sink current = 1mA		-	-	0.4	V
Timing							
$t_{EN\_DAC\_DELAY}$	Delay from ENx high transition to start of DACx_OUT ramp	-		-	0.6	-	ms
t_{RAIL_TIMING}	Timing between subsequent rail power up and down	-		-	1	-	ms
$t_{FLT\_RECOVERY\_DELAY}$	Time between a fault response and restart attempt	-		-	1.5	-	s
t_{CRD}	Cold Reset Recovery Delay	-		-	1.5	-	s
t_{PG_TIMING}	Delay to PG state change when not initiated by a fault	-		-	1	-	ms
t_{PG_DELAY}	Delay to PG rising after all outputs are in regulation	-		-	50	-	µs

Pin Information

Pin Configuration

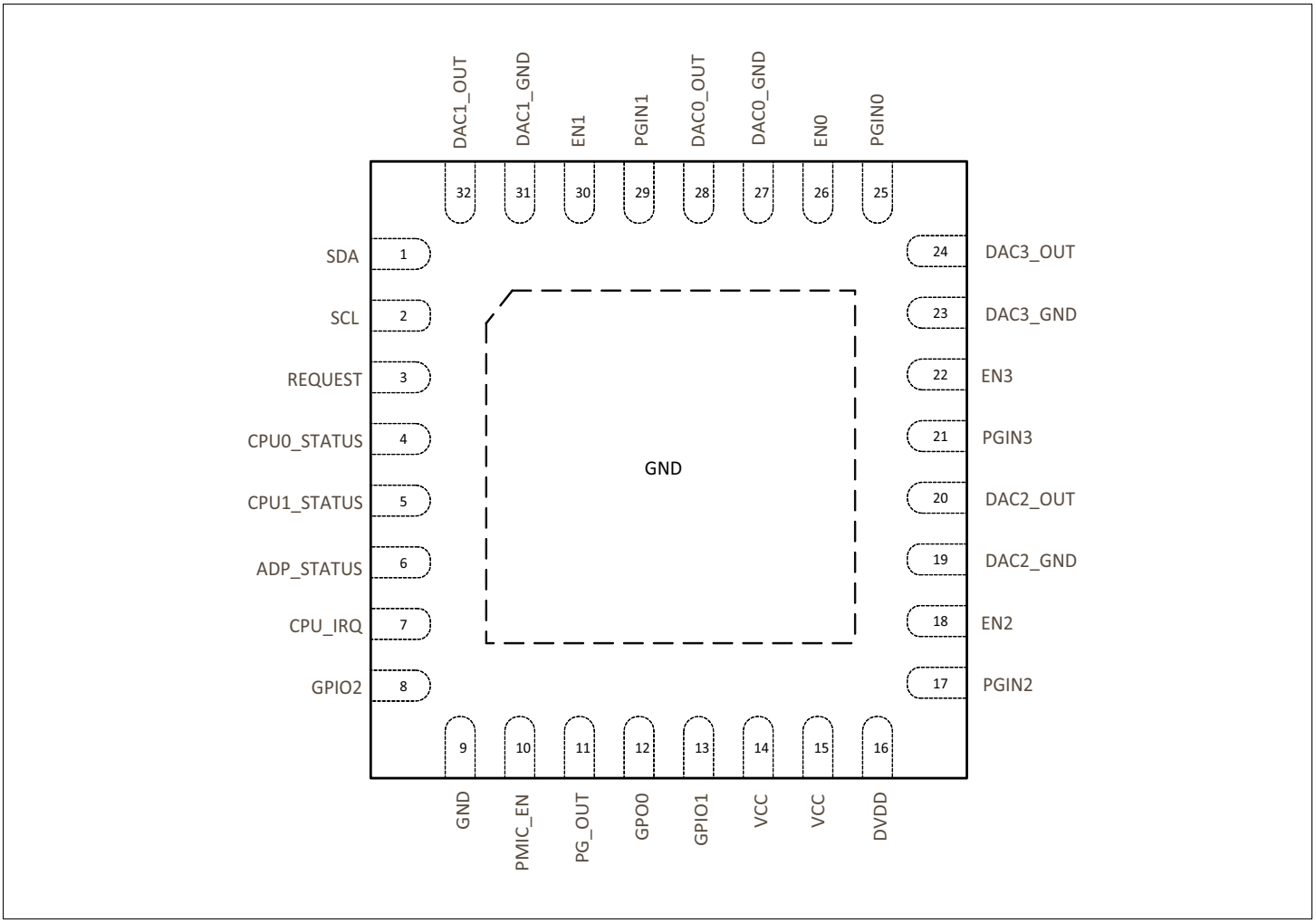


Figure 2: Pin Configuration—4mm × 4mm QFN (Top View)

Pin Description

Table 5: Pin Description

Pin Name	Pin Number	Description
SDA	1	Serial interface data, open drain.
SCL	2	Serial interface clock, open drain.
REQUEST	3	Input from CPU which triggers entry into low power mode (LPM), cold off, cold reset, or DVS of one or more outputs. Ensures proper timing with the CPU of these actions.
CPU0_STATUS	4	Status signal output for the CPU0 rail. This signal is asserted high when the output voltage is within the tolerance of the final voltage during a DVS.
CPU1_STATUS	5	Status signal output for the CPU1 rail. This signal is asserted high when the output voltage is within the tolerance of the final voltage during a DVS. This signal also goes high when the device enters LPM and toggles low when it exits LPM.
ADP_STATUS	6	Status signal output for the ADP rail. This signal is asserted high when the output voltage is within the tolerance of the final voltage during a DVS.
CPU_IRQ	7	Device interrupt output to the CPU indicating erroneous request conditions.
GPIO2	8	Open-drain output. The GPIO pins pull low in the event of a fault or during a cold reset, whereby they remain low for 1.5 seconds. During cold boot, these pins remain open so as not to interfere with the normal sequencing of the power system.
GND	9	Ground.
PMIC_EN	10	Input from a platform regulator to the device that initiates the cold boot sequence of the four CPU rails when toggled from low to high.
PG_OUT	11	Device open-drain PGOOD indicator for all four DAC outputs combined.
GPO0	12	Open-drain output. The GPO pins pull low in the event of a fault or during a cold reset, whereby they remain low for 1.5 seconds. During cold boot, these pins remain open so as not to interfere with the normal sequencing of the power system.
GPIO1	13	Open-drain output. The GPIO pins pull low in the event of a fault or during a cold reset, whereby they remain low for 1.5 seconds. During cold boot, these pins remain open so as not to interfere with the normal sequencing of the power system.
VCC	14, 15	Input power supply to the device. The VCC pin supplies DVDD.
DVDD	16	Internal 1.5V digital supply. Connect a 1µF decoupling capacitor to ground.
PGIN2	17	PGOOD input from the ADP rail VR. This input is ignored when DAC2_OUT is <500mV
EN2	18	Input to the ADP rail VR EN pin. Enables the regulator and transitions between DCM and FCCM levels during a DVS. This pin provides tri-level values (0V Off, 1.65V FCCM, 3.3V DCM) for the respective modes of operation.
DAC2_GND	19	DAC output2 ground pin. Connect this pin to the AGND pin of the ADP rail VR. DAC2_OUT and DAC2_GND must be routed as a differential pair to the VR.
DAC2_OUT	20	DAC output of the device that provides the reference to the ADP rail VR.
PGIN3	21	PGOOD input from the ROC rail VR. This input is ignored when DAC3_OUT is <500mV.
EN3	22	Input to the ROC rail VR EN pin. Enables the regulator and transitions between DCM and FCCM levels during a DVS. This pin provides tri-level values (0V Off, 1.65V FCCM, 3.3V DCM) for the respective modes of operation.
DAC3_GND	23	DAC output3 ground pin. Connect this pin to the AGND pin of the ROC VR. DAC3_OUT and DAC3_GND must be routed as a differential pair to the VR.
DAC3_OUT	24	DAC output of the device that provides the reference to the ROC rail VR.
PGIN0	25	PGOOD input from the CPU0 rail VR. This input is ignored when DAC0_OUT is <500mV.

Table 5: Pin Description (Continued)

Pin Name	Pin Number	Description
EN0	26	Input to the CPU0 rail VR EN pin. Enables the regulator and transitions between DCM and FCCM levels during a DVS. This pin provides tri-level values (0V Off, 1.65V FCCM, 3.3V DCM) for the respective modes of operation.
DAC0_GND	27	DAC output0 ground pin. Connect this pin to the AGND pin of the CPU0 rail VR. DAC0_OUT and DAC0_GND must be routed as a differential pair to the VR.
DAC0_OUT	28	DAC output of the device that provides the reference to the CPU0 rail VR.
PGIN1	29	PGOOD input from the CPU1 rail VR. This input is ignored when DAC1_OUT is <500mV.
EN1	30	Input to the CPU1 rail VR EN pin. Enables the regulator and transitions between DCM and FCCM levels during a DVS. This pin provides tri-level values (0V Off, 1.65V FCCM, 3.3V DCM) for the respective modes of operation.
DAC1_GND	31	DAC output1 ground pin. Connect this pin to the AGND pin of the CPU1 rail VR. DAC1_OUT and DAC1_GND must be routed as a differential pair to the VR.
DAC1_OUT	32	DAC output of the device that provides the reference to the CPU1 rail VR.
GND	PADDLE	Ground. Connect to pin 9.

Typical Performance Characteristics

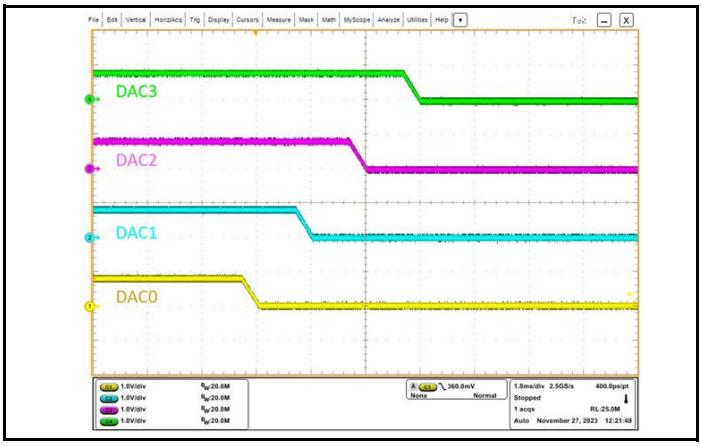


Figure 3: Cold Off—DAC#_OUT Outputs

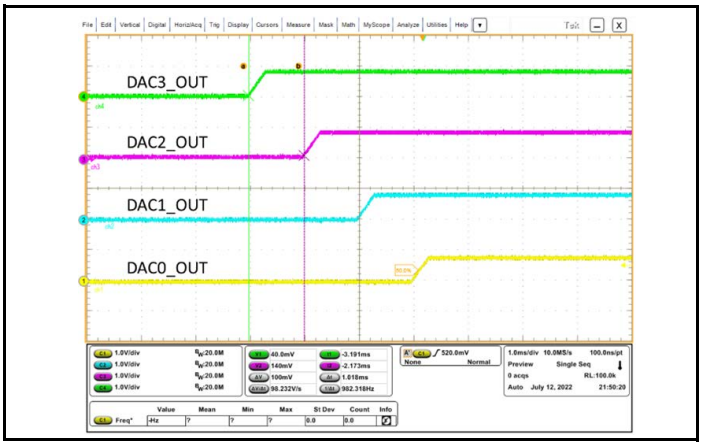


Figure 4: Cold Boot—DAC#_OUT Outputs

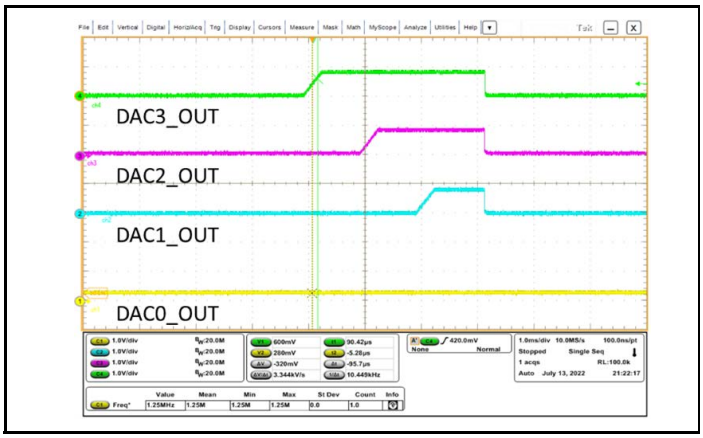


Figure 5: Cold Boot—Fault Response to DAC0 Shorted to GND

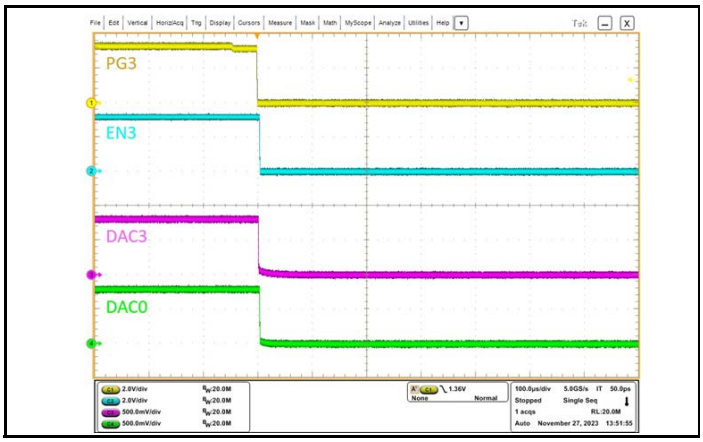


Figure 6: Cold Boot—Fault Response to MxL76500 PG Low

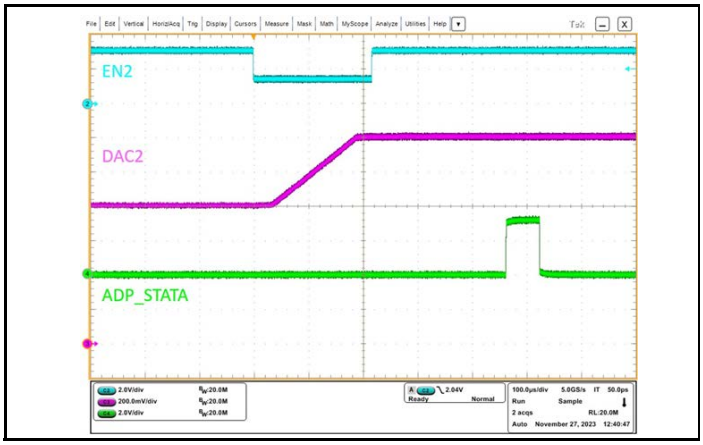


Figure 7: DVS Up

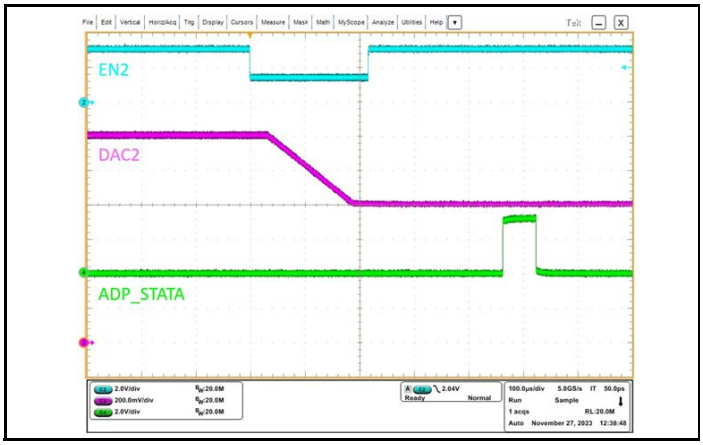


Figure 8: DVS Down

Block Diagram

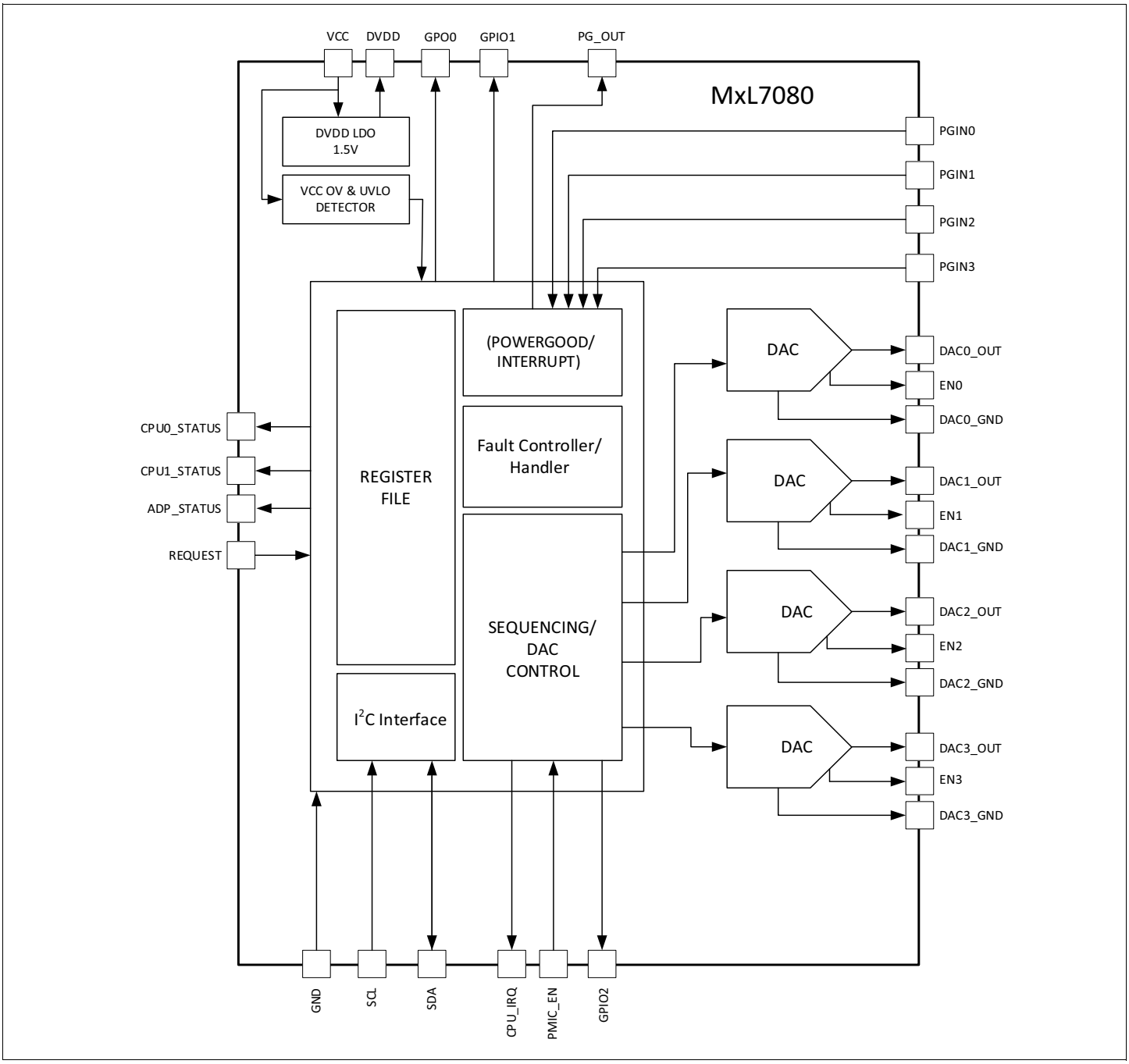


Figure 9: Top Level Block Diagram

Functional Description

Overview

The MxL7080 power manager is designed to interface between MaxLinear's URX8xx/6xx and MxL256xx AnyWAN™ and PUMA™ 8 SoCs and four MxL76500 step-down synchronous buck regulators providing power to the CPU0, CPU1, ADP, and ROC power domains. There are three primary interfaces integrating the MxL7080 into the system: an I^2C interface and five sideband signals communicating with the SoC, an interface to the four MxL76500 regulators and for system integration and control a PMIC_EN, PG_OUT, and three GPIO pins.

This disintegrated approach versus an all-in-one PMIC minimizes thermal challenges while providing single stage power conversion from standard 12V inputs. Other solutions are targeted to lower power systems where CPU0, CPU1, ADP, and ROC are 2.2A, 2.2A, 1.5A, and 3.2A respectively. The combination of the MxL7080 and four MxL76500 support full power operation where those outputs are 3.5A, 3.5A, 3A, and 4.2A

SoC Interface

The I^2C interface between the MxL7080 and the SoC communicates dynamic voltage scaling (DVS) commands, power state changes, and polling of certain status bits within the MxL7080. It can operate at either 400kHz or 1MHz and is qualified with the SoCs to meet the I^2C timing requirements which can be unique to the SoC. The I^2C interface is 1.8V compatible, 3.3V tolerant, and requires pullup resistors to operate as expected.

The SoC interface also includes a number of sideband IOs. These are active outputs, and no pullup resistors are required.

- CPU0_STATUS, CPU1_STATUS, and ADP_STATUS toggle high for ~62ms approximately 250ms after DVS command is complete, and the output has settled to the new value.
- CPU1_STATUS also outputs high when the system acknowledges a low power mode (LPM) command is given. It outputs low when the LPM exists.
- CPU_IRQ device interrupt to the SoC indicating erroneous request conditions different requests at the same time.
- REQUEST is a timing signal for the MxL7080 to execute an action predetermined by the SoC through a prior I^2C write. Those actions include: enter LPM, execute a cold off, or execute a cold reset. The SoC also can dynamically change the polarity of the REQUEST signal.

MxL76500 Regulator Interface

The interface to the MxL76500 regulators consists of:

- An EN# output which enables the regulator and changes its operation state between low power mode (LPM) and forced continuous conduction mode (FCCM). FCCM is used during DVS commands.
- A DAC#_OUT output which connects to the regulators REF_IN pin to control the regulators output voltage.
- A DAC#_GND which is routed as a differential pair with DAC#_OUT and connected to the regulators AGND pin.
- A PGIN# input which monitors for faults on the regulator as indicated by the regulators PG_OUT pin.

Figure 10 shows how these signals operate between the MxL7080 and MxL76500 during a normal start-up. For more details on power good lower threshold values for V_PG_THL and VP_PG_HYS, refer to the *MxL76500 Data Sheet* (261DS).

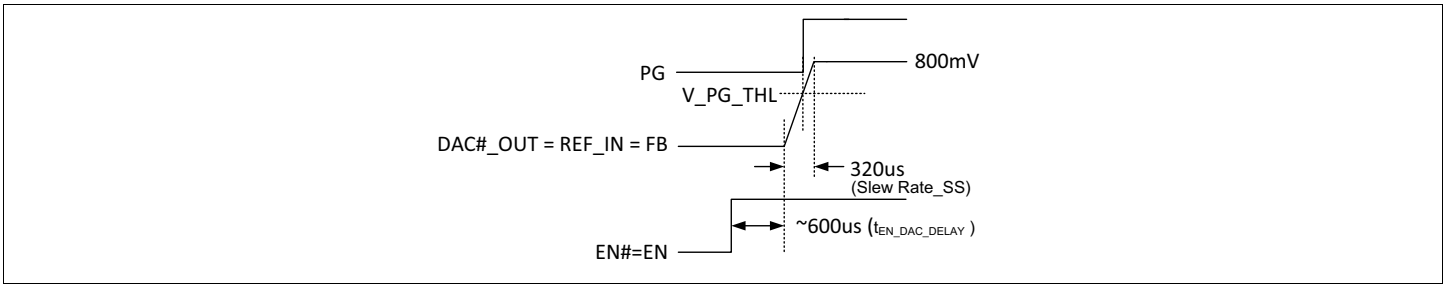


Figure 10: MxL7080 and MxL76500 Signals during Startup

During a normal shut down, the EN# pin drives to 1.5V which puts the MxL76500 into FCCM which enables the device to sink current from the output cap and drive the output to 0V.

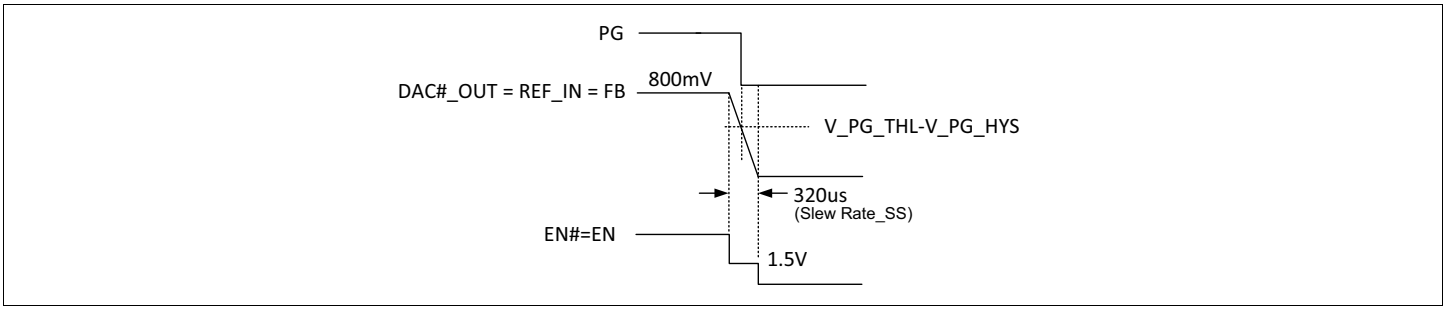


Figure 11: MxL7080 and MxL76500 Signals during Controlled Shutdown

During a fault shut down, the EN# and DAC#_OUT pins are all immediately pulled low. In Figure 12, the fault is initiated by the MxL76500 PG pulling low due an event on the regulator output (FB) which pulls it out of regulation.

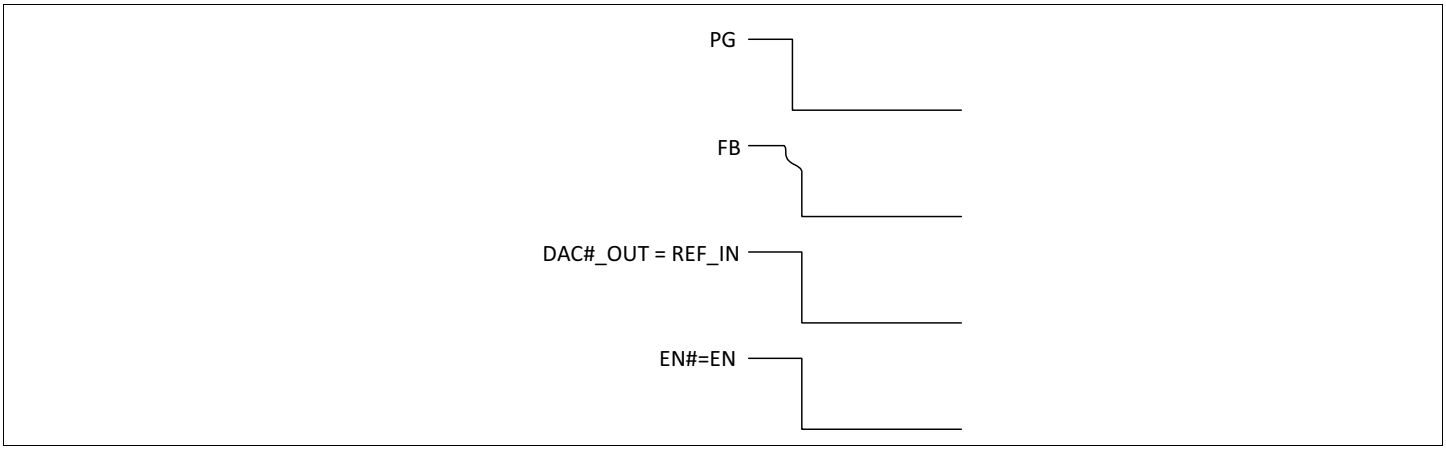


Figure 12: MxL7080 and MxL76500 Signals during MxL76500 Fault

System Interface

The following description details the system level functionality between MxL7080, MxL76500, and SoC:

- PMIC_EN initiates the cold boot sequence required by the SoC. This pin is usually connected to the PGOOD output of the P34 (Ethernet PHY) core regulator.
- PG_OUT is an open drain output which transitions to high impedance once cold boot is successfully completed. It is usually connected to the EN of the V0P8_A regulator as well as GPIO96 of the SoC. In event of a fault, PG_OUT pulls low. This output is rated for 3.6V and below. Do not connect to 5V.

System Timing Diagrams

Cold start is the typical action when power is applied to the system. It is expected that the sequencing chain between the 3.3V regulator and the Ethernet PHY core regulator power good is <10ms.

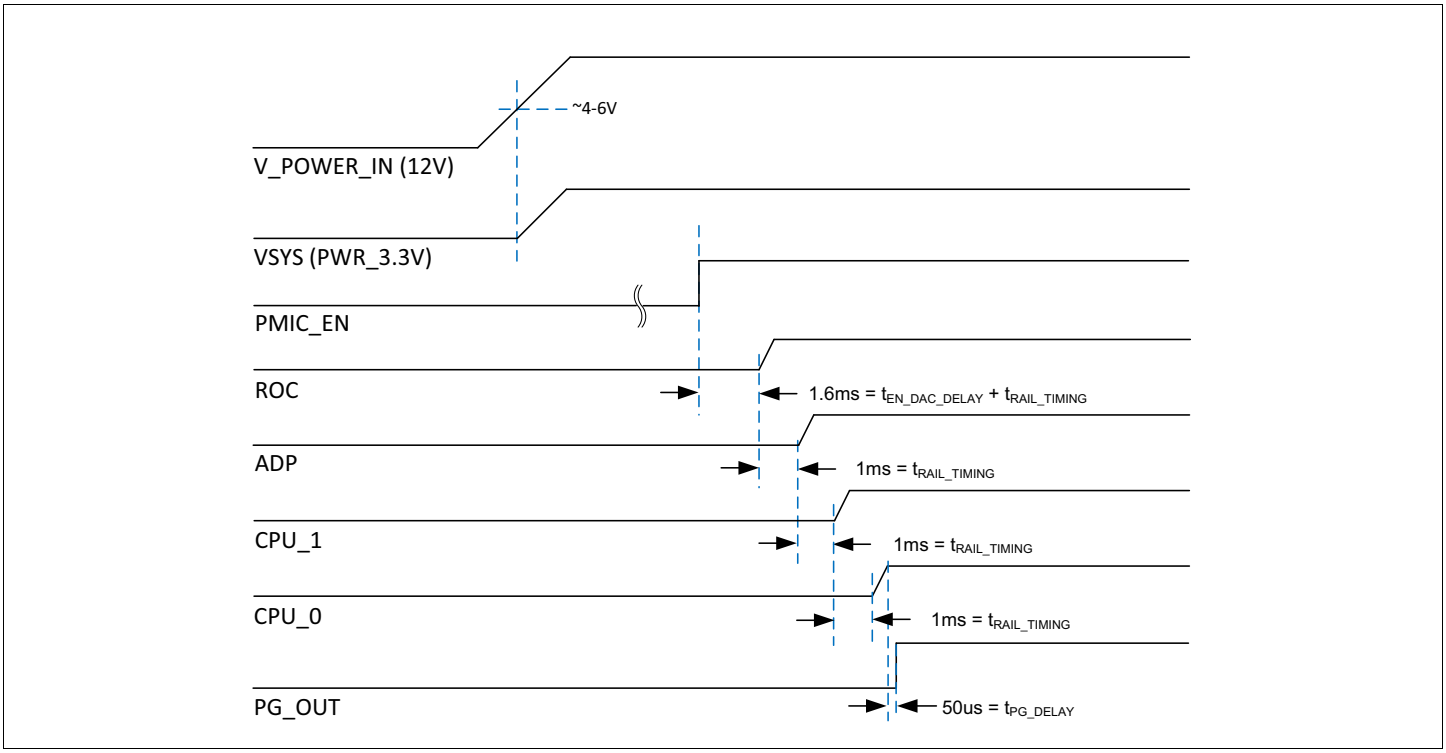


Figure 13: Cold Boot Timing Diagram

A cold off initiated by the SoC is intended to shut down the entire system until some other external event triggers a restart. Cold off is triggered by assertion of the REQUEST line by the SoC. The SoC should previously send a command setting the MxL7080 response to assertion of the REQUEST as a cold off action. When the power good from the Ethernet PHY core rail pulls low, PMIC_EN pulls low as well. At this point the system remains cold unless the 3.3V or main input 12V power is recycled.

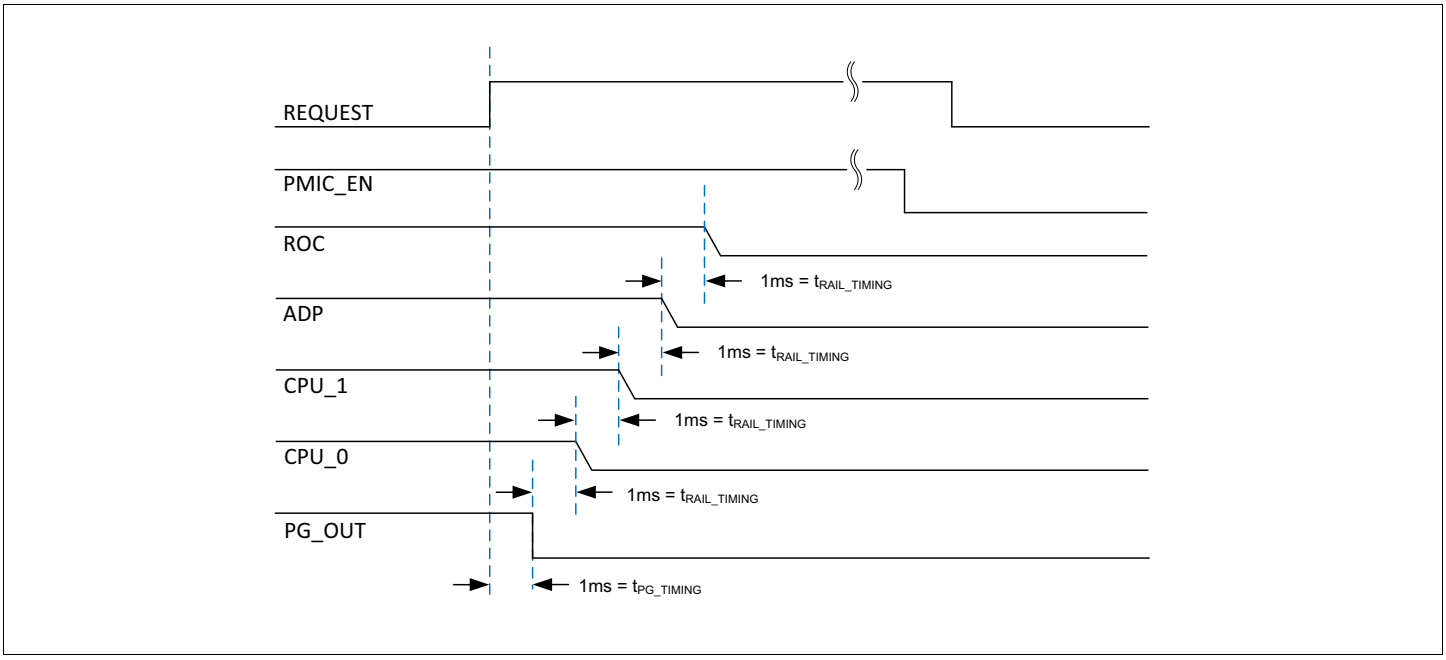


Figure 14: SoC Initiated Cold Off

A cold off can also be initiated by puling PMIC_EN low. Timing and behavior are the same as above but no request signal is sent.

The SoC can also initiate a cold reset. This completely shuts down the system and then initiates a restart after 1.5 second (t_{CRD}). PMIC_EN is ignored so it is insensitive to potential glitches as the rest of the power system is shut down. In a cold reset, the rails are sequenced as shown in Figure 15 on page 12.

The SoC can command the ROC rail to remain on during this sequence as shown in Figure 15 by the dashed line.

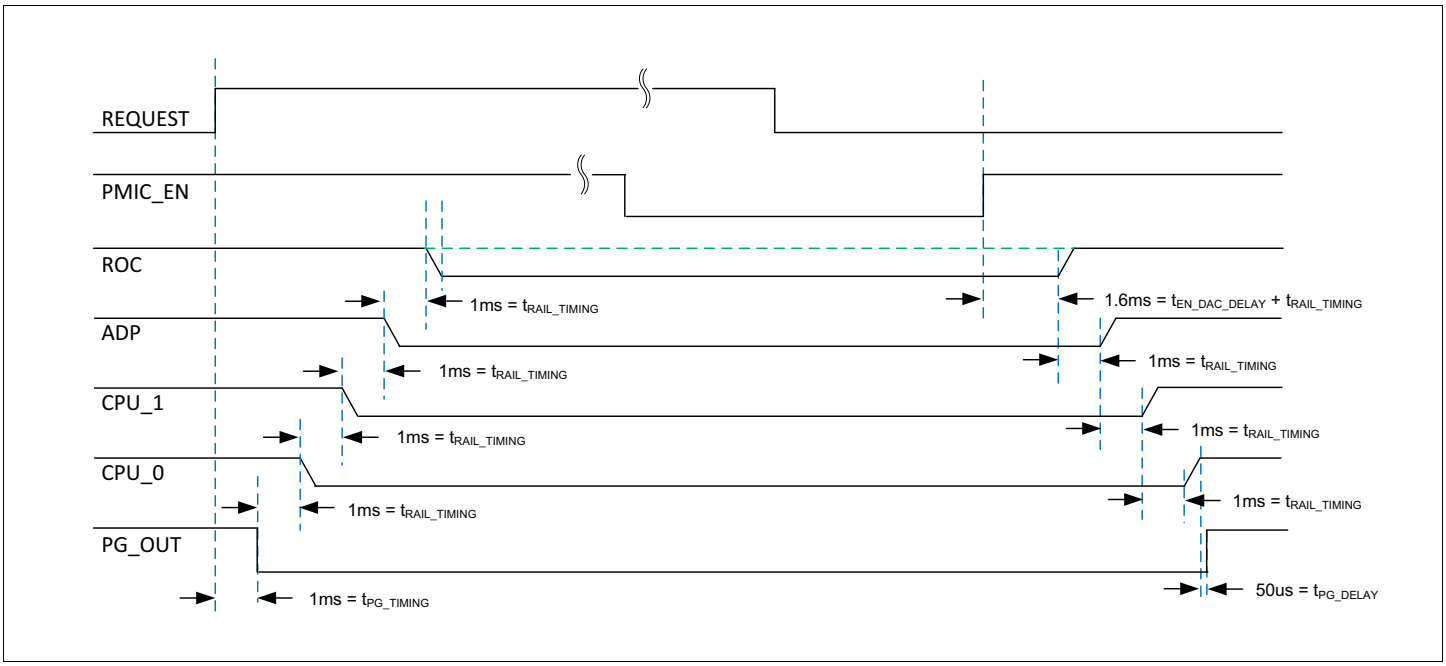


Figure 15: Cold Reset

A shutdown due to a fault is controlled solely by the MxL7080. Faults are generated by one of the MxL76500 PG pins transitioning low or by one of the DAC#_OUT pins being pulled low. Upon a fault being triggered, all outputs are immediately shut down after a 20µs deglitch filter. Outputs of the regulators decay based on the loading and capacitance value on the outputs. If the fault remains the system attempts to restart up to four times. Note that if a fault is present at initial power up, the number of restart attempts is unlimited.

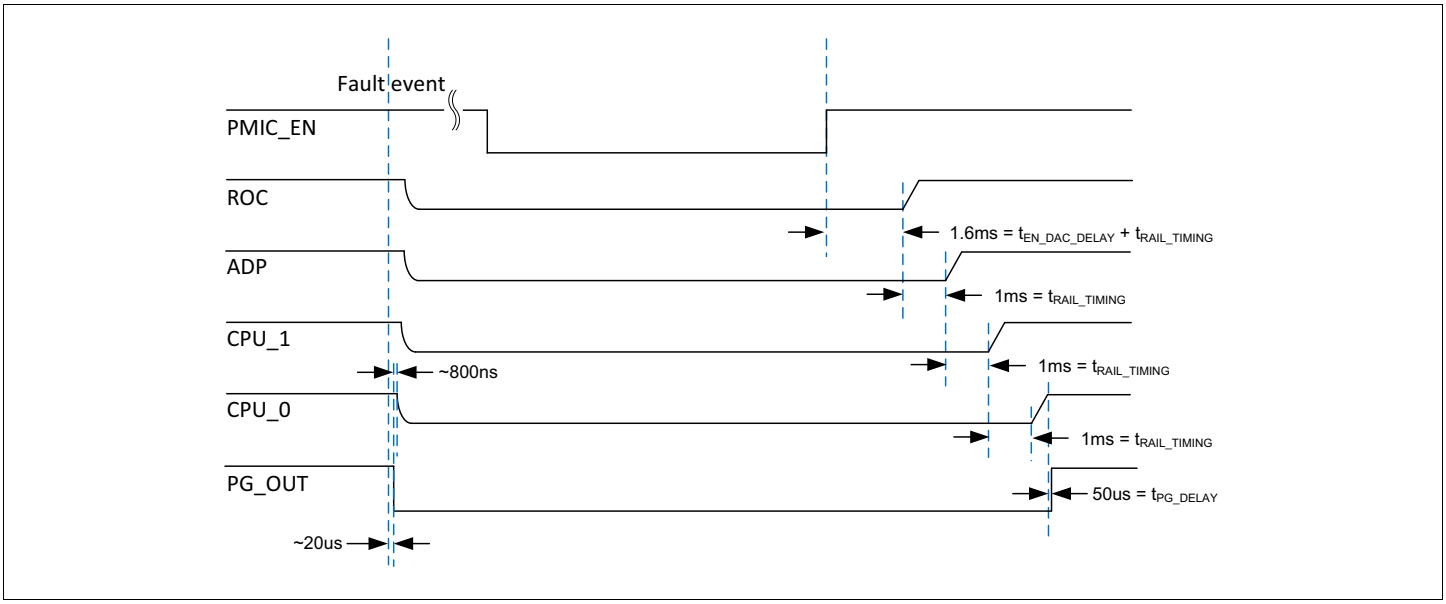


Figure 16: Fault and Recovery

OTP Default Configuration

The factory defaults are programmed according to the following table. The MxL7080 default values can be updated at the factory upon customer request.

Table 6: Factory Defaults

Setting	Default
I^2C Address	0x6A
Output Voltage	0.8V
Slew Rate	2.5mV/µs
Boot Rail Sequence#	3, 2, 1, 0
Rail Timing (each rail)	1ms

I2C Interface

The MxL7080 contains an I2C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply. The I2C signals should be 3.3V. The following figure shows the timing diagram.

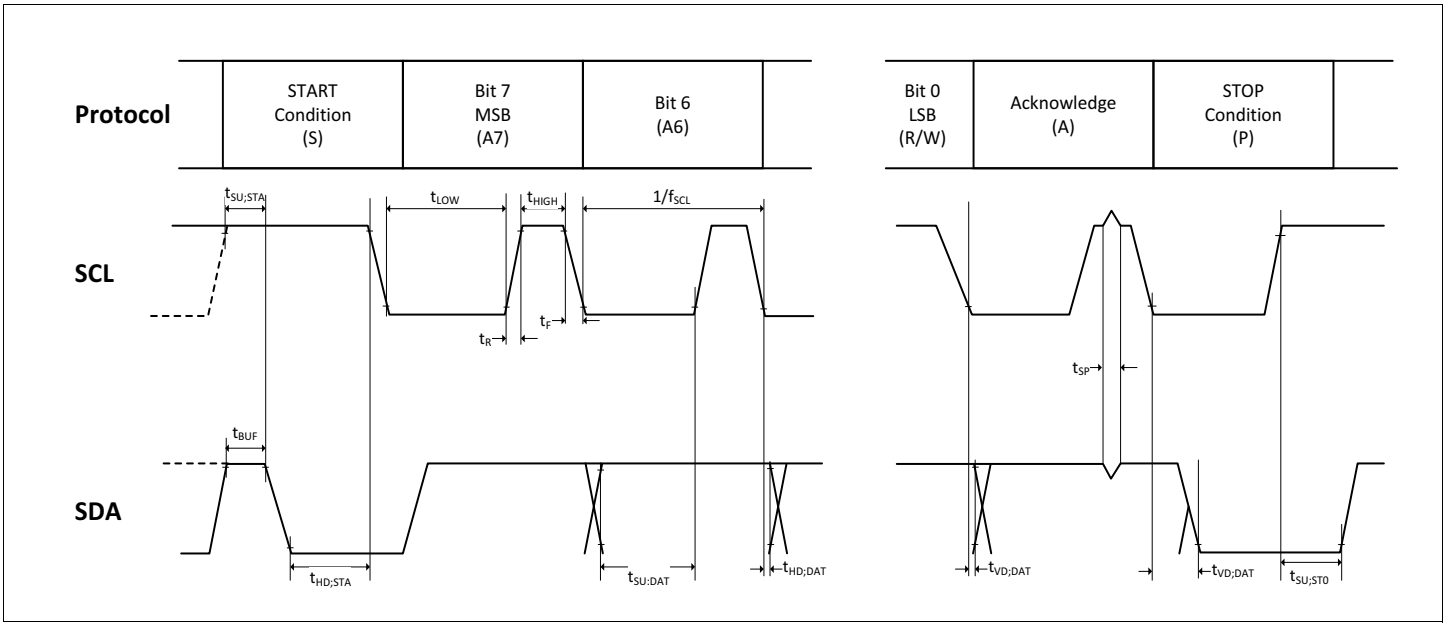


Figure 17: MxL7080 Timing Diagram

I2C Address

The configuration register space includes the standard MxL7080 register.

Table 7: I2C Addresses

Description	7-bit	8-bit (Write)	8-bit (Read)	Notes
MxL7080 Register set	0x6A	0xD4	0xD5	Alternative address: 0x6B

Register Map

You can use the MxL7080 registers listed in this section to configure, control, and monitor the MxL76500 regulators for the power sequencing, output voltage, and fault monitoring.

The following table lists the runtime registers that can be changed through the I^2C.

Table 8: **Register Address Map**

Address	Register	Access	Lock	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VENDID	RO	-	VENDID[7:0]							
01h	REV	RO	-	MAJREV0[3:0]				MINREV0[3:0]			
09A	LPM_RECOVERY	RW	-	-	-	-	-	-	-	-	LPM_RECOV
0Ah	OUT0_VID_SET	RW	-	OUT0_VID_SET[7:0]							
0Bh	OUT0_BOOT_VAL	RO	-	BOOT0_VID[7:0]							
0Ch	OUT0_SLEW_RATE	RW	REGLOCK	-	-	-	1	OUT0_SLOW_SR		-	-
0Dh	OUT0_MAX_VID	RW	-	OUT0_MAX_VID[7:0]							
0Eh	OUT1_VID_SET	RW	-	OUT1_VID_SET[7:0]							
0Fh	OUT1_BOOT_VAL	RO	-	BOOT1_VID[7:0]							
10h	OUT1_SLEW_RATE	RW	REGLOCK	-	-	-	1	OUT1_SLOW_SR	-	-	-
11h	OUT1_MAX_VID	RW	-	OUT1_MAX_VID[7:0]							
12h	OUT2_VID_SET	RW	-	OUT2_VID_SET[7:0]							
13h	OUT2_BOOT_VAL	RO	-	BOOT2_VID[7:0]							
14h	OUT2_SLEW_RATE	RW	REGLOCK	-	-	-	1	OUT2_SLOW_SR	-	-	-
15h	OUT2_MAX_VID	RW	-	OUT2_MAX_VID[7:0]							
16h	OUT3_VID_SET	RW	-	OUT3_VID_SET[7:0]							
17h	OUT3_BOOT_VAL	RO	-	BOOT3_VID[7:0]							
18h	OUT3_SLEW_RATE	RW	-	-	-	-	1	OUT3_SLOW_SR	-	-	-
19h	OUT3_MAX_VID	RW	-	OUT3_MAX_VID[7:0]							
21h	DVS_STAT	W1C	-	OUT3_REJECT	OUT2_REJECT	OUT1_REJECT	OUT0_REJECT	OUT3_SETTLE	OUT2_SETTLE	OUT1_SETTLE	OUT0_SETTLE
24h	PWRGD_STAT	RO	-	-	-	-	-	OUT3_PG	OUT2_PG	OUT1_PG	OUT0_PG
25h	PWRGD_MASK	RW	-	-	-	PGD_CFG_FAULT	PG_CFG_CR	OUT3_PG_M	OUT2_PG_M	OUT1_PG_MASK	OUT0_PG_MASK
26h	REQ_CTRL_IN	RW	-	-	-	-	-	-	-	-	REQUEST_IN
27h	REQ_CTRL_OUT	RW	REGLOCK	-	-	-	-	-	-	-	REQUEST_OUT
28h	REQ_CTRL_SEL	RW	-	-	-	-	-	-	-	-	REQ_CTRL_SEL
29h	REQ_ACT	RW	-	-	-	-	-	-	LPM	SHUT_DOWN_EN	COLD_RST_EN
2Ah	CRD_REG	RW	-	-	-	-	CRD[4:0]				
2Bh	LPM_STATUS	RO	-	-	-	-	-	-	-	-	LPM_STAT
2Ch	LPM_MODE	RW	-	-	GPIO2_LPM	GPIO1_LPM	GPO0_LPM	OUT3_LPM	OUT2_LPM	OUT1_LPM	OUT0_LPM
78h	CLD_RES	W1C	-	OUT3_VRF	OUT2_VRF	OUT1_VRF	OUT0_VRF	-	-	COLDRST_REQ	VR_FAULT
79h	SHDN_RES	W1C	-	-	-	-	-	-	-	PMIC_EN	COLDOFF_REQ
7Ah	VSYS_DET	W1C	-	-	-	-	-	-	-	-	VSYS_OV
7Bh	DAC_SHORT_FAULT	W1C	-	-	-	-	-	DAC3_FAULT	DAC2_FAULT	DAC1_FAULT	DAC0_FAULT
82h	RCVCFG	RW	REGLOCK	RCVLMT[3:0]				RCVDT[3:0]			
83h	RCVNUM	RW	REGLOCK	-	-	-	-	RCVNUM[3:0]			
84h	CPU_IRQLVL1	W1C	-	-	-	-	AIN_EVENT	I2C_EVENT	-	REQ_FAIL	-

Table 8: **Register Address Map**

Address	Register	Access	Lock	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
85h	CPU_IRQLVL1_MASK	RW	-	-	-	-	AIN_EVENT_M	I2C_EVENT_M	-	REQ_FAIL_M	-
86h	AIN_EVENT_IRQ	W1C	-	-	-	AIN_CMP_2_DN	AIN_CMP_1_DN	AIN_CMP_0_DN	AIN_CMP2_UP	AIN_CMP_1_UP	AIN_CMP_0_UP
87h	AIN_EVENT_IRQ_MASK	RW	-	-	-	AIN_CMP_2_DN_M	AIN_CMP_1_DN_M	AIN_CMP_0_DN_M	AIN_CMP2_UP_M	AIN_CMP_1_UP_M	AIN_CMP_0_UP_M
88h	I2C_EVENT_IRQ	W1C	-	-	-	-	-	-	I2C_RD_ERR	I2C_VAL_ERR	I2C_ADDR_ERR
89h	I2C_EVENT_IRQ_MASK	RW	-	-	-	-	-	-	I2C_RD_ERR_M	I2C_VAL_ERR_M	I2C_ADDR_ERR_M
90h	GPO0_CNTL	RW	-	-	-	-	-	-	GPO0_POL	GPO0_OUT	GPO0_MODE
91h	GPIO1_CNTL	RW	-	-	-	GPIO1_IN_POL	GPIO1_IN_DIS	GPIO1_IN_OUT	GPIO1_POL	GPIO1_OUT	GPIO1_MODE
92h	GPIO2_CNTL	RW	-	-	-	-	-	GPIO2_IN_OUT	GPIO2_POL	GPIO2_OUT	GPIO2_MODE
94h	CR_CONFIG	RW	-	-	GPIO2_CFG	GPIO1_CFG	GPO0_CFG	ROC_CR_M	ADP_CR_M	CPU1_CR_M	CPU0_CR_M
95h	AIN_THR0	RW	-	-	-	AIN_THR0_VAL[5:0]					
96h	AIN_THR1	RW	-	-	-	AIN_THR1_VAL[5:0]					
97h	AIN_THR2	RW	-	-	-	AIN_THR2_VAL[5:0]					
98h	AIN_CONFIG	RW	-	-	-	-	-	-	AIN_WAIT_TIME		AIN_CLK_GATE
99h	AIN_STAT	RO	-	-	-	-	-	-	AIN_CMP2	AIN_CMP1	AIN_CMP0
A0h	REGLOCK	RW	REGLOCK	-	-	-	-	-	-	-	REG_LCK

Note: W1C (Write 1 to Clear) access indicates that writing a logic *1* to the bit position clears the status bit.

Vendor Identification Codes and Revision Number

Table 9: Vendor Identification Register (00h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VENDID	RO	VENDID[7:0]								0x4D	0x00

Bit	Bit Field	Function	Default
[7:0]	VENDID	Specific MaxLinear's identification number.	0x4D

Table 10: Revision Register (01h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REV	RO	MAJREV0[3:0]				MINREV0[3:0]				0xA0	0x01

Bit	Bit Field	Function	Default
D[7:4]	MAJREV0[3:0]	Major revision: The first stepping should start with *1010* and increment by 1 for each new complete mask stepping: ■ 1010 = A ■ 1011 = B ■ …	A
D[3:0]	MINREV0[3:0]	Minor revision: The first stepping should start with *0000* and increment by 1 for each new metal layer stepping. Resets to *0000* when MAJREV0[3:0] increments: ■ 0000 = 0 ■ 0001 = 1 ■ …	0

Register Lock

The REGLOCK register prevents accidental or malicious writes to the specific registers after they are set/tuned by the SoC. The initial state of REGLOCK register is *0* (un-lock), so the SoC can overwrite all registers during the boot process. However, for safety reasons, MaxLinear strongly recommends that you set the REGLOCK register to *1* (lock) just after the boot process.

The REGLOCK group of registers include:

REGLOCK(0Ah), OUT0_SLEW_RATE(0Ch), OUT1_SLEW_RATE(10h), OUT2_SLEW_RATE(14h), OUT3_SLEW_RATE(18h), REQ_CTRL_SEL(27h), RCVCFG(82h), RCVNUM(83h)

Table 11: Register LOCK Register (A0h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REGLOCK	R/W	RSVD							REG_LCK	0x00	0xA0

Bit	Bit Field	Function	Default
D[7:1]	RSVD	Reserved.	0
D[0]	REG_LCK	Write access for REGLOCK group registers: ■ 0 = Do not lock the registers that are listed in the REGLOCK group. ■ 1 = Lock the registers that are listed in the REGLOCK group. Once REG_LCK is written to 1, it cannot be over-written to 0. REG_LCK can only be cleared when the power state is PMIC_G3.	0

Controlling Registers

This section lists the registers that manage the DVS control for each rail.

DVS

The MxL7080 and MxL76500 solution is required to signal the SoC when the DVS rail transition is completed, and the output voltage is within the target requested value with the requested tolerance. Following a new VID request by the SoC, the MxL7080 should start ramping the specific rail at the programmed slew rate. Once the specific rail has settled, the MxL7080 should assert the corresponding OUTx_SETTLE bit in the DVS_STAT (21h) register and then assert the specific rail status to the SoC, in a form of a pulse.

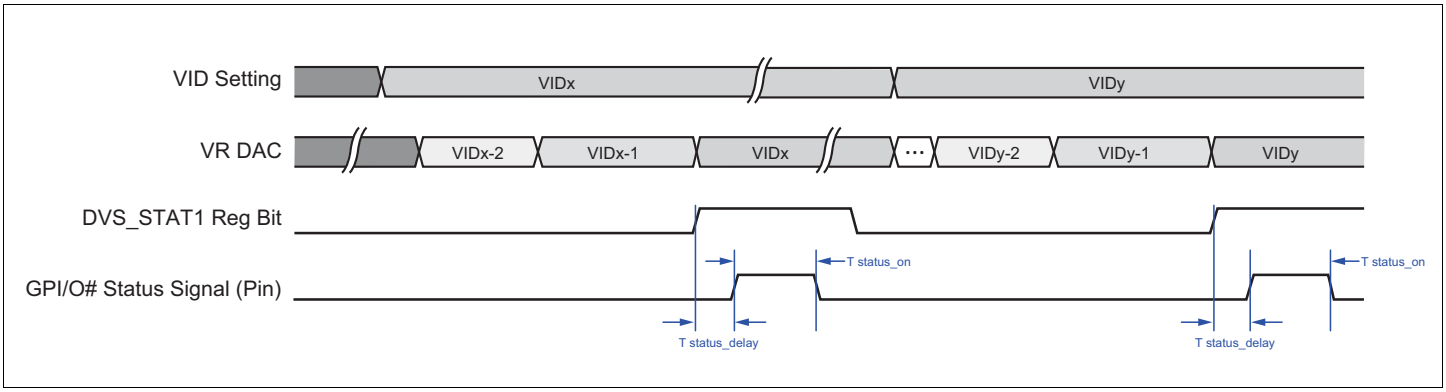


Figure 18: VR Rail Status Timing

VID Settings

Write to the relevant DAC register to DVS to a specific VID setting. For reference, select the code to write from the Table 28 on page 24.

Prior to programming OUT0_VID_SET, ensure that OUT0_MAX_VID is set to a value not exceeding 1000mV.

Table 12: DVS Rail VID Setting Register DAC0 (0Ah)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT0_VID_SET	R/W	OUT0_VID[7:0]								0x00	0x0A

Bit	Bit Field	Function	Default
D[7:0]	OUT0_VID[7:0]	Currently programmed VID for DAC0. Following a write command, the specific rail starts to ramp: ■ 0x00 = OFF (Rail shut down).	0x00

Prior to programming OUT1_VID_SET, ensure that OUT1_MAX_VID is set to a value not exceeding 1000mV.

Table 13: DVS Rail VID Setting Register DAC1 (0Eh)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT1_VID_SET	R/W	OUT1_VID[7:0]								0x00	0x0E

Bit	Bit Field	Function	Default
D[7:0]	OUT1_VID[7:0]	Currently programmed VID for DAC1. Following a write command, the specific rail starts to ramp: ■ 0x00 = OFF (Rail shut down).	0x00

Prior to programming OUT2_VID_SET, ensure that OUT2_MAX_VID is set to a value not exceeding 1000mV

Table 14: DVS Rail VID Setting Register DAC2 (12h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT2_VID_SET	R/W	OUT2_VID[7:0]								0x00	0x12

Bit	Bit Field	Function	Default
D[7:0]	OUT2_VID[7:0]	Currently programmed VID for DAC2. Following a write command, the specific rail starts to ramp: ■ 0x00 = OFF (Rail shut down).	0x00

Prior to programming OUT3_VID_SET, ensure that OUT3_MAX_VID is set to a value not exceeding 1000mV.

Table 15: DVS Rail VID Setting Register DAC3 (16h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT3_VID_SET	R/W	OUT3_VID[7:0]								0x00	0x16

Bit	Bit Field	Function	Default
D[7:0]	OUT3_VID[7:0]	Currently programmed VID for DAC3. Following a write command, the specific rail starts to ramp: ■ 0x00 = OFF (Rail shut down).	0x00

Rail Default Boot Value

Write to the relevant OUT#_BOOT_VAL register to set the output voltage after a cold boot. For reference, select the code to write from the Table 28 on page 24.

Table 16: DVS Rail VID Setting Register DAC0 (0Bh)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT0_BOOT_VAL	RO	BOOT0_VID[7:0]								0x3D	0x0B

Bit	Bit Field	Function	Default
D[7:0]	BOOT0_VID[7:0]	The value which the VR has following cold boot: ■ 0x00 = OFF (Rail shut down).	0x3D

Table 17: DVS Rail VID Setting Register DAC1 (0Fh)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT1_BOOT_VAL	RO	BOOT1_VID[7:0]								0x3D	0x0F

Bit	Bit Field	Function	Default
D[7:0]	BOOT1_VID[7:0]	The value which the VR has following cold boot: ■ 0x00 = OFF (Rail shut down).	0x3D

Table 18: DVS Rail VID Setting Register DAC2 (13h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT2_BOOT_VAL	RO	BOOT2_VID[7:0]								0x3D	0x13

Bit	Bit Field	Function	Default
D[7:0]	BOOT2_VID[7:0]	The value which the VR has following cold boot: 0x00 = OFF (Rail shut down).	0x3D

Table 19: DVS Rail VID Setting Register DAC3 (17h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT3_BOOT_VAL	RO	BOOT3_VID[7:0]								0x3D	0x17

Bit	Bit Field	Function	Default
D[7:0]	BOOT3_VID[7:0]	The value which the VR has following cold boot: 0x00 = OFF (Rail shut down).	0x3D

Slew Rate

Write to the relevant OUT#_SLEW_RATE register to set the slew rate.

Table 20: DAC0 DVS Rail Slew Rate Register (0Ch)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT0_SLEW_RATE	RW	RSVD			1	OUT0_SLOW_SR		RSVD		0x10	0x0C

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0001b).	0001b
D[3:2]	OUT0_SLOW_SR	■ 00b = 2.5mV/µs ■ 01b = 5mV/µs ■ 10b = 10mV/µs ■ 11b = 20mV/µs	00b
D[1:0]	RSVD	Reserved (00b).	00b

Note: The slew rate register must not change during rail ramp up/down.

Table 21: DAC1 DVS Rail Slew Rate Register (10h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT1_SLEW_RATE	RW	RSVD			1	OUT1_SLOW_SR		RSVD		0x10	0x10

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0001b).	0001b
D[3:2]	OUT1_SLOW_SR	■ 00b = 2.5mV/µs ■ 01b = 5mV/µs ■ 10b = 10mV/µs ■ 11b = 20mV/µs	00b
D[1:0]	RSVD	Reserved (00b).	00b

Note: The slew rate register must not change during rail ramp up/down.

Table 22: DAC2 DVS Rail Slew Rate Register (14h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT2_SLEW_RATE	RW	RSVD			1	OUT2_SLOW_SR		RSVD		0x10	0x14

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0001b).	0001b
D[3:2]	OUT2_SLOW_SR	■ 00b = 2.5mV/µs ■ 01b = 5mV/µs ■ 10b = 10mV/µs ■ 11b = 20mV/µs	00b
D[1:0]	RSVD	Reserved (00b).	00b

Note: The slew rate register must not change during rail ramp up/down.

Table 23: DAC3 DVS Rail Slew Rate Register (18h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT3_SLEW_RATE	RW	RSVD			1	OUT3_SLOW_SR		RSVD		0x10	0x18

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0001b).	0001b
D[3:2]	OUT3_SLOW_SR	■ 00b = 2.5mV/µs ■ 01b = 5mV/µs ■ 10b = 10mV/µs ■ 11b = 20mV/µs	00b
D[1:0]	RSVD	Reserved (00b).	00b

Note: The slew rate register must not change during rail ramp up/down.

DVS Max Values

Program the corresponding OUT#_MAX_VID register for each rail to ensure the maximum VID permitted for Dynamic Voltage Scaling (DVS) does not exceed 1000mV. For reference, select the code to write from the Table 28 on page 24.

Table 24: DAC0 DVS Max Value Register (0Dh)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT0_MAX_VID	R/W	OUT0_MAX_VID[7:0]								0x8D	0x0D

Bit	Bit Field	Function	Default
D[7:0]	OUT0_MAX_VID [7:0]	Maximum VID that the specific DVS rail supports.	0x8D

Table 25: DAC1 DVS Max Value Register (11h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT1_MAX_VID	R/W	OUT1_MAX_VID[7:0]								0x8D	0x11

Bit	Bit Field	Function	Default
D[7:0]	OUT1_MAX_VID [7:0]	Maximum VID that the specific DVS rail supports.	0x8D

Table 26: DAC2 DVS Max Value Register (15h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT2_MAX_VID	R/W	OUT2_MAX_VID[7:0]								0x8D	0x15

Bit	Bit Field	Function	Default
D[7:0]	OUT2_MAX_VID [7:0]	Maximum VID that the specific DVS rail supports.	0x8D

Table 27: DAC3 DVS Max Value Register (19h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OUT3_MAX_VID	R/W	OUT3_MAX_VID[7:0]								0x8D	0x19

Bit	Bit Field	Function	Default
D[7:0]	OUT3_MAX_VID [7:0]	Maximum VID that the specific DVS rail supports.	0x8D

VID Values

Each 8-bit VID code represents 5mV on the output voltage.

Table 28: VID Values and Output Voltage

VID Code	Output Voltage (V)
0x00–0x14	Invalid
0x15	0.600
0x16	0.605
0x17	0.610
0x18	0.615
:	:
0x3d	0.800 (Default boot VID)
:	:
0x65	1.000 (Practical maximum value)
0x66–0xFF	Invalid

DVS Rail Status

The MxL7080 and MxL76500 devices are a solution required to signal the SoC when the DVS rail transition is completed and the output voltage is within the target requested value with the requested tolerance.

The rail settled function is critical to the SoC function when moving from a lower VID to a higher VID.

Following a new VID request by the SoC, the MxL7080 should start ramping the specific rail at the programmed slew rate. After the specific rail has settled, the MxL7080 should assert the corresponding settle bit in the DVS Rail status register and then assert the specific rail status signal to the SoC in the form of a pulse.

Register Description (only for status indications)

- Settle Condition: It is the *Settle* bit in the *DVS Rail status* register that should be asserted. The status signal should be also triggered when a DVS rail output voltage reaches the target voltage set in the rail VID setting register within the target tolerance.
- Reject Condition: It is the *Reject* bit in the *DVS Rail status* register that should be asserted when a VID code is higher than the DVS maximum value register set to the VID setting register.

Table 29: DVS Rail Status Register (21h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
DVS_STAT	W1C	OUT3 REJECT	OUT2 REJECT	OUT1_ REJECT	OUT0_ REJECT	OUT3 SETTLE	OUT2 SETTLE	OUT1_ SETTLE	OUT0_ SETTLE	0x00	0x21

Bit	Bit Field	Function	Default
D[7:4]	OUT3_ REJECT OUT2_ REJECT OUT1_REJECT OUT0_REJECT	■ 0 = No reject event. ■ 1 = A higher VID code than VOUT maximum register is set to the VID setting register.	0
D[3:0]	OUT3_SETTLE OUT2_SETTLE OUT1_SETTLE OUT0_SETTLE	■ 0 = Rail is ramping. ■ 1 = Rail output reached the target voltage, which is set in the rail VID setting register, within the defined tolerance.	0

Note: The `DVS_STAT` register bits should be cleared (asserted back to *0*) when a new VID value is written by the SOC.

Power Good Status and Mask Register

Table 30: Power Good Status Register (24h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PWRGD_STAT	RO	RSVD				OUT3_PG	OUT2_PG	OUT1_PG	OUT0_PG	0x00	0x24

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0000b).	0
D[3]	OUT3_PG	■ 0 = Rail is invalid (ROC). ■ 1 = Rail has a valid output (ROC).	0
D[2]	OUT2_PG	■ 0 = Rail is invalid (ADP). ■ 1 = Rail has a valid output (ADP).	0
D[1]	OUT1_PG	■ 0 = Rail is invalid (CPU1). ■ 1 = Rail has a valid output (CPU1).	0
D[0]	OUT0_PG	■ 0 = Rail is invalid (CPU0). ■ 1 = Rail has a valid output (CPU0).	0

Note: This register should be cleared only after cold boot.

Table 31: Power Good Status Mask Register (25h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PWRGD_MASK	R/W	RSVD		PGD_CFG_FAULT	PG_CFG_CR	OUT3_PG_M	OUT2_PG_M	OUT1_PG_M	OUT0_PG_M	0x00	0x25

Bit	Bit Field	Function	Default
D[7:6]	RSVD	Reserved (00b).	0
D[5]	PGD_CFG_FAULT	■ 0 = PWRGD becomes low during a fault. ■ 1 = PWRGD remains high when a fault occurs (assuming that the PWRGD is originally high before fault).	0
D[4]	PG_CFG_CR	■ 0 = PWRGD becomes low during a cold reset. ■ 1 = PWRGD remains high during a cold reset (assuming that the PWRGD is originally high before fault).	0
D[3]	OUT3_PG_M	■ 0 = Rail is not masked. ■ 1 = Rail is masked.	0
D[2]	OUT2_PG_M	■ 0 = Rail is not masked. ■ 1 = Rail is masked.	0
D[1]	OUT1_PG_M	■ 0 = Rail is not masked. ■ 1 = Rail is masked.	0
D[0]	OUT0_PG_M	■ 0 = Rail is not masked. ■ 1 = Rail is masked.	0

DAC Fault Detection

Table 32: DAC Short Fault Register (7Bh)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
DAC_SHORT_FAULT	W1C	RSVD	RSVD	RSVD	RSVD	DAC3_FAULT	DAC2_FAULT	DAC1_FAULT	DAC0_FAULT	0x00	0x7B

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0000b).	0
D[3]	DAC3_FAULT	■ 0 = No fault detected on DAC3. ■ 1 = DAC3 fault detected which shuts down the part and follow fault sequence.	0
D[2]	DAC2_FAULT	■ 0 = No fault detected on DAC2. ■ 1 = DAC2 fault detected which shuts down the part and follow fault sequence.	0
D[1]	DAC1_FAULT	■ 0 = No fault detected on DAC1. ■ 1 = DAC1 fault detected which shuts down the part and follow fault sequence.	0
D[0]	DAC0_FAULT	■ 0 = No fault detected on DAC0 ■ 1 = DAC0 fault detected which shuts down the part and follow fault sequence.	0

Note: This register should be cleared when writing 1 to the register.

Request Signal

The request signal is an active high signal from the SoC which indicates several events such as severe catastrophic events, watchdog timer (WD) expiration, thermal events, power mode transition, cold reset, etc. This signal should trigger MxL7080 to carry out pre-defined actions such as shut-down, re-boot, change some VR output, or any operation listed in the Table 33.

The request signal is asynchronous to any other signal and not related to any power mode which the MxL7080 may reside in. MxL7080 should respond to this signal without any other dependencies.

Request signal voltage levels should be 3.3v.

- The REQ_CTRL_IN register acts identically to the request signal posedge (low to high).
- The REQ_CTRL_OUT register acts identically to the request signal negedge (high to low).

Table 33: Request Control Selection Register (28h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REQ_CTRL_SEL	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	REQ_CTRL_SEL	0x01	0x28

Bit	Bit Field	Function	Default
D[7:1]	RSVD	Reserved (0000 000b).	0
D[0]	REQ_CTRL_SEL	■ 0 = Enables the option to trigger request by the host writing to the REQ_IN/OUT registers. The REQUEST pin/signal control is disabled. ■ 1 = Disables the option to trigger request by the host writing to the REQ_IN/OUT registers. The REQUEST pin/signal control is enabled.	1

Table 34: Request Control Signal Register – In (26h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REQ_CTRL_IN	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	REQUEST_IN	0x00	0x26

Bit	Bit Field	Function	Default
D[7:1]	RSVD	Reserved (0000 000b).	0
D[0]	REQUEST_IN	■ 0 = Default state of the request, not being trigger by the SoC host. ■ 1 = Request is triggered by the SoC host. For LPM command, it is LPM entry.	0

Note: This register should be cleared to default (0x00) after a write operation.

Table 35: Request Control Signal Register – Out (27h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REQ_CTRL_OUT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	REQUEST_OUT	0x00	0x27

Bit	Bit Field	Function	Default
D[7:1]	RSVD	RSVD.	0
D[0]	REQUEST_OUT	■ 0 = Default state of the request, not being trigger by the SoC host. ■ 1 = Request is triggered by the SoC host. For LPM command, it is LPM Exit.	0

Upon receiving the request signal (using register or a signal), the MxL7080 should respond according to the function programmed in a dedicated request events register. This dedicated register should be programmed by the SoC host or the SoC EPU prior to any actual request:

Table 36: Request Event Register (29h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REQ_ACT	R/W	RSVD					LPM	SHUT_DOWN_EN	COLD_RST_EN	0x01	0x29

Bit	Bit Field	Function	Default
D[7:3]	RSVD	Reserved (0000 0b).	0
D[2]	LPM	■ 0 = LPM disabled. ■ 1 = MxL7080 switches to the lower power mode as defined in LPM register.	0
D[1]	SHUT_DOWN_EN	■ 0 = Shut-down disabled. No action is executed. ■ 1 = The MxL7080 executes the shut-down procedure, and then stays at this state until the AC/DC cable is re-plugged.	0
D[0]	COLD_RST_EN	■ 0 = Cold reset disabled. No action is executed. ■ 1 = The MxL7080 executes the cold reset procedure with Off duration as indicated by the cold reset duration CRD[4:0] of CRD_REG (2Ah).	1

Cold Reset Request

When the cold reset is configured by the SoC and triggered, the MxL7080 should execute a cold reset process according to the delay programmed in cold reset duration register (CRD_REG).

During the cold reset, the MxL7080 should assert GPO0 (low) for the duration defined by CRD and after the CRD time is expired, the GPO0 must return to High-Z state (there are PU resistors on the PCB) to enable all the platform VR devices.

Following the cold reset process, all the rail's output voltage values should be as their default values defined in 3.1.

The MxL7080 should have an option to control all the rail's output during the cold reset and should implement two options of behavior for each rail using a dedicated register:

- The rail ramps down and after t_CRD ramp up as shown in Figure 15 on page 12.
- The rail remains high during the cold reset.

In any of the above cases, the general MxL7080 PG signal should be de-asserted (and then asserted) whenever the PMIC is performing the cold reset request.

Table 37: Cold Reset Configuration Register (94h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
CR_CONFIG	R/W	RSVD	GPIO2_ CFG	GPIO1_ CFG	GPO0_ CFG	ROC_ CR_M	ADP_ CR_M	CPU1_ CR_M	CPU0_ CR_M	0x00	0x94

Bit	Bit Field	Function	Default
D[7]	RSVD	Reserved (0b).	0
D[6]	GPIO2_CFG	■ 0 = GPIO2 is cycled off and on during the cold reset. ■ 1 = GPIO2 remains at the latest state during the cold reset.	0
D[5]	GPIO1_CFG	■ 0 = GPIO1 is cycled OFF and ON during the cold reset. ■ 1 = GPIO1 remains at the latest state during the cold reset.	0
D[4]	GPO0_CFG	■ 0 = GPO0 is cycled off and on during the cold reset. ■ 1 = GPO0 remains at the latest state during the cold reset.	0
D[3]	ROC_CR_M	■ 0 = ROC is cycled off and on during the cold reset. ■ 1 = ROC remains at the latest value during the cold reset.	0
D[2]	ADP_CR_M	■ 0 = ADP rail is cycled off and on during the cold reset. ■ 1 = ADP remains at the latest value during the cold reset.	0
D[1]	CPU1_CR_M	■ 0 = CPU1 rail is cycled off and on during the cold reset. ■ 1 = CPU1 remains at the latest value during the cold reset.	0
D[0]	CPU0_CR_M	■ 0 = CPU0 rail is cycled off and on during the cold reset. ■ 1 = CPU0 remains at the latest value during the cold reset.	0

Table 38: Cold Reset Duration Register (2Ah)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
CRD_REG	R/W	RSVD	RSVD	RSVD	CRD[4:0]					0x0F	0x2A

Bit	Bit Field	Function	Default
D[7:5]	RSVD	Reserved (000b).	0
D[4:0]	CRD[4:0]	The cold reset duration time during which the MxL7080 stays in shut down mode following a cold reset request, before performing the following cold boot sequence: ■ 00000 = 5ms ■ 00001 = 10ms ■ 00010 = 15ms ■ 00011 = 20ms ■ 00100 = 25ms ■ 00101 = 30ms ■ 00110 = 35ms ■ 00111 = 40ms ■ 01000 = 45ms ■ 01001 = 50ms ■ 01010 = 75ms ■ 01011 = 100ms ■ 01100 = 250ms ■ 01101 = 500ms ■ 01110 = 750ms ■ 01111 = 1500 ms ■ 10000 = 3s (0.05 min) ■ 10001 = 6s (0.1 min) ■ 10010 = 12s (0.2 min) ■ 10011 = 24s (0.4 min) ■ 10100 = 48s (0.8 min) ■ 10101 = 96s (1.6 min) ■ 10110 = 192s (3.2 min) ■ 10111 = 384s (6.4 min) ■ 11000 = 768s (12.8 min) ■ 11001 = 1536s (25.6min) ■ 11010 = 3072s (51.2min)	0xF

Note: Lower CRD numbers than 30ms are not recommended.

LPM Request

In the case of the LPM mode is requested by the SoC, the MxL76500 outputs should change according to the state programmed in the following `LPM_MODE` register.

Table 39: LPM Mode Register (2Ch)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LPM_MODE	R/W	RSVD	GPIO2_LPM	GPIO1_LPM	GPIO_0_LPM	OUT3_LPM	OUT2_LPM	OUT1_LPM	OUT0_LPM	0x3F	0x2C

Bit	Bit Field	Function	Default
D[7]	RSVD	Reserved (0b).	0
D[6]	GPIO2_LPM	Only if GPIO1 is configured as output using the OTP: ■ 0 = GPIO = *0* ■ 1 = GPIO = *1*	1
D[5]	GPIO1_LPM	Only if GPIO1 is configured as output using the OTP: ■ 0 = GPIO = *0* ■ 1 = GPIO = *1*	1
D[4]	GPO0_LPM	■ 0 = GPIO = *0* and `PMIC_EN` = Do not care (`PMIC_EN` is ignored). ■ 1 = GPIO = *1*	1
D[3]	OUT3_LPM	■ 0 = Rail is off ■ 1 = Rail is on	1
D[2]	OUT2_LPM	■ 0 = Rail is off ■ 1 = Rail is on	1
D[1]	OUT1_LPM	■ 0 = Rail is off ■ 1 = Rail is on	1
D[0]	OUT0_LPM	■ 0 = Rail is off ■ 1 = Rail is on	1

Note: If a GPIO is connected to the SoC 3.3V regulator, it is prohibited to change the GPIO bit in the LPM_MODE register to be low, since in that case the request signal from the SoC loses its power (the SoC-to-MxL7080 are 3.3V).
SoC should write to this register only in PMIC_S0 state.

Table 40: LPM Recovery Register (09h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LPM_RECOVERY	RW	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LPM_RECOV	0x00	0x09

Bit	Bit Field	Function	Default
D[7:1]	RSVD	Reserved (0000 000b).	0
D[0]	LPM_RECOV	■ 0 = Upon exit from LPM, boot with V_{OUT} value based on OUT#_VID_SET_REG register. ■ 1 = Upon exit from LPM, boot with V_{OUT} value based on OUT#_BOOT_VAL register.	0

Table 41: LPM Status Register (2Bh)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
LPM_STATUS	RO	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LPM_STAT	0x00	0x2B

Bit	Bit Field	Function	Default
D[7:1]	RSVD	Reserved (0000 000b).	0
D[0]	LPM_STAT	■ 0 = MxL7080 is not in LPM mode. ■ 1 = MxL7080 is in LPM mode.	0

AIN Control Registers

The analog input (AIN) functionality has three programmable analog threshold values used for comparison. The AIN threshold values should represent 25mv, within the range from 0v to 1575mv.

The following figure shows the high-level block diagram of the AIN functionality.

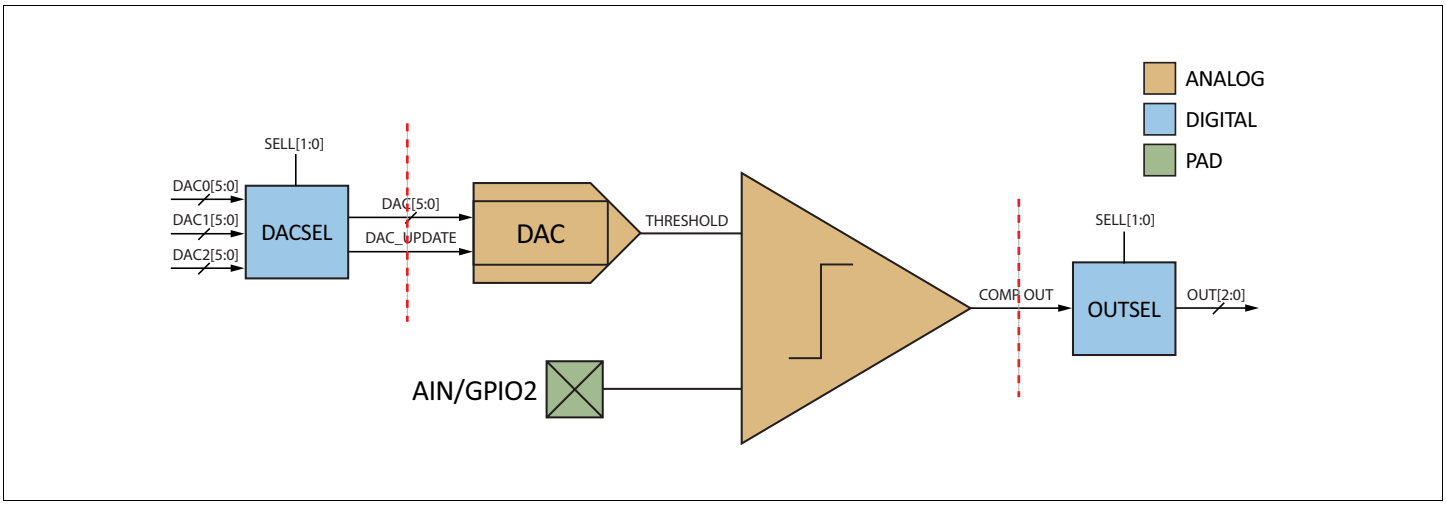


Figure 19: AIN Block Diagram

Table 42: AIN Threshold Register0 (95h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
AIN_THR0	R/W	RSVD	RSVD	AIN_THR0_VAL						0x00	0x95

Bit	Bit Field	Function	Default
D[7:6]	RSVD	Reserved (00b).	0
D[5:0]	AIN_THR0_VAL	Threshold #0 value: ■ 0x00 = 0mV ■ 0x01 = 25mV ■ … ■ 0x3F = 1575mV	0

Table 43: AIN Threshold Register1 (96h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
AIN_THR1	R/W	RSVD	RSVD	AIN_THR1_VAL						0x00	0x96

Bit	Bit Field	Function	Default
D[7:6]	RSVD	Reserved (00b).	0
D[5:0]	AIN_THR1_VAL	Threshold #0 value: ■ 0x00 = 0mV ■ 0x01 = 25mV ■ … ■ 0x3F = 1575mV	0

Table 44: AIN Threshold Register2 (97h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
AIN_THR2	R/W	RSVD	RSVD	AIN_THR2_VAL						0x00	0x97

Bit	Bit Field	Function	Default
D[7:6]	RSVD	Reserved (00b).	0
D[5:0]	AIN_THR2_VAL	Threshold #0 value: ■ 0x00 = 0mV ■ 0x01 = 25mV ■ … ■ 0x3F = 1575mV	0

Table 45: AIN Configuration Register (98h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
AIN_CONFIG	RW	RSVD	RSVD	RSVD	RSVD	RSVD	AIN_WAIT_TIME		AIN_CLK_GATE	0x01	0x98

Bit	Bit Field	Function	Default
D[7:3]	RSVD	Reserved (0000 0b).	0
D[2:1]	AIN_WAIT_TIME	Wait time after setting the threshold before the comparator value is not sampled. ■ 0 = 0.5ms ■ 1 = 1ms ■ 2 = 2ms ■ 3 = 4ms	0
D[0]	AIN_CLK_GATE	■ 0 = AIN CLK gate is disabled (AIN clock is enabled). ■ 1 = AIN CLK gate is enabled (AIN clock is disabled).	1

Table 46: AIN Status Register (99h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
AIN_STAT	RO	RSVD	RSVD	RSVD	RSVD	RSVD	AIN_ CMP_2	AIN_ CMP_1	AIN_ CMP_0	0x00	0x99

Bit	Bit Field	Function	Default
D[7:3]	RSVD	Reserved (0000 0b).	0
D[2]	AIN_CMP_2	■ 0 = AIN value is lower than threshold #2. ■ 1 = AIN value is higher than threshold #2.	0
D[1]	AIN_CMP_1	■ 0 = AIN value is lower than threshold #1. ■ 1 = AIN value is higher than threshold #1.	0
D[0]	AIN_CMP_0	■ 0 = AIN value is lower than threshold #0. ■ 1 = AIN value is higher than threshold #0.	0

SOC First Level IRQ

Table 47: Level 1 IRQ Register (84h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
CPU_IRQLVL1	W1C	RSVD			AIN_EVENT	I2C_EVENT	RSVD	REQ_FAIL	RSVD	0x00	0x84

Bit	Bit Field	Function	Default
D[7:5]	RSVD	Reserved (000b).	0
D[4]	AIN_EVENT	■ 0 = No event. ■ 1 = AIN event, to be detailed in second level registers.	0
D[3]	I2C_EVENT	■ 0 = No event. ■ 1 = I^2C event, to be detailed in second level registers Refer to registers AIN_EVENT_IRQ(86h) and AIN_EVENT_IRQ_MASK(87h).	0
D[2]	RSVD	Reserved (0b).	0
D[1]	REQ_FAIL	■ 0 = Violating the request register write rule IRQ not asserted. ■ 1 = Violating the request register write rule IRQ asserted. Refer to registers I2C_EVENT_IRQ(88h) and I2C_EVENT_IRQ_MASK(89h).	0
D[0]	RSVD	Reserved (0b).	0

Table 48: Level 1 IRQ Mask Register (85h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
CPU_IRQLVL1_MASK	R/W	RSVD			AIN_EVENT_M	I2C_EVENT_M	RSVD	REQ_FAIL_M	RSVD	0x0A	0x85

Bit	Bit Field	Function	Default
D[7:5]	RSVD	Reserved (000b).	0
D[4]	AIN_EVENT_M	■ 0 = AIN event IRQ unmasked. ■ 1 = AIN event IRQ masked.	1
D[3]	I2C_EVENT_M	■ 0 = I^2C event IRQ unmasked. ■ 1 = I^2C event IRQ masked.	1
D[2]	RSVD	Reserved (0b).	0
D[1]	REQ_FAIL_M	■ 0 = REQ_FAIL IRQ unmasked. ■ 1 = REQ_FAIL IRQ masked.	1
D[0]	RSVD	Reserved (0b).	0

SOC Second Level IRQ

Table 49: Request Fail IRQ Register (88h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
I2C_EVENT _IRQ	W1C	RSVD	RSVD	RSVD	RSVD	RSVD	I2C_RD _ERR	I2C_VAL _ERR	I2C_ADDR _ERR	0x00	0x88

Bit	Bit Field	Function	Default
D[7:3]	RSVD	Reserved (0000 0b).	0
D[2]	I2C_RD_ERR	■ 0 = No error. ■ 1 = Host master failed to read.	0
D[1]	I2C_VAL_ERR	■ 0 = No error. ■ 1 = Host master wrote wrong or not valid value.	0
D[0]	I2C_ADDR_ERR	■ 0 = No error. ■ 1 = Host master accessed wrong address.	0

Table 50: Request Fail IRQ Mask Register (89h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
I2C_EVENT_IRQ _MASK	R/W	RSVD					I2C_RD _ERR_M	I2C_VAL _ERR_M	I2C_ADDR _ERR_M	0x07	0x89

Bit	Bit Field	Function	Default
D[7:3]	RSVD	RSVD (0000 0b).	0
D[2]	I2C_RD_ERR_M	■ 0 = Read error IRQ unmasked. ■ 1 = Read error IRQ masked.	1
D[1]	I2C_VAL_ERR_M	■ 0 = I^2C Value error IRQ unmasked. ■ 1 = I^2C Value error IRQ masked.	1
D[0]	I2C_ADDR_ERR_M	■ 0 = I^2C ADDR error IRQ unmasked. ■ 1 = I^2C ADDR error IRQ masked.	1

Note: The set bits are cleared when the SoC writes *1* to the corresponding bits

Table 51: AIN IRQ Register (86h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
AIN_EVENT_IRQ	W1C	RSVD	RSVD	AIN_CMP_2_DN	AIN_CMP_1_DN	AIN_CMP_0_DN	AIN_CMP_2_UP	AIN_CMP_1_UP	AIN_CMP_0_UP	0x00	0x86

Bit	Bit Field	Function	Default
D[7:6]	RSVD	Reserved (00b).	
D[5]	AIN_CMP_2_DN	■ 0 = AIN value does not cross the threshold #2 downwards. ■ 1 = AIN value crosses the threshold #2 downwards.	0
D[4]	AIN_CMP_1_DN	■ 0 = AIN value does not cross the threshold #1 downwards. ■ 1 = AIN value crosses the threshold #1 downwards.	0
D[3]	AIN_CMP_0_DN	■ 0 = AIN value does not cross the threshold #0 downwards. ■ 1 = AIN value crosses the threshold #0 downwards.	0
D[2]	AIN_CMP_2_UP	■ 0 = AIN value does not cross the threshold #2 upward. ■ 1 = AIN value crosses the threshold #2 upward.	0
D[1]	AIN_CMP_1_UP	■ 0 = AIN value does not cross the threshold #1 upward. ■ 1 = AIN value crosses the threshold #1 upward.	0
D[0]	AIN_CMP_0_UP	■ 0 = AIN value does not cross the threshold #0 upward. ■ 1 = AIN value crosses the threshold #0 upward.	0

Table 52: AIN IRQ Mask Register (87h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
AIN_EVENT_IRQ_MASK	R/W	RSVD	RSVD	AIN_CMP_2_DN_M	AIN_CMP_1_DN_M	AIN_CMP_0_DN_M	AIN_CMP_2_UP_M	AIN_CMP_1_UP_M	AIN_CMP_0_UP_M	0x00	0x87

Bit	Bit Field	Function	Default
D[7:6]	RSVD	Reserved (00b).	
D[5]	AIN_CMP_2_DN_M	Event where AIN value crosses threshold#2 downwards: ■ 0 = Mask is disabled. ■ 1 = Mask is enabled.	0
D[4]	AIN_CMP_1_DN_M	Event where AIN value crosses threshold#1 downwards: ■ 0 = Mask is disabled. ■ 1 = Mask is enabled.	0
D[3]	AIN_CMP_0_DN_M	Event where AIN value crosses threshold#0 downwards: ■ 0 = Mask is disabled. ■ 1 = Mask is enabled.	0
D[2]	AIN_CMP_2_UP_M	Event where AIN value crosses threshold#2 upwards: ■ 0 = Mask is disabled. ■ 1 = Mask is enabled.	0
D[1]	AIN_CMP_1_UP_M	Event where AIN value crosses threshold#1 upwards: ■ 0 = Mask is disabled. ■ 1 = Mask is enabled.	0
D[0]	AIN_CMP_0_UP_M	Event where AIN value crosses threshold#0 upwards: ■ 0 = Mask is disabled. ■ 1 = Mask is enabled.	0

Failure Events

VR Fault Mechanism

The VR fault mechanism should be used as part of the MxL7080 responsive actions to failures. If the VR fault feature is enabled (RCVLMT bits in RCVCFG (82h) Register >0), the MxL7080 device should attempt to perform several cold reset attempts. The number of attempts should be configurable using RCVLMT. If the number of attempts reached the configured limit, the MxL7080 device should shut down all MxL76500 devices and wait for a cold boot event. All the relevant registers should be accessible by the host to gather event statistics.

To disable the VR fault mechanism, 0x00 should be written to RCVLMT bits in RCVCFG (82h).

The PWRGD_MASK (25h) register should be used to mask individual failures from triggering the VR fault mechanism. In case of a mask (*1*), even if a fault signal is received (via PG of a MxL76500) the VR fault mechanism should not be activated, and the MxL7080 PWRGOOD should not be de-asserted. During reboot attempts, the PMIC_EN input should be ignored for RCVDT duration.

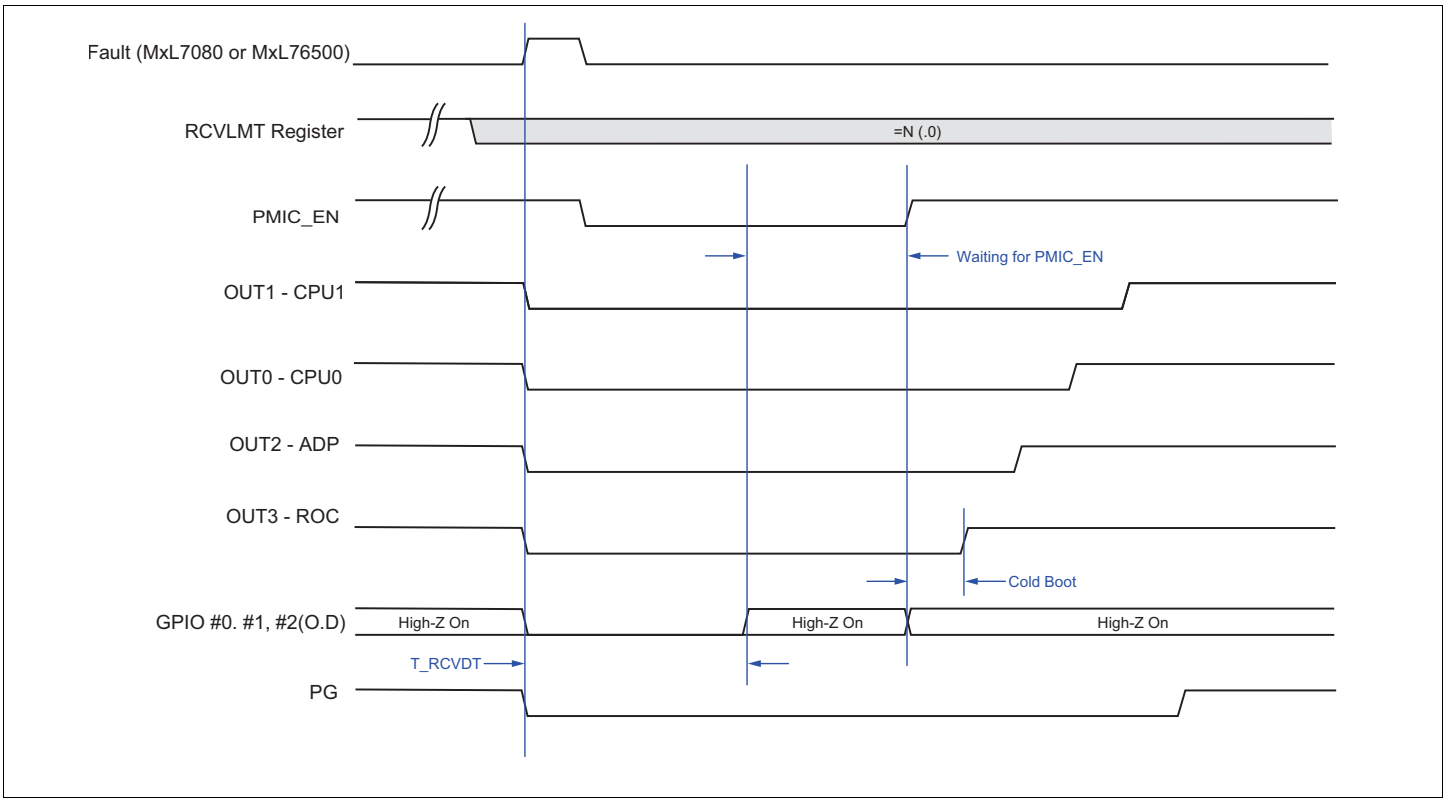


Figure 20: VR Fault Boot Attempt

GPIO signals should change from High-Z On (*Hi*) to Off (*Low*) during the T_RCVDT duration. Once the T_RCVDT expires, the GPIO signal should change from *High-Z Off* back to *Off*.

A PU resistor on the platform ensures that the GPIO signal is *1* which allows the entire platform power chain to boot again. The MxL7080 device should wait to receive the PMIC_EN = 1 to initiate a boot sequence. The rail's output discharge and decay, therefore lower RCVDT timing numbers (<30ms) are not recommended. During reboot attempts, the PMIC_EN input should be ignored for T_RCVDT duration.

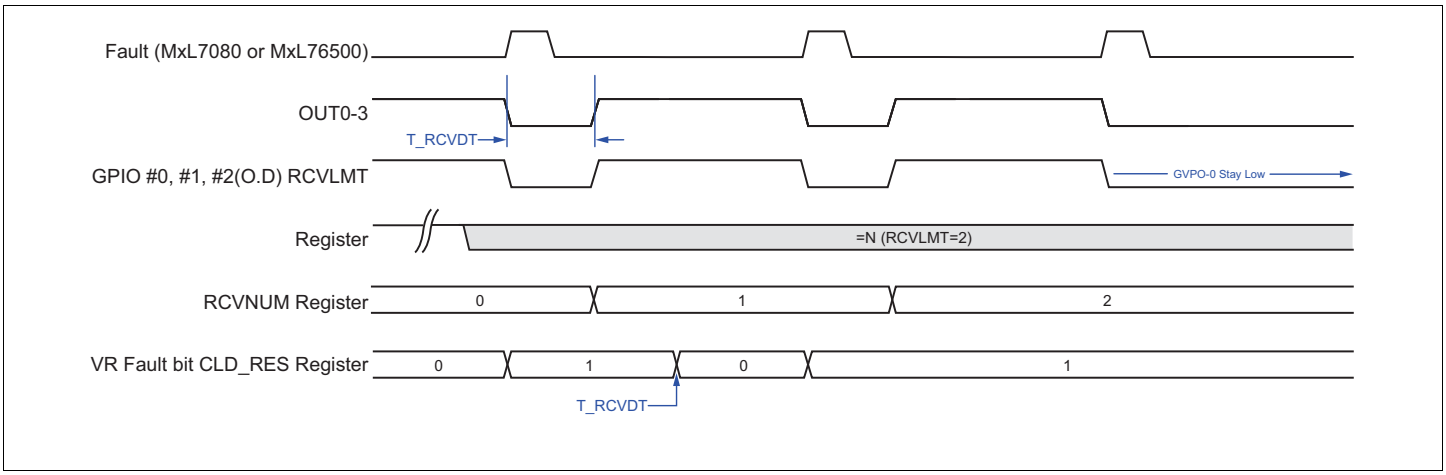


Figure 21: VR Fault Registers Example (RCVLMT = 2)

Table 53: VR Fault Recovery Configuration Register (82h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
RCVCFG	RW	RCVLMT[3:0]				RCVDT[3:0]				0x4F	0x82

Bit	Bit Field	Function	Default
D[7:4]	RCVLMT[3:0]	The maximum number of attempts to recover the power failure, after the VR fault occurred: ■ 0000 = No recovery. MxL7080 stays shut down until a cold boot triggered again. 0001 = 1 time. 0010 = 2 times. …. 1110 = 14 times. ■ 1111 = No limit of attempts to recover.	0x4
D[3:0]	RCVDT[3:0]	The duration time during which the MxL7080 stays in shut down mode following the VR fault event, before performing the a cold boot sequence: ■ 0000 = 5ms ■ 0001 = 10ms ■ 0010 = 15ms ■ 0011 = 20ms ■ 0100 = 25ms ■ 0101 = 30ms ■ 0110 = 35ms ■ 0111 = 40ms ■ 1000 = 45ms ■ 1001 = 50ms ■ 1010 = 75ms ■ 1011 = 100ms ■ 1100 = 250ms ■ 1101 = 500ms ■ 1110 = 750ms ■ 1111 = 1500ms	0xF

Note: RCVDT <30ms is not recommended.

Table 54: VR Fault Recovery Counter Register (83h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
RCVNUM	R/W	RSVD				RCVNUM[3:0]				0x00	0x83

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0000b).	0
D[3:0]	RCVNUM[3:0]	The counter for the actual number of attempts made to recover from the power failure.	0

Event Statistics

Table 55: Cold Reset Reason Register (78h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
CLD_RES	W1C	OUT3_ VRF	OUT2_ VRF	OUT1_ VRF	OUT0_ VRF	RSVD		COLDRST _REQ	VR_ FAULT	0x00	0x78

Bit	Bit Field	Function	Default
D[7]	OUT3_VRF	■ 0 = No VR fault event occurred due to the OUT3PG failure. ■ 1 = VR fault event occurred due to the OUT3 PG failure (MxL76500).	0
D[6]	OUT2_VRF	■ 0 = No VR fault event occurred due to the OUT2 PG failure. ■ 1 = VR fault event occurred due to the OUT2 PG failure (MxL76500).	0
D[5]	OUT1_VRF	■ 0 = No VR fault event occurred due to the OUT1 PG failure. ■ 1 = VR fault event occurred due to the OUT1 PG failure (MxL76500).	0
D[4]	OUT0_VRF	■ 0 = No VR fault event occurred due to the OUT0 PG failure. ■ 1 = VR fault event occurred due to the OUT0 PG failure (MxL76500).	0
D[3:2]	RSVD	Reserved (00b).	0
D[1]	COLDRST_REQ	■ 0 = No cold reset request event occurred. ■ 1 = Cold reset request event occurred.	0
D[0]	VR_FAULT	■ 0 = No VR fault event occurred. ■ 1 = VR fault event occurred (details are in bits 7:4).	0

Table 56: Cold Off Reason Register (79h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
SHDN_RES	W1C	RSVD						PMIC_EN	COLDOFF_REQ	0x00	0x79

Bit	Bit Field	Function	Default
D[7:2]	RSVD	Reserved (0000 00b).	0
D[1]	PMIC_EN	■ 0 = No cold off due to PMIC_EN de-assertion. ■ 1 = Cold off due to PMIC_EN de-assertion.	0
D[0]	COLDOFF_REQ	■ 0 = No cold off request event occurred. ■ 1 = Cold off request event occurred.	0

Table 57: VSYS (VCC) Analog Fault Detection Register (7Ah)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VSYS_DET	W1C	RSVD							VSYS_OV	0x00	0x7A

Bit	Bit Field	Function	Default
D[7:1]	RSVD	Reserved (0000 000b).	0
D[0]	VSYS_OV	■ 0 = No over voltage fault. ■ 1 = Over voltage fault.	0

GPI/O Control Registers

GPO 0

Table 58: GPO0 Control Register (90h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
GPO0_CNTL	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	GPO0_ POL	GPO0_ OUT	GPO0_ MODE	0x00	0x90

Bit	Bit Field	Function	Default
D[7:3]	RSVD	Reserved (0000 0b).	0
D[2]	GPO0_POL	OTP configuration only. GPO0 output polarity and state in case of GPO0_MODE = 0 (MxL7080 state machines) This is also the GPIO state after a cold boot. ■ 0 = Active High (High-Z On). Default value. ■ 1 = Active Low (High-Z Off). Programmable at OTP factory at customer request.	0
D[1]	GPO0_OUT	Depending on OTP configuration, but can be changed by I^2C commands. GPO0 output values in case of GPO0_MODE = 1. ■ 0 = Low (High-Z Off). ■ 1 = High (High-Z On). Default value.	0
D[0]	GPO0_MODE	OTP configuration only, ■ 0 = GPO0 is controlled by the MxL7080 device various sequences and state-machines. LPM, GPO0 output state is programmed by the LPM_MODE register. ■ 1 = GPO0 is controlled by the GPO0_OUT bit of the GPO0_CNTL register. Programmable at OTP factory at customer request.	0

Note: The GPO0 output should be an open-drain pin.

GPIO 1 and GPIO 2

In the case that GPIO1 is selected as an input, then it can be used as an external trigger for MxL7080 to move into LPM mode, similar to the request signal functionality. As an example, the MxL7080 device can be connected to an external real time clock (RTC) device which triggers entering and exiting LPM depending on the time and date. The MxL7080 executes the event which is programmed in the “Request Event Register (29h)” on page 29, same as if it is triggered using the “Request Control Selection Register (28h)” on page 28. The MxL7080 device should override the request option to control the entering and exiting LPM mode.

The following figures show the GPIO1 LPM timing diagrams by highlighting different use cases.

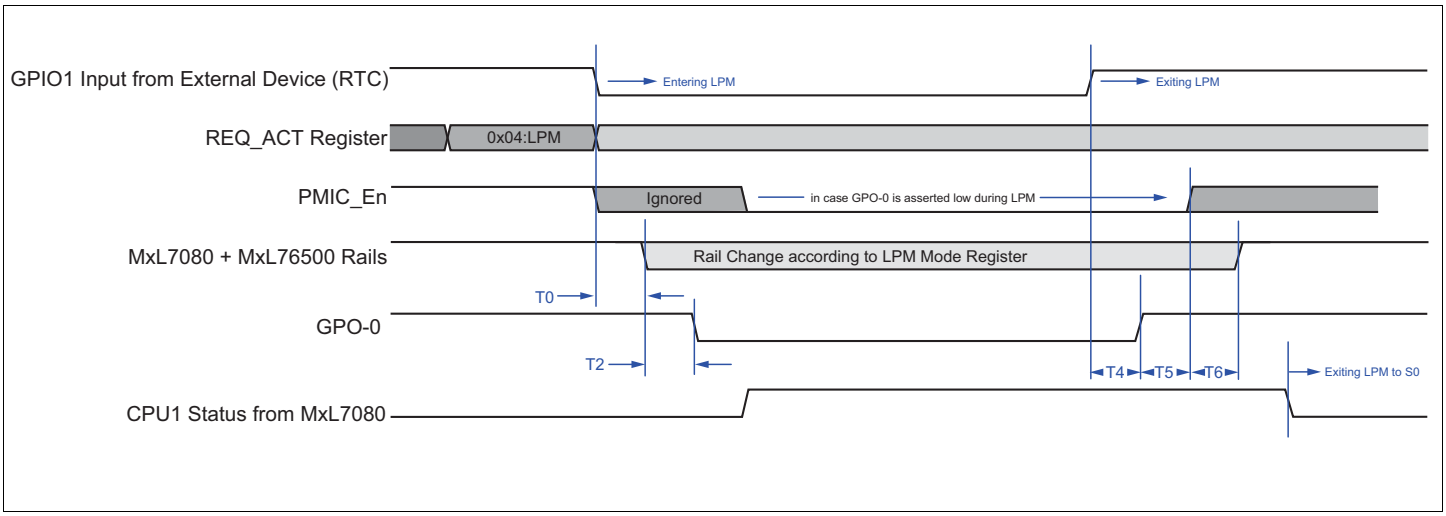


Figure 22: GPIO1 Based LPM Timing Diagram–GPIO_0_LPM = 0 (Neg Edge Example)

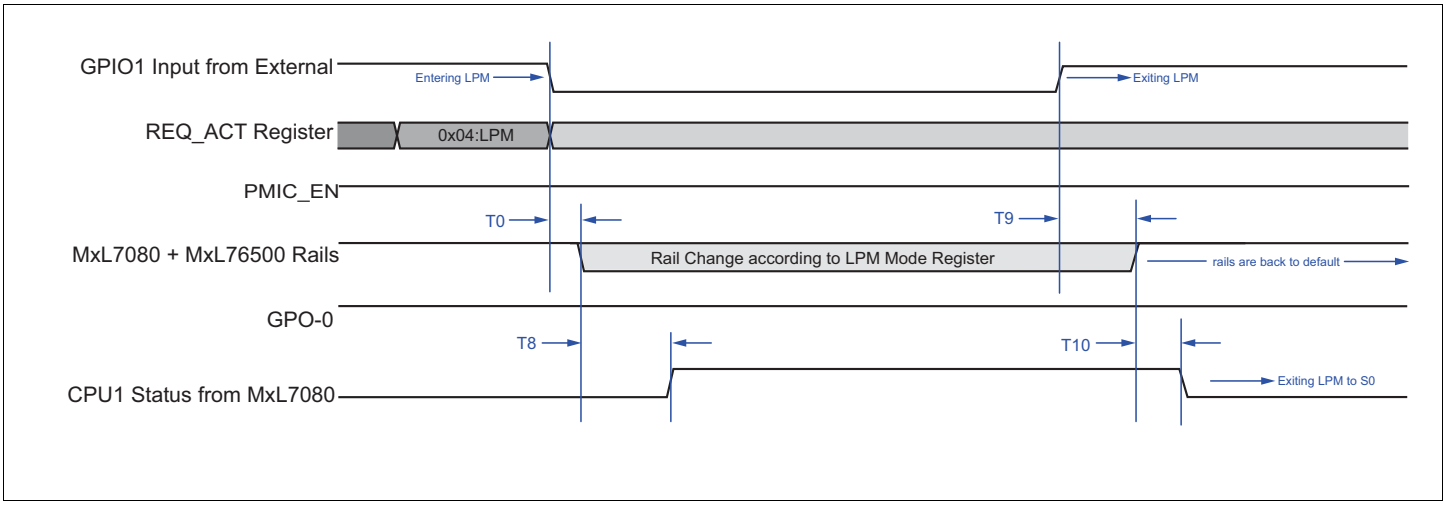


Figure 23: GPIO1 Based LPM Timing Diagram–GPIO_0_LPM = 1 (Neg Edge Example)

Table 59: GPIO1 Control Register (91h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
GPIO1_CNTL	R/W	RSVD	RSVD	GPIO1_ IN_POL	GPIO1_ IN_DIS	GPIO1_ IN_OUT	GPIO1_OUT_ POL	GPIO1_ OUT	GPIO1_ MODE	0x02	0x91

Bit	Bit Field	Function	Default
D[7:6]	RSVD	Reserved (00b).	0
D[5]	GPIO1_IN_POL	Depending on OTP configuration. However, it can be changed by I^2C commands. ■ 0 = GPIO1 Input is entering/exiting LPM using Negedge. Default value. ■ 1 = GPIO1 Input is entering/exiting LPM using Posedge.	0
D[4]	GPIO1_IN_DIS	Depending on OTP configuration. However, it can be changed by I^2C commands. ■ 0 = GPIO1 is controlling the entering/exiting LPM (overriding the request usage). Default value. ■ 1 = GPIO1 Input is disabled (LPM is controlled using the request pin or register).	0
D[3]	GPIO1_IN_OUT	OTP configuration only. ■ 0 = GPIO1 is input. Default value. ■ 1 = GPIO1 is output. Programmable at OTP factory at customer request.	0
D[2]	GPIO1_OUT_ POL	OTP configuration only. GPIO1 output polarity and state in case of GPIO1_MODE= 0 (MxL7080 state machines). This is also the GPIO1 state after a cold boot. ■ 0 = Active High (High-Z On). Default value. ■ 1 = Active Low (High-Z Off). Programmable at OTP factory at customer request.	0
D[1]	GPIO1_OUT	Depending on OTP configuration. However, it can be changed by I^2C commands. GPIO1 output values in case of GPIO1_MODE = 1. ■ 0 = Low (High-Z Off). ■ 1 = High (High-Z On). Default value.	1
D[0]	GPIO1_MODE	OTP configuration only. ■ 0 = GPIO1 is in output mode and is controlled by the MxL7080 device various sequences and state-machines. Default value. In LPM, GPIO1 output state is programmed by the LPM_MODE register. ■ 1 = GPIO1 is controlled by the GPIO1_OUT bit of the GPIO1_CNTL register. Programmable at OTP factory at customer request.	0

Note: The GPIO1 output should be an open-drain pin.

Table 60: GPIO2 Control Register (92h)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
GPIO2_CNTL	R/W	RSVD	RSVD	RSVD	RSVD	GPIO2_ IN_OUT	GPIO2_ OUT_POL	GPIO2_ OUT	AIN_GPIO2 _MODE	0x02	0x92

Bit	Bit Field	Function	Default
D[7:4]	RSVD	Reserved (0000b)	0
D[3]	GPIO2_IN_OUT	OTP configuration only ■ 0 = GPIO2 is input. AIN functionality, if supported. ■ 1 = GPIO2 is output. Programmable at OTP factory at customer request.	0
D[2]	GPIO2_OUT_POL	OTP configuration only. GPIO2 output polarity and state in case of GPIO2_MODE = 0 (MxL7080 state-machine) This is also the GPIO2 state after a cold boot. ■ 0 = Active High (High-Z On). Default value. ■ 1 = Active Low (High-Z Off). Programmable at OTP factory at customer request.	0
D[1]	GPIO2_OUT	Depending on OTP configuration. However, it can be changed by I^2C commands GPIO2 output values in case of GPIO2_MODE = 1. ■ 0 = Low (High-Z Off). ■ 1 = High (High-Z On). Default value.	1
D[0]	GPIO2_MODE	OTP configuration only. ■ 0 = GPIO2 is controlled by the MxL7080 device various sequences and state-machines. In LPM, GPIO2 output state is programmed by the LPM_MODE register. ■ 1 = GPIO2 is controlled by the GPIO2_OUT bit of the GPIO2_CNTL register. Programmable at OTP factory at customer request.	0

Note: The GPIO2 output should be an open-drain pin.

Application Information

System performance can be impacted by the layout. For more information about layout recommendations and guidelines, contact MaxLinear Customer Technical Support.

External Components and Connections

The MxL7080 is simple to use requiring a minimal number of external components to operate. VCC pins 14 and 15 should be shorted together and bypassed to ground with a minimum capacitor value of 1µF. To ensure noise free operation of the DAC outputs, MaxLinear recommends bypassing the input supply with an RC filter. Initial filter values of 10Ω and 2µF are recommended to start with but they can be modified depending upon the application environment.

The DVDD pin 16 should be bypassed to GND with a 1µF capacitor. The I^2C interface to the SoC should be pulled up to the 3.3V system supply.

Routing Recommendations

The first key signal routing requirement is the DAC#_REF and DAC#_GND connection between the MxL7080 and MxL76500. DAC#_REF and DAC#_GND should be routed as a differential pair to the REF_IN and AGND pins on the MxL76500. The MxL76500 pinout does not need those signals crossed.

The FB pin of the MxL76500 is then routed to the SoC sense point. The AGND signal is optimally routed to local GND at the SoC. However, the GND planes between the regulator output caps and the SoC are generally very low impedance, and you can avoid running the AGND trace to the SoC and simply connect to the GND of the output caps (optional routing).

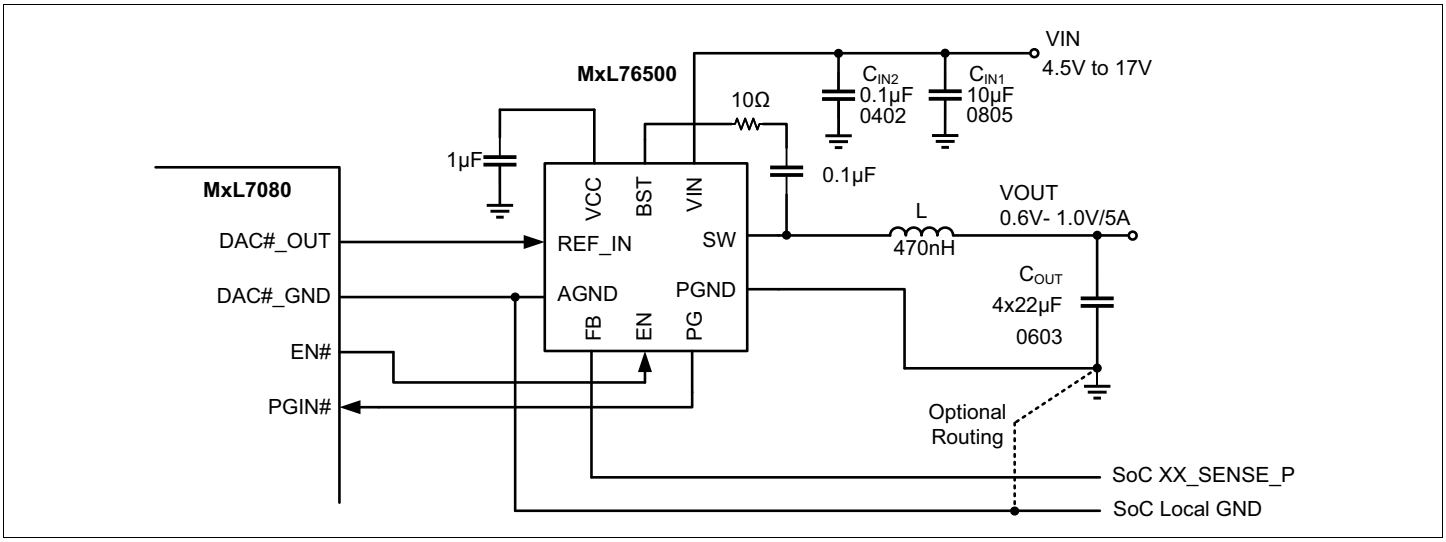
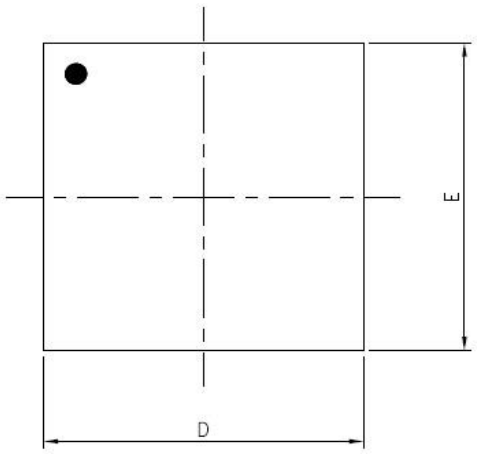


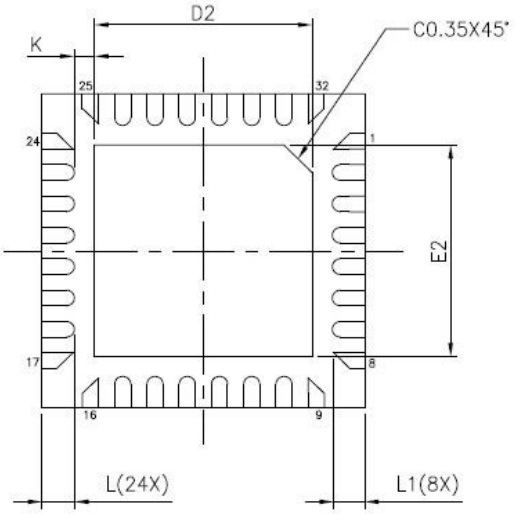
Figure 24: Routing Recommendations from MxL7080 to MxL76500 to SoC

Mechanical Dimensions

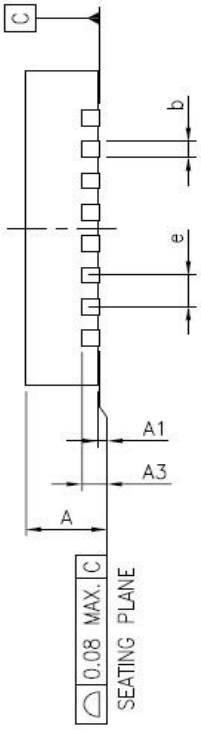
4mm × 4mm QFN



TOP VIEW



BOTTOM VIEW



SIDE VIEW

JEDEC OUTLINE	N/A		
PKG CODE	VQFN (Y432)		
SYMBOLS	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
e	0.40 BSC		
L	0.35	0.40	0.45
L1	0.332	0.382	0.432
K	0.20	-	-

PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
114 x 114 mil	V	X	N/A

NOTE:
1. All dimensions are in millimeters
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

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Figure 25: Packaging Dimensions—4mm × 4mm QFN

Ordering Information

Table 61: Ordering Information

Ordering Part Number	Operating Temperature Range	Package	Packaging Method
MXL7080-AQB-R	$-40°C \le T_a \le 85°C$	4mm × 4mm QFN	Reel

Note: For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/MxL7080.

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