MxL76500

15V, 5A Synchronous Step-Down Regulator for URX8xx/URX6xx SoCs

Data Sheet

General Description

The MxL76500 is a 5A synchronous step-down switching voltage regulator designed to pair with the MxL7080 power manager which interfaces with MaxLinear's AnyWAN™ SoC URX800/600 series and PUMA™ 8 DOCSIS 4.0 SoC.

In a typical system design, four MxL76500 regulators provide the power for CPU0, CPU1, ADP, and ROC rails. The companion MxL7080 device controls the output voltage regulation setpoints including dynamic positioning (DVS) along with sequencing through the MxL76500 REF_IN and enable pins while simultaneously monitoring the PGOOD pins for any faults. If any fault occurs resulting in a latch-off, the MxL7080 power manager restarts the system.

The MxL76500 has a working input voltage range from 4.5V to 15V with 500kHz and 1MHz switching frequency allowing you to trade off size versus efficiency.

The MxL76500 employs a fixed frequency constant on-time (COT) control architecture providing fast transient response. Feedback loop compensation is internal and is designed to work with all-ceramic output capacitors.The MxL76500 can be configured to work in either diode emulation mode (DEM) that improves the efficiency at light or forced continuous conduction mode (FCCM) to maintain constant switching frequency. Dynamic switching between DEM and FCCM is supported.

Protection features include over-current protection (OCP), under-voltage protection (UVP), thermal shutdown, and input under-voltage lockout (UVLO).The MxL76500 is available in a 2mm × 2mm thermally enhanced 10-pin QFN package.

Features

- Power solution for URX800/600 SoCs when paired with MxL7080
- Up to 5A of load current
- Input voltage range from 4.5V to 15V
- Output voltage range from 0.6V to 1.0V
- DVS and soft start controlled by MxL7080
- Latch-off fault
- Fast load transient response
- Excellent line transient rejection
- 500kHz or 1MHz switching frequency
- High light-load efficiency in DEM
- Dynamic switching between DEM and FCCM
- Output over-current protection
- Output under-voltage protection
- Thermal shutdown
- Input under-voltage lockout
- Thermally enhanced 2mm × 2mm QFN package

Applications

- DOCSIS 4.0 modems and gateways
- Fiber optics home gateway unit (HGU)
- Ethernet Wi-Fi home router
- DSL/G.fast home gateway
- Fixed wireless access (FWA) home gateway

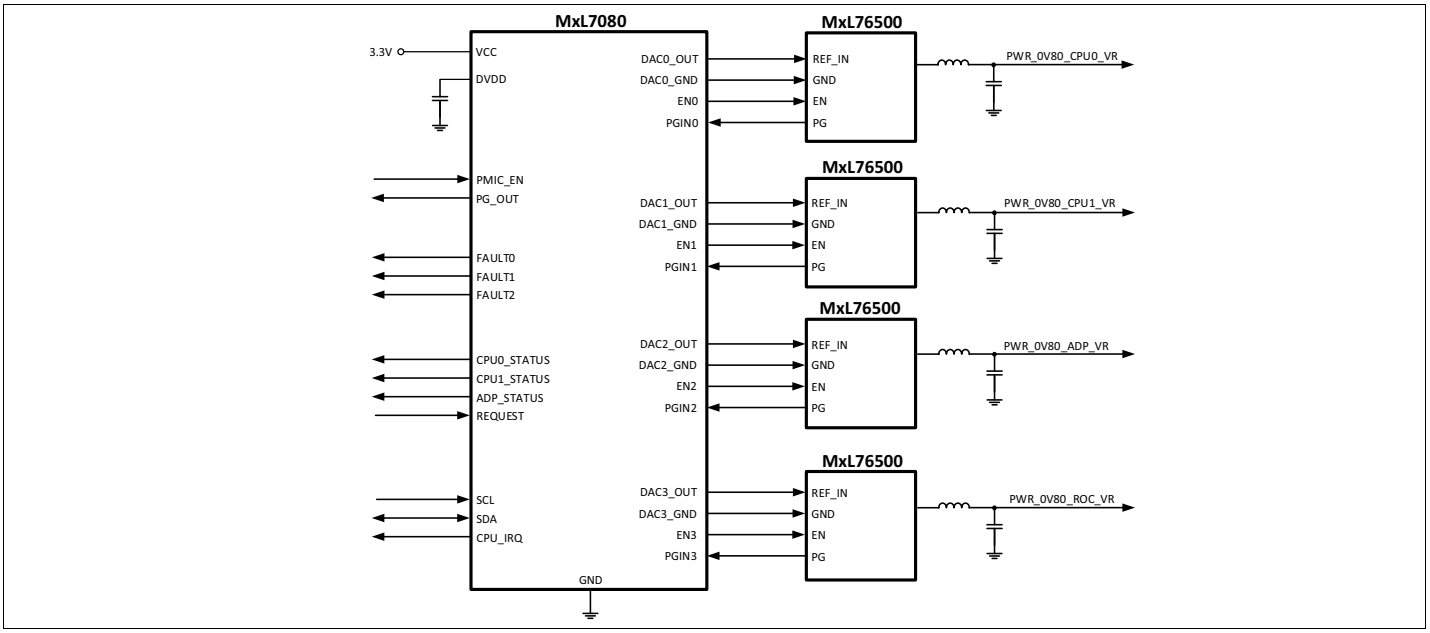

Figure 1: Typical Application

Revision History

Document No.	Release Date	Change Description
289DSR00	March 31, 2026	Initial release.

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Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard. The thermal resistance profile is based on the *JEDEC EIA/JESD51-(2A, 8, 29)* standards.

Table 1: Absolute Maximum Ratings

Parameter	Conditions	Minimum	Maximum	Unit
Supply Voltage VIN	-	-	17	V
SW Pin Voltage	DC	–0.3	VIN + 0.3	V
SW Pin Voltage	AC (10ns)	–2	VIN + 5	V
BST Pin Voltage	-	-	VSW + 6	V
VCC Pin Voltage	-	-	6	V
EN, PG, REF_IN Pin Voltage	-	-	6	V
FB Pin Voltage	-	-	3.6	V
Junction Temperature	-	-	150	°C
Storage Temperature	-	–65	150	°C

Operating Conditions

Table 2: Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage VIN	4.5	15	V
Continuous Output Current	0	5	A
REF_IN Voltage	0	1.0	V
Junction Temperature	–40	125	°C

Table 3: ESD Ratings

ESD Model	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC-001	±2000	V
Charged Device Model (CDM), per JESD22-C101	±500	V

Thermal Specifications

Table 4: Thermal Specifications

Symbol	Parameter	Conditions	Typical	Unit
$\theta_{JC(top)}$	Junction-to-Case Top Thermal Resistance	JEDEC 2s2p 4.5" x 3" PCB with thermal vias. Natural convection. Measured at 1mm from package edge on PCB.	102	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	JEDEC 2s2p 4.5” × 3” PCB with thermal vias. Natural convection. Measured at 1mm from package edge on PCB.	28	°C/W
θ_{JA}	Junction-to-Ambient Thermal Resistance	JEDEC 2s2p 4.5” × 3” PCB with thermal vias. Natural convection.	56	°C/W
Ψ_{JB}	Junction-to-Board Thermal Characteristic	JEDEC 2s2p 4.5” × 3” PCB with thermal vias. Natural convection. Measured at 1mm from package edge on PCB.	32	°C/W

Electrical Characteristics

The • denotes specifications that apply over junction temperature range under "Operating Conditions" on page 1. Otherwise, T_J = 25°C. The typical specifications are T_J = 25°C only.

Table 5: Electrical Characteristics

Symbol	Parameter	Conditions	Temp	Min	Typ	Max	Unit
Supply Current							
I_IN_NS	Input Supply Current, Non-switching	REF_IN = 0.8V, EN > 2.2V, FB = 1V	•	-	320	520	µA
I_IN_SD	Input Supply Current, Shutdown	EN = 0V	•	-	8	20	µA
Switching Frequency							
FSW_1M	Switching Frequency, 1MHz Version	VIN = 12V, VOUT = 1.2V, FCCM, no load		-	1000	-	kHz
FSW_500	Switching Frequency, 500kHz Version	VIN = 12V, VOUT = 1.2V, FCCM, no load		-	500	-	kHz
Enable and Mode of Operation							
V_EN_FCCM	EN Pin Rise Threshold for FCCM Operation	-	•	1.15	1.3	1.4	V
V_EN_DEM	EN Pin Threshold for DEM Operation	EN rising	•	1.9	2	2.2	V
V_EN_HYS	EN Pin Hysteresis	-		-	100	-	mV
T_EN_DLY	Enable Delay	From rising edge of EN to start of switching	•	-	0.5	1	ms
Error Amplifier							
I_FB	FB Pin Input Current	-	•	–100	-	100	nA
V_OFS_EA	Offset between FB and REF_IN	FCCM. Regulator is in steady state and VOUT is regulated.	•	–6	-	6	mV
Protection							
T_TSD_THR	Thermal Shutdown Threshold	-		-	150	-	°C
T_TSD_HYS	Thermal Shutdown Hysteresis	-		-	20	-	°C
V_UVP	FB Trigger Voltage for Output UVP	FB voltage falling toward 0V		-	0.39	-	V
ILIM	Current Limit Threshold	Inductor valley current	•	5.1	6.7	8	A
I_NOC	Negative Current Limit Threshold	Inductor valley current		-	–3.9	-	A
UVLO	Input Under-voltage Lockout Threshold, Rising	VIN rising	•		-	4.4	V
UVLO_HYS	Input UVLO Hysteresis	VIN falling		-	600	-	mV
Power Good							
V_PG_THL	Power Good UV Rising Threshold	FB rising		450	500	550	mV
V_PG_HYS	Power Good Hysteresis	FB falling		-	50	-	mV
V_PG_THU	Power Good OV Upper Threshold	FB rising		1.045	1.1	1.155	V
V_PG	PG Pin Voltage when Power Good is asserted.	Isink = 1mA		-	0.13	0.4	V
Power FETs							
RON_HS	ON Resistance of the Top FET	VCC = 5V, VBST-VSW = 5V		-	48	-	mΩ
RON_LS	ON Resistance of the Bottom FET	VCC = 5V		-	24	-	mΩ

Table 5: Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Temp	Min	Typ	Max	Unit
Others							
T_ON_MIN	Minimum ON Time	-	•	-	90	-	ns
T_OFF_MIN	Minimum OFF Time	-	•	-	400	-	ns
I_ZCD	SW Node Zero Crossing Detector Threshold	Low-side FET source-to-drain current		-	100	-	mA
V_VCC	VCC Pin Voltage	VIN > 5.5V		-	5	-	V

Pin Information

Pin Configuration

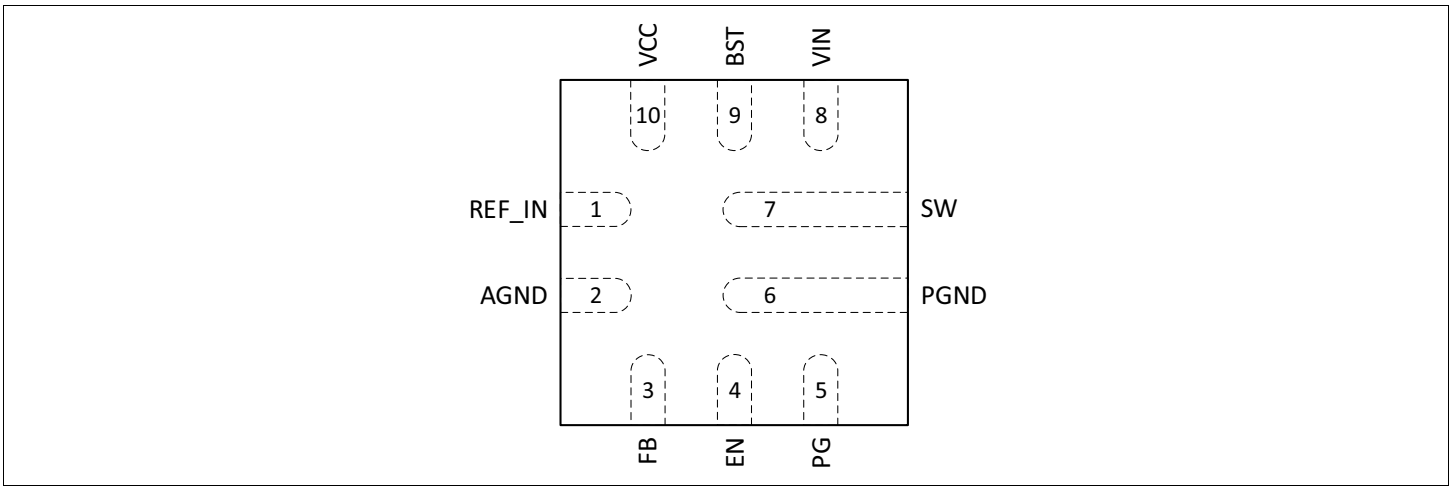


Figure 2: Pin Configuration (Top View)

Pin Description

Table 6: Pin Description

Pin Name	Pin Number	Description
REF_IN	1	Reference voltage input. Voltage applied between this pin and the AGND pin is considered the target output voltage. After the 600µs enable delay, ramp this voltage up from 0V to achieve soft start. During a dynamic voltage scaling (DVS) action, ramp this voltage with desired output voltage slew rate. To actively ramp down the output voltage during DVS, the EN pin needs to be set to FCCM level so that the low-side FET is allowed to conduct negative inductor current.
AGND	2	Ground reference for internal quiet analog circuitry. To achieve remote output voltage sensing, route the AGND and FB traces right next to each other to the desired point of regulation.
FB	3	VOUT feedback connection. Connect this pin directly to VOUT. To achieve VOUT remote sensing, run the FB trace in parallel with and right next to the AGND trace all the way to the desired point of regulation.
EN	4	Soft-start enable and DEM/FCCM select. Bring this pin above 1.35V to operate in FCCM or above 2.2V to operate in DEM. Dynamic switching between FCCM and DEM is allowed. Before the REF_IN pin reaches 550mV (typical), part always operates in DEM, even if the EN is above FCCM threshold and below the DEM threshold.
PG	5	Open-drain power good indicator. An internal MOSFET between this pin and PGND turns off once FB voltage is above 500mV (typical). The internal MOSFET is open-drain when EN is low or there is no input power.
PGND	6	Power ground. Connect to system power ground plane where input and output capacitors connect to.
SW	7	Switch node. This pin connects to the source of the internal high-side NFET and drain of the internal low-side NFET. Connect a 0.1µF capacitor between this pin and the BST pin to provide power for the high-side FET drive.
VIN	8	Input supply. Place a 1µF 0402 ceramic capacitor between this pin and PGND pin as close to the IC as possible to reduce switching ringing.
BST	9	Bootstrap pin. Connect a 0.1µF ceramic capacitor between this pin and the SW pin to provide power for the top FET gate drive.
VCC	10	Output of the internal linear regulator. Decouple the VCC LDO with a 0603 4.7µF X7R type ceramic capacitor between this pin and PGND.

Typical Performance Characteristics

V_{IN} = 12V, T_A = 25°C, f_{SW} = 1MHz, unless otherwise noted.

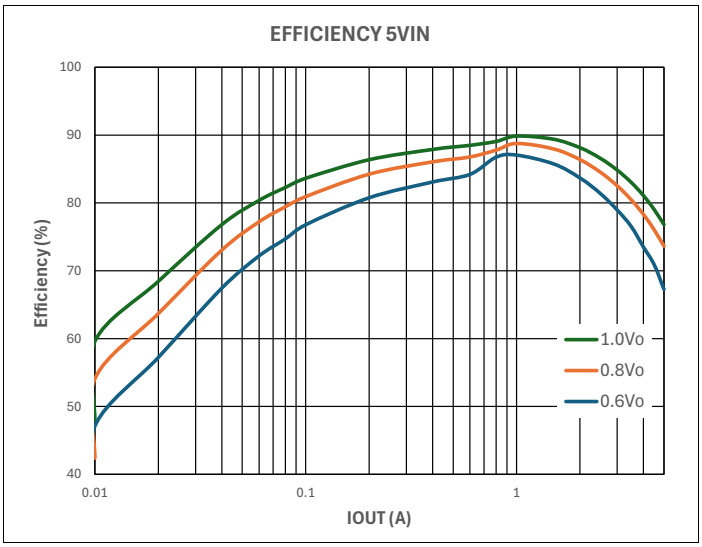


Figure 3: MxL76500C Efficiency 5V_{IN} 500kHz

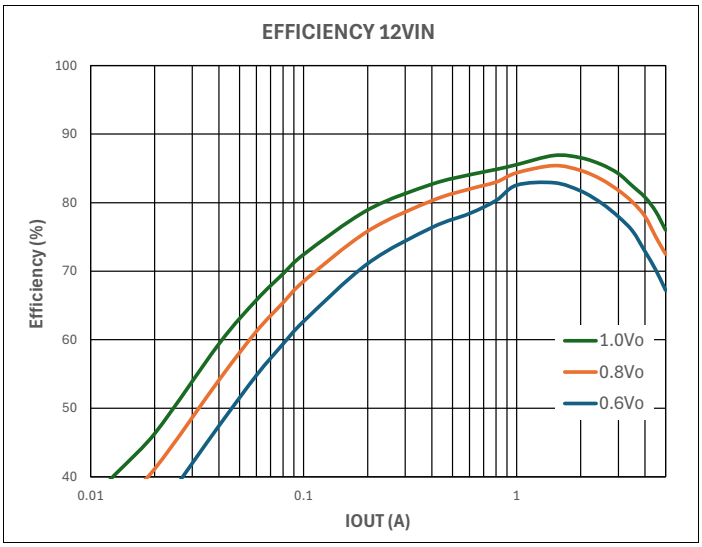


Figure 4: MxL76500C Efficiency 12V_{IN} 500kHz

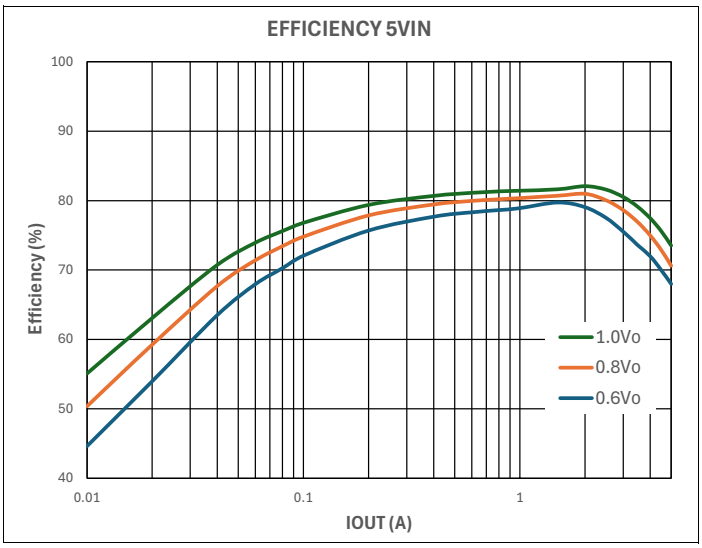


Figure 5: MxL76500D Efficiency 5V_{IN} 1MHz

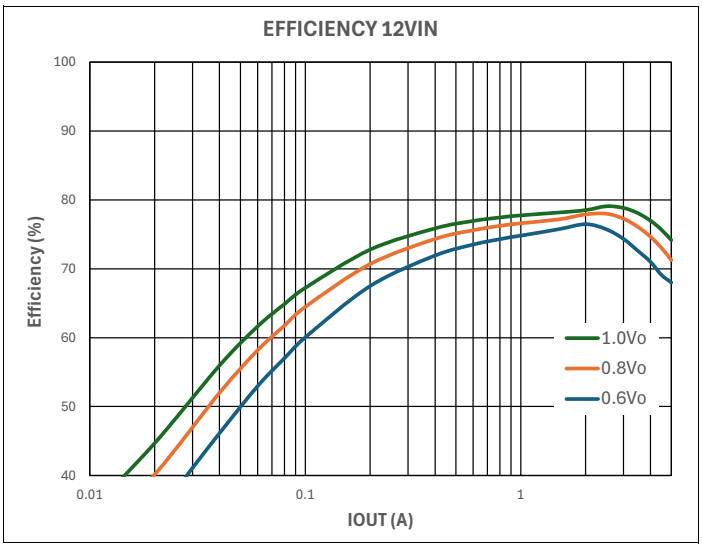


Figure 6: MxL76500D Efficiency 12V_{IN} 1MHz

Table 7: Inductor Information (500kHz)

MxL76500C (500kHz)		
V_{OUT} (V)	Inductor (µh)	DCR (mΩ)
1	1	5.2
0.8	1	5.2
0.6	1	5.2

Table 8: Inductor Information (1MHz)

MxL76500D (1MHz)		
V_{OUT} (V)	Inductor (µh)	DCR (mΩ)
1	0.47	4.6
0.8	0.47	4.6
0.6	0.47	4.6

V_{IN} = 12V, V_{OUT} = 0.8V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

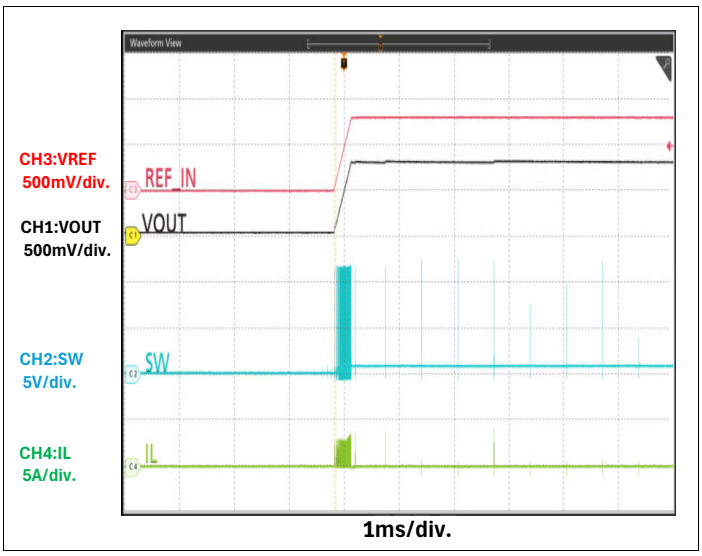


Figure 7: Start-up through REF_IN, Load = 0A

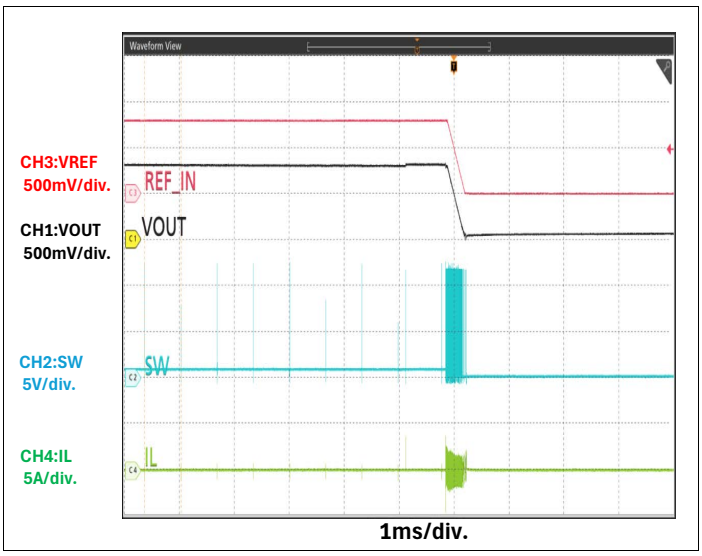


Figure 8: Power-down through REF_IN, Load = 0A

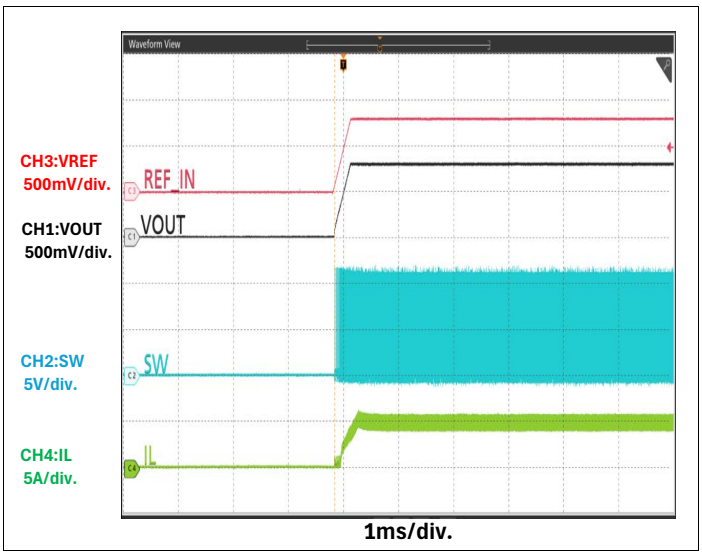


Figure 9: Start-up through REF_IN, Load = 5A

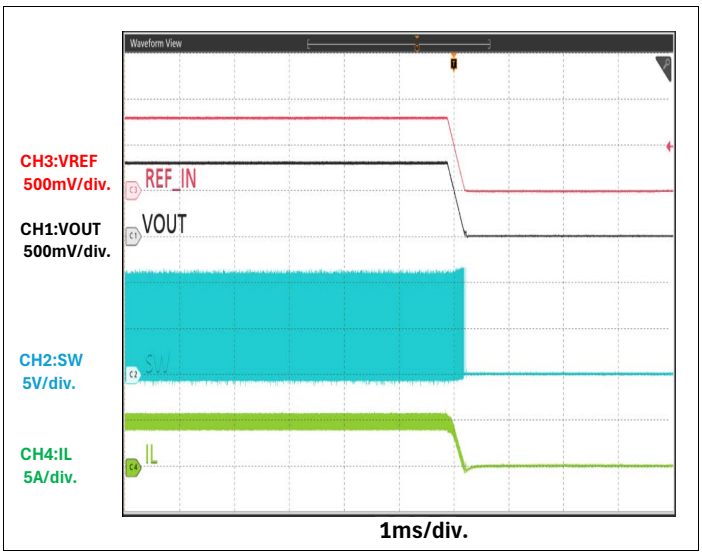


Figure 10: Power-down through REF_IN, Load = 5A

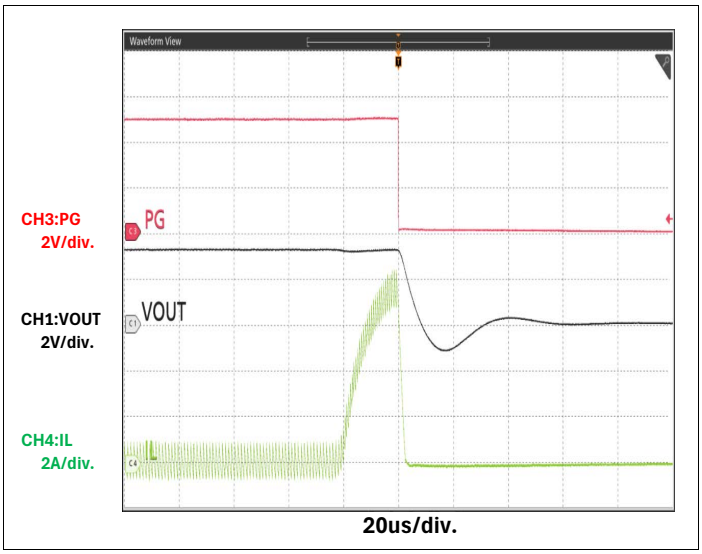


Figure 11: Over-Current Protection Entry

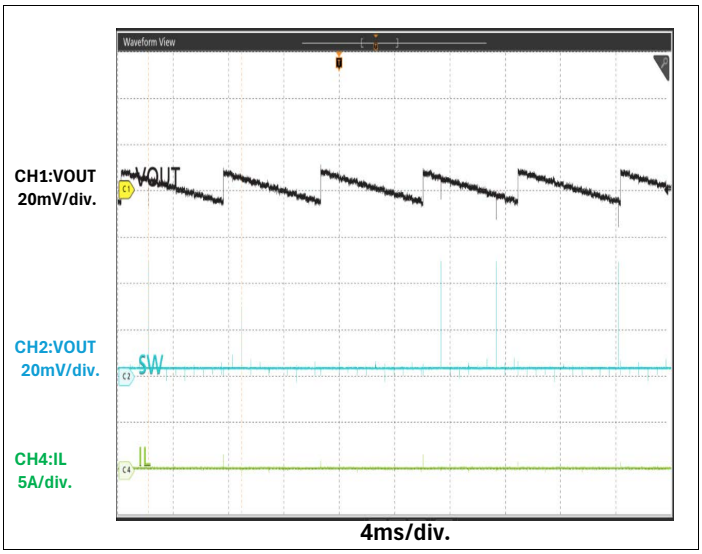


Figure 12: Output Ripple, Load = 0A

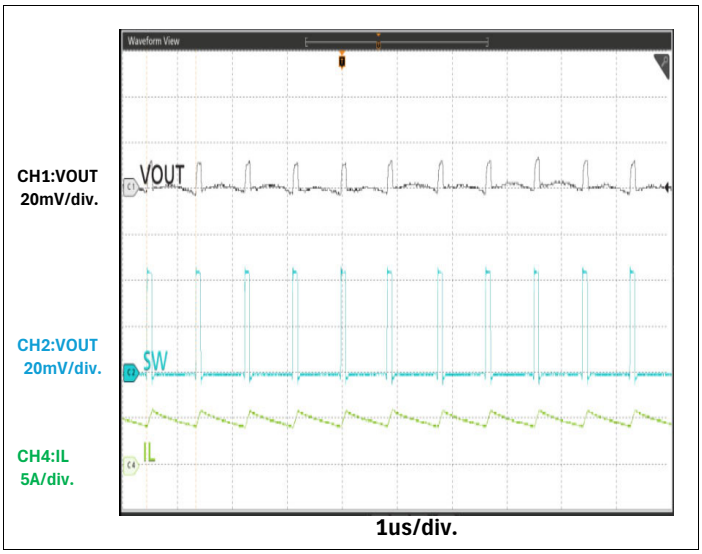


Figure 13: Output Ripple, Load = 5A

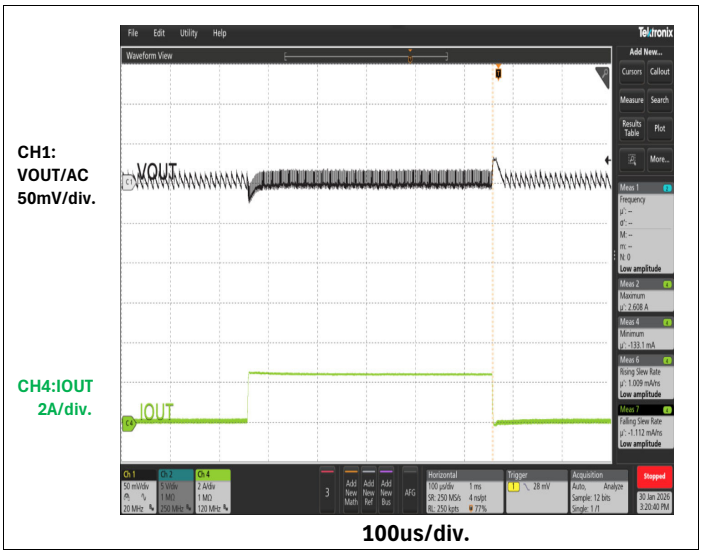


Figure 14: Load Transient Response, I_{OUT} = 0A–2.5A–0A, Slew Rate = 1A/µs

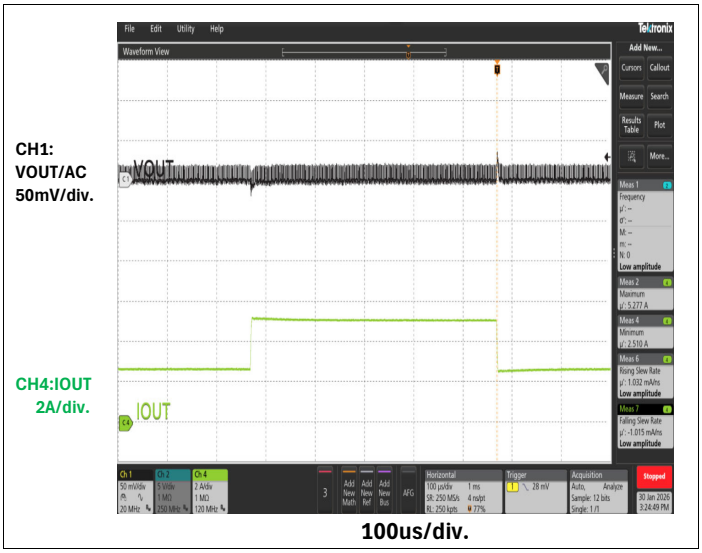


Figure 15: Load Transient Response, I_{OUT} = 2.5A–5A–2.5A, Slew Rate = 1A/µs

Block Diagram

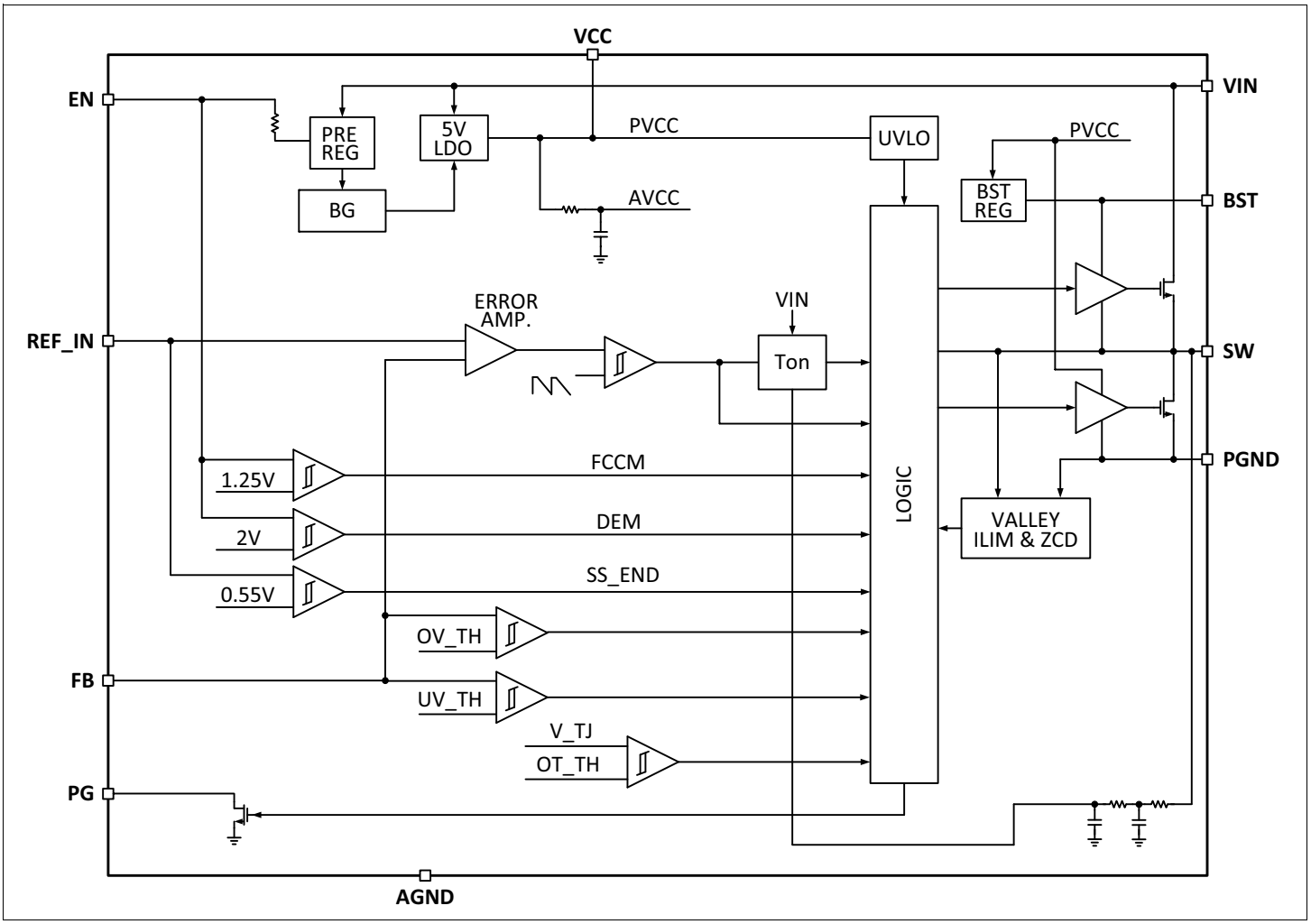


Figure 16: Functional Block Diagram

Functional Description

Overview

The MxL76500 is a fully integrated, monolithic, synchronous step-down switched-mode converter capable of 5A continuous current, and designed to operate in conjunction with the *MxL7080 URX800/URX600 Power Manager Data Sheet* (257DS).

The solution shown in Figure 17 meets all the requirements of the URX85x, URX65x, and MxL256xx AnyWAN™ Broadband SoC's core rail requirements. The MxL7080 controls the MxL76500 regulators through three interfaces: the ENx output controls the EN pin of the MxL76500 device, the PGINx input monitors for faults detected by the MxL76500 device,
and a DAC output acts as the reference voltage to the control loop to provide dynamic voltage control (DVS).

This *disintegrated* approach versus an all-in-one PMIC minimizes thermal challenges while providing single stage power conversion from standard 12V inputs.

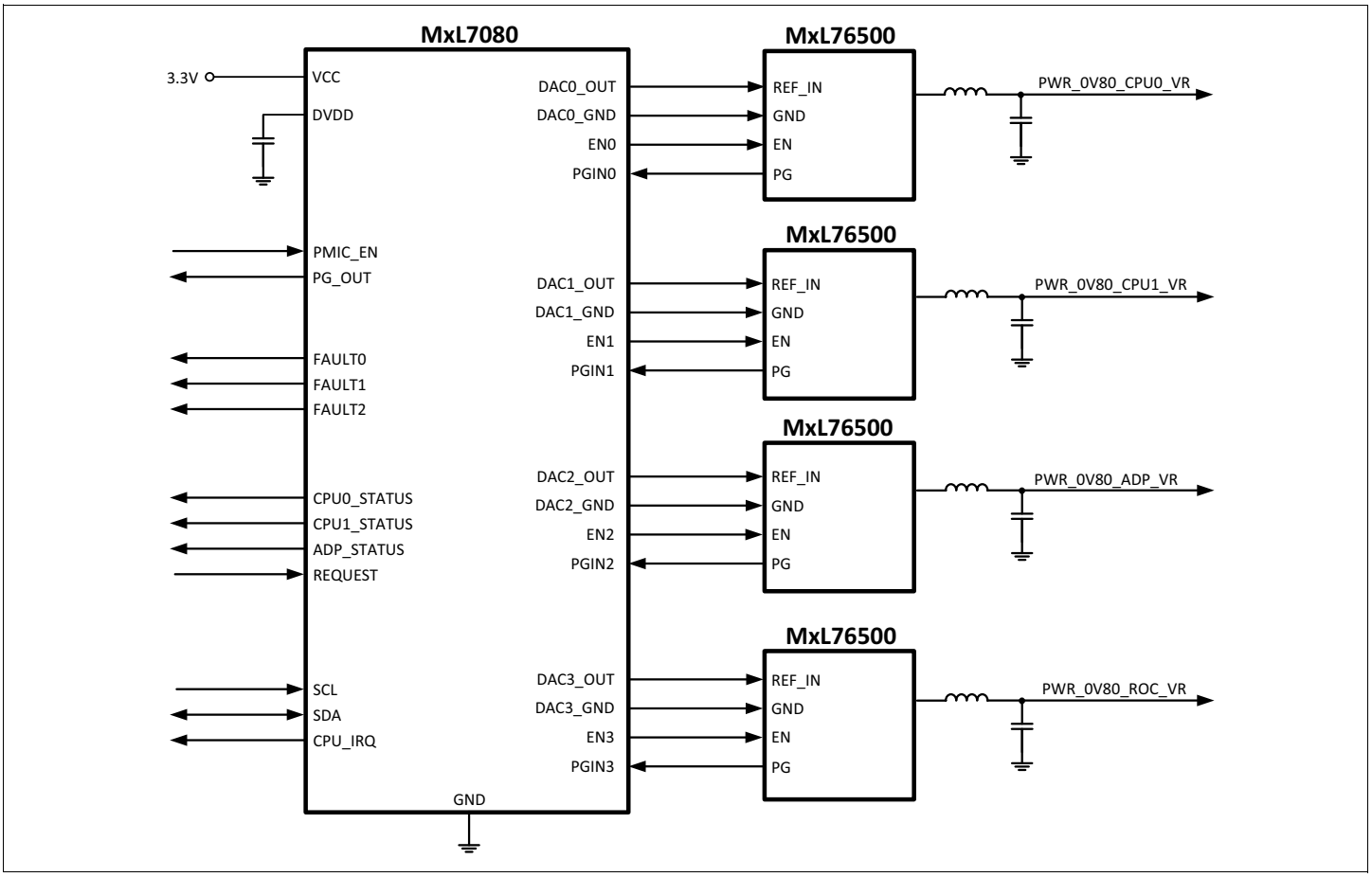


Figure 17: High Level Application Circuit

Control Loop

The MxL76500's feedback control is based on an adaptive voltage-mode constant on-time (COT) mechanism. Loop stability is achieved through adaptive on-time control with an internally compensated error amplifier feeding a comparator. The error amplifier inputs are the reference voltage provided by the MxL7080 at the REF_IN pin and the output voltage connected to the FB pin. The error amplifier output is compared to a compensating ramp which ensures stability when using ceramic output capacitors. Response to a large unloading transient is aided by voltage clamps in and around the error amplifier circuit.

MxL7080 ENx Pin to MxL76500 EN Pin Functionality

The MxL7080 ENx output feeds the EN pin of the MxL76500 to enable and disable the device or to change the operating mode from either forced continuous conduction mode (FCCM) or diode emulation mode (DEM).

In FCCM, the high-side and low-side MOSFETs operate fully synchronously, which keeps the switching frequency fairly constant. The inductor current can swing both positive and negative. At high load currents, the inductor current is always above 0A. At lower load currents, the inductor current can go below 0A.

In DEM, a zero-crossing detector circuit is activated, which turns off the low-side MOSFET. This in turn prevents negative current flow, thus emulating the functionality of a diode. As the load or output current decreases, the inductor current decreases. When the inductor current reaches 0A, the MOSFET operation transitions to discontinuous conduction mode (DCM). In DCM operation, the on-time remains constant while the off-time increases as the load current decreases. This lowers the switching frequency, thereby improving light-load efficiency.

DEM operation is the normal operating mode for the MxL76500 unless a DVS command is given. When a DVS command from the processor is received, the MxL7080 commands FCCM through the EN pin. FCCM operation is needed for negative DVS commands to ensure that the output capacitors can be discharged and the output reaches the command voltage in a controlled manner, even under light-load conditions. Once the DVS is complete, the MxL7080 returns the EN pin voltage of the MxL76500 to DEM operation.

Start-up

When the MxL76500 device begins a start-up sequence for a given output, the EN# goes high and the DAC#_OUT ramps after a ~600µs delay. The output ramps to 800mV at rate 2.5mV/µs upon initial boot. The power good (PG) pin on the MxL76500 goes high after the output reaches ~500mV, although the state of PG is ignored by the MxL7080 until the DAC output has completed ramping.

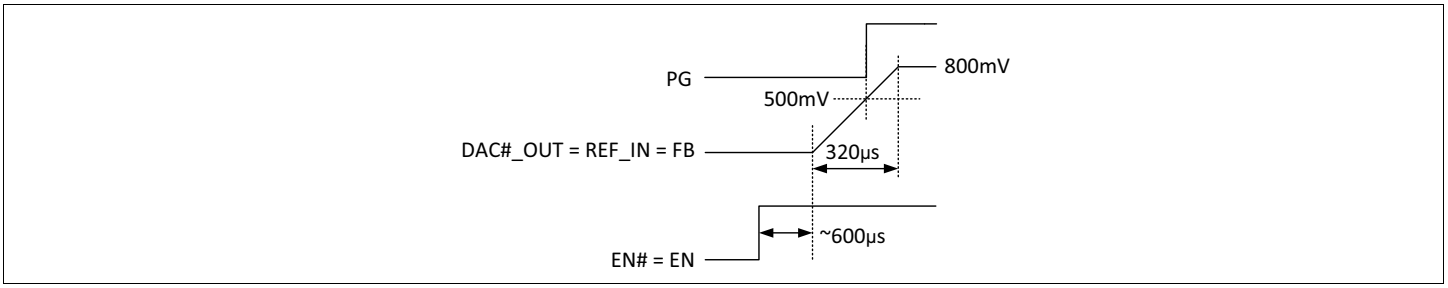


Figure 18: Start-up Sequence and Timing

During start-up when PG is low, under-voltage protection (UVP) is disabled but over-current protection (OCP), over-temperature protection (OTP), and over-voltage protection (OVP) are all enabled. Note that if a fault condition is present and PG remains low, the MxL7080 does not detect this until the DAC ramp is complete.

In the case of a pre-biased start-up where the output voltage is greater than 0V to begin with, both high-side and low-side FETs remain off until the SS (REF_IN) pin reaches the pre-biased FB voltage. This behavior prevents output capacitor from being discharged and provides a monotonic voltage ramp during start-up.

Shutdown

When the MxL7080 device initiates a shutdown, it ramps the DAC to 0V at 2.5mV/µs and then pull the EN pin low.

Over-Current Protection (OCP)

The MxL76500 monitors the current in the low-side MOSFET. During each switching cycle when the feedback loop attempts to turn on the high-side FET, if the sensed low-side FET current is higher than 6.7A, an OCP counter increments by 1 and the high-side FET is not allowed to turn on until the current drops below 6.7A. Otherwise, the high-side FET is turned on and the OCP counter resets to 0. If the OCP counter counts to four, the MxL76500 turns off both FETs, pulls PG low, and remains non-operational in a latched off OCP protection state. To recover out of the OCP protection mode, the MxL7080 must cycle the EN pin and initiate a re-start.

Negative Over-Current (NOC)

When operating in DEM, the negative instantaneous current limit is 0A, meaning the low-side MOSFET is emulating the operation of a diode. When in FCCM, that current limit is changed to –3.9A instantaneous current. During a negative DVS event, there can be significant negative current in the inductor to discharge the output capacitance. The negative inductor current limit protects the device from being damaged. If the instantaneous inductor current becomes more negative than –3.9A, the NOC circuit turns off the low-side FET and turns on the high-side FET for one on-time. Afterwards, the feedback loop takes back the control. A NOC event only causes early termination of the off-time of the present cycle. During the next cycle, the low-side FET is allowed to turn on again. If NOC occurs during a negative DVS, the output voltage trails the `REF_IN` voltage, which is a normal function of the device. Operation of the SoC is not affected.

When the device is operating in DEM, during a load release that moves the operating point from CCM to DCM the –3.9A, NOC is active for the first four switching cycles before reverting to DEM. Allowing a few cycles of negative current improves unloading transient response.

Over-Temperature Protection (OTP)

During operation, if the die temperature exceeds 160°C, the MxL76500 turns off both FETs, shuts down, and PG pulls low. The MxL7080 powers down the system and then initiates a re-start.

Over-Voltage Protection (OVP)

Over-voltage protection (OVP) protects the device and SoC when a higher external voltage is inadvertently connected to the output of the regulator. As the output voltage rises above ~1.1V of the set point, PG is pulled low and the MOSFETs are switched to tri-state. The MxL7080 powers down the system and then initiates a re-start.

Power Good (PG) Flag

The power good (PG) pin is an open-drain signal which indicates whether VOUT is within ~0.5V to ~1.0V. When outside the regulation window or a fault has occurred, the PG pin pulls low.

During start-up, PG is initially low. After the REF_IN pin exceeds 500mV and the output is within the PG window, the PG pin goes high impedance, asserting power good.

When VIN is lower than the UVLO threshold, the PG pin is in high-impedance state. This does not indicate a power good state.

Under-Voltage Protection (UVP)

If the FB pin is quickly pulled down to <0.39V during normal operation, under-voltage protection (UVP) is triggered, in which case the MxL76500 turns off both FETs and pulls PG low. The MxL7080 powers down the system and then initiates a re-start.

UVP is disabled during start-up although most events resulting in UVP cause an OCP event during start-up.

Recovering from a Fault

Upon triggering OCP, UVP or OTP, the MxL76500 turns off both FETs and pulls PG low. It remains in that state until EN is toggled or the input power is cycled. In the event of a fault, the MxL7080 powers down the system and then initiates a re-start.

Application Information

The MxL76500 is a fully integrated, monolithic synchronous buck switching regulator that works with an input ranging from 4.5V to 15V and regulates an output from 0.6V to 1.0V. The maximum continuous load current rating is 5A within thermal limits of the device. The switching frequency of the MxL76500D is 1MHz. The following figure shows a design example utilizing the 1MHz MxL76500D together with the MxL7080.

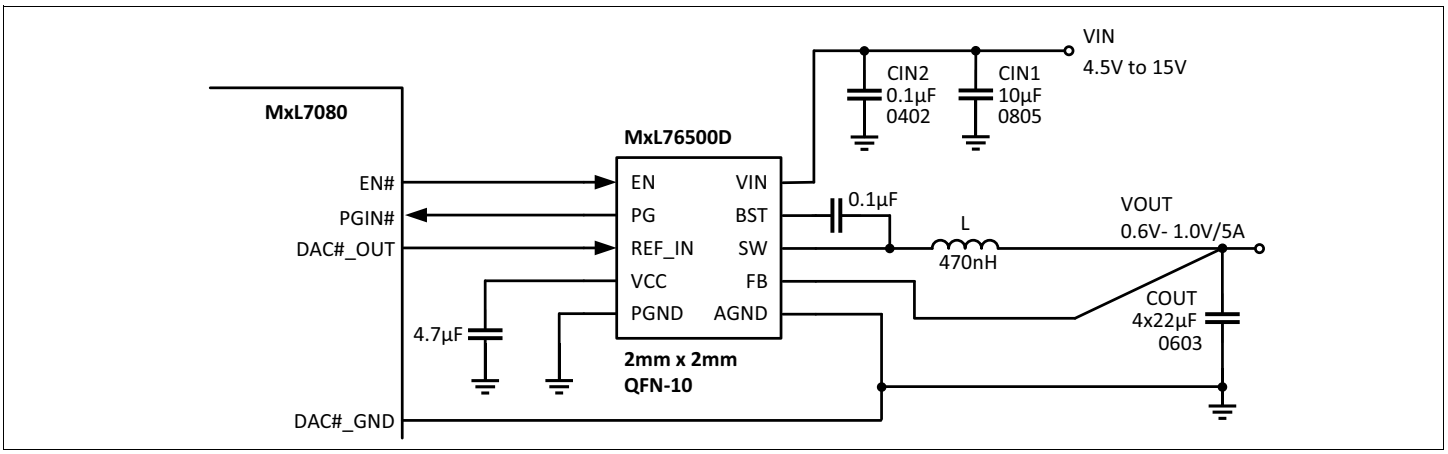


Figure 19: URX8xx/6xx Application Schematic

Bootstrap Capacitor

MaxLinear recommends using a 0.1µF ceramic capacitor for the bootstrap capacitor which is connected between the SW pin and the BST pin. MaxLinear also recommends using a 22Ω resistor in series with this capacitor to reduce ringing on the switch node and reduce high-frequency conducted electromagnetic interference (EMI).

VCC Capacitor

MaxLinear recommends using a 4.7µF X7R ceramic capacitor of 0603 size or smaller for the capacitor between the VCC and PGND pins.

Input Capacitors

The devices require input decoupling capacitors on the power supply input, VIN. The function of the input capacitors (C_{IN}) is to provide the AC component of the input current, reducing both conducted noise emitted back to the input voltage rail as well as ripple voltage seen by the VIN pin. MaxLinear recommends using high-quality X5R or X7R input decoupling capacitors. The MxL76500 uses a 10µF to 22µF 0805 for primary bypassing and a 0.1µF 0402 for high frequency bypassing. Pay attention to inductive loops which are described in the “Layout Guidelines” on page 17.

Based upon having an input ripple requirement (VIN_{ripple}), the minimum input capacitance required is as follows:

$$C_{IN(min)} = \frac{I_{OUT} \cdot V_{OUT}}{VIN_{ripple} \cdot VIN \cdot f_{SW}}$$

Ensure that the input capacitor RMS current rating matches the application requirements. That current can be calculated as follows:

$$I_{in\_ac\_rms} = IOUT\sqrt{D \cdot (1 - D)}$$

Where D is the CCM duty cycle approximately equal to VOUT/VIN, and $I_{in\_ac\_rms}$ is the RMS value of the AC current that flows through the capacitors. Manufacturers of capacitors can provide curves of temperature rise versus AC RMS current.

Output LC Filter and Feedback Loop Stability

The internal loop compensation of the MxL76500 puts certain requirements on the values of the output inductor and output capacitors to ensure stable operation. The choice of the LC filter components is also key to overall transient performance and in the case of the inductor, efficiency.

The control loop of the MxL76500 is optimized for ceramic output capacitors. Since the feedback loop compensation network is internal and fixed, the double-pole frequency of the output LC filter needs to be bounded to achieve a stable loop. Since the application of the MxL76500 is very specific, use the schematic shown in Figure 19 on page 15 for CP0/1, ADP, and ROC power rails of the URX SoC.

Specifying the Inductor

There are three main factors in specifying a suitable inductor: inductance, saturation current, and power loss. The nominal inductance value used with the MxL76500D is 470nH. The inductors should be rated for an RMS current of >4A and a saturation current of >6A. Larger inductors generally result in lower DC resistance. For example, 5mΩ lower DCR improves efficiency by 1.9% @ $0.8V_{OUT}$, 3A. Practical inductors for this application range from 20mΩ to 3mΩ. The following table list some examples.

Table 9: Inductor Examples

Manufacturer	Manufacturer PN	IRMS (A)	ISAT (A)	DCR (nom mΩ)	Size (L×W×H mm)
Murata	DFE252010F-R47M	4.4	6.0	20.0	2.5×2×1
Cyntec	HBTD043T-R47MS	21.0	21.0	3.2	4.1×4.1×3
Cyntec	HBTD042T-R47MS	19.7	14.5	4.0	4.1×4.1×2
Wurth	744393240047	17.1	19.2	4.5	4.3×4.3×3.2

Layout Guidelines

The second layer should be used as an internal PGND plane. Minimize the distance between the top layer and the second layer, if possible. For more information, see Figure 19 on page 15 and Figure 22 on page 19. The MxL76500 is mounted on the top layer.

1. The high frequency 0.1µF 0402 bypassing capacitor uses the 2nd layer PGND plane to minimize the effective loop length. This reduces inductance to a minimum making the capacitor more effective at bypassing HF content of the AC input current. The return current on the second layer does not follow a direct path back but tends to follow the same path as the current on the top layer due to coupling.
2. Place four or more PGND vias in the area between the PGND and PG pins.
3. Assign as much copper as allowed to the VIN and PGND pins to help keep the MxL76500 cool. In this case, VIN has via connections to the large 12V power plane on an inner layer.
4. Place the VCC capacitor as close as possible to the VCC pin. Add PGND vias right next to the C_{VCC} PGND pin.
5. C_{BST} is on the bottom layer connecting to R_{BST} on the top layer which is close to the BST pin.
6. If remote ground sensing is desired, connect the AGND pin to the PGND net at the remote sensing location. Otherwise, short the AGND net to the PGND net at the AGND pin.
7. Place feedback voltage divider, RFB1 and RFB2, close to the FB pin.
8. VOUT feedback trace should avoid passing under the inductor or overlap with any SW traces.

PCB Layouts

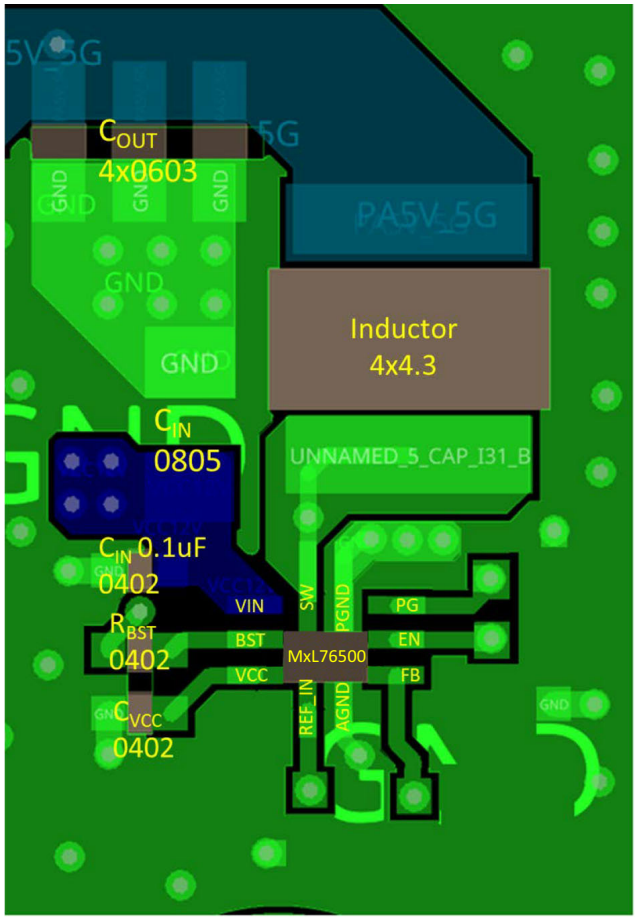


Figure 20: Recommended PCB Layout—Top Layer

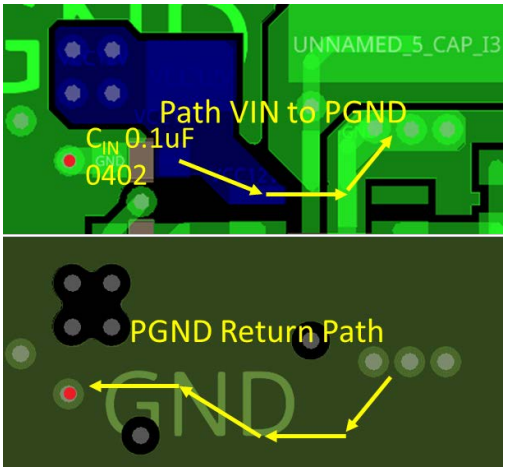
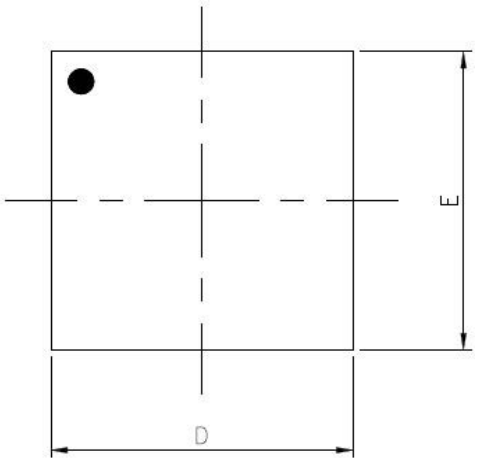


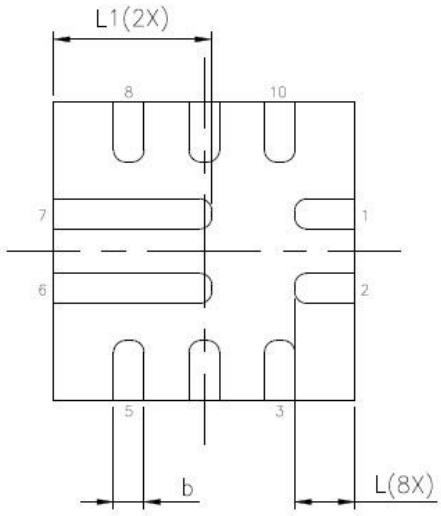
Figure 21: Recommended PCB Layout—2nd Layer HF PGND Return

Mechanical Dimensions

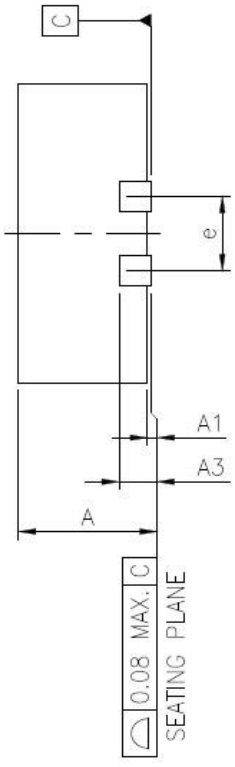
2mm × 2mm QFN



TOP VIEW



BOTTOM VIEW



SIDE VIEW

JEDEC OUTLINE	N/A		
PKG CODE	VQFN		
SYMBOLS	**MIN**	**NOM**	**MAX**
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	0.50 BSC		
L	0.35	0.40	0.45
L1	1.00	1.05	1.10

PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
	V	X	N/A

NOTE:
1. All dimensions are in millimeters
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

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Figure 22: Mechanical Dimensions—2mm × 2mm QFN

Ordering Information

Table 10: Ordering Information

Ordering Part Number	Frequency	Fault Handling	Package	T_J Range	Packing Method	SPQ	Lead Free
MXL76500C-AQF-R	500kHz	Latch	2 × 2mm QFN-10	–40°C to 125°C	Tape and Reel	5000	Yes
MXL76500D-AQF-R	1MHz	Latch	2 × 2mm QFN-10	–40°C to 125°C	Tape and Reel	5000	Yes
MXL7080-EVK-1	MxL7080 Evaluation Kit						

Note:

- For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/MxL76500 and www.maxlinear.com/MxL7080.
- For more information about the EVK, refer to the *MxL7080/MxL76500 EVK User Manual* (041UM).

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
Tel.: +1 (760) 692-0711
Fax: +1 (760) 444-8598

www.maxlinear.com