General Description

The XRT75R12 is a twelve channel, fully integrated Line Interface Unit (LIU) featuring MaxLinear's R^3 Technology (Reconfigurable, Relayless Redundancy) for E3, DS3, and STS-1 applications. The LIU incorporates 12 independent receivers, transmitters and jitter attenuators in a single 420 lead TBGA package.

Each channel of the XRT75R12 can be independently configured to operate in E3 (34.368MHz), DS3 (44.736MHz) or STS-1 (51.84MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75R12's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12dB of cable attenuation.

Each channel of the XRT75R12 incorporates an advanced crystal-less jitter attenuator that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

The XRT75R12 provides a parallel microprocessor interface for programming and control.

The XRT75R12 supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect a single bit error for diagnostic purposes.

Applications

- E3 and DS3 access equipment
- DSLAMs
- Digital cross connect systems
- CSU and DSU equipment
- Routers
- Fiber optic terminals

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Block Diagram

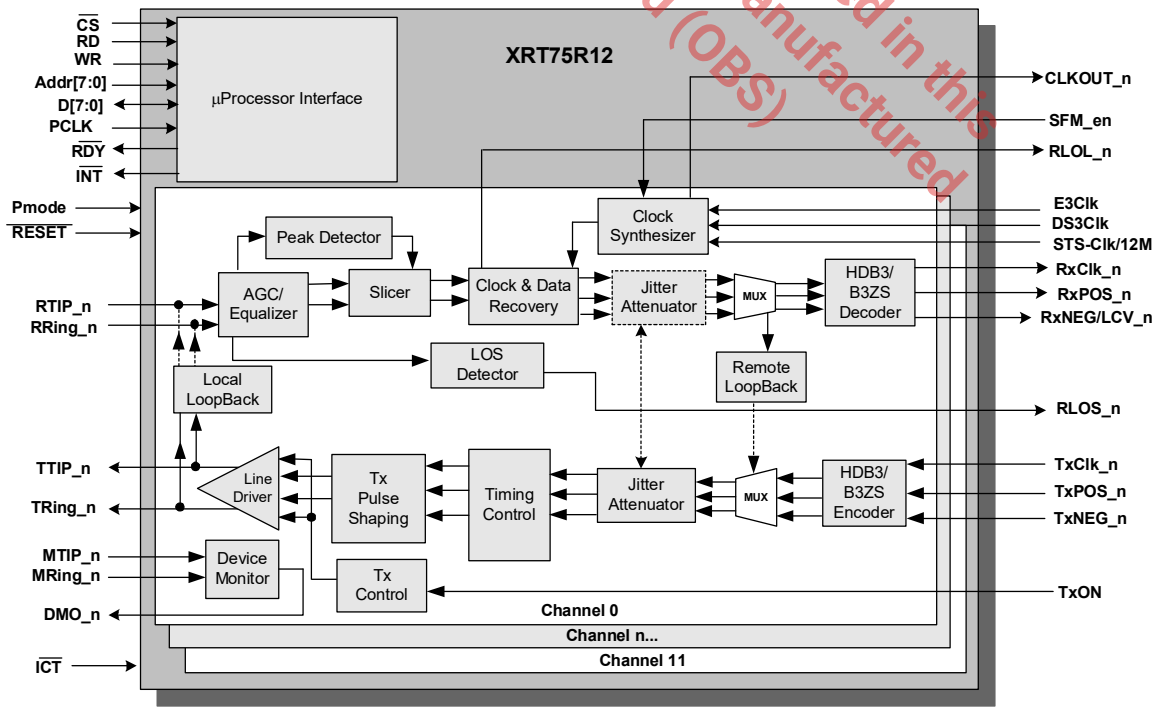

Figure 1: XRT75R12 Block Diagram

Revision History

Document No.	Release Date	Change Description
1.0.0	05/10/05	Final Release Version of XRT75R12 datasheet.
1.0.1	April 2006	1. Added current and power consumption on Table 50, “DC Electrical Characteristics:,” on page 84. 2. Revised Receive Monitor Enable Bit functional description and Section 3.3.1 description. 3. Updated Table 3, “The ALOS (Analog LOS) Declaration and Clearance Thresholds for a given setting of REQEN (DS3 and STS-1 Applications),” on page 23. 4. Minor corrections on Transmitter Section of Features Summary on page 2. 5. Minor typo corrections in STS1Clk/12M pin description and in Sections 1.0, 3.3, and 4.5, Table 17 and Table 19. 6. Added Table 2, “Reference Clock Performance Specifications,” on page 19.
1.0.2	12/07/06	1. Corrected package thermal resistance specification.
1.0.3	6/11/07	1. Corrected global register 0x08 and added global registers 0x80 & 0x88. 2. Added (N = [0:11] & M = 0-5 & 8-D) to channelized register titles.
1.0.4	10/26/07	1. Theta-jC thermal value added.
1.0.5	03/24/15	1. Add "-L" to part number. 2. Update Exar logo. 3. Add technical support email address. ECN 1513-06
1.0.6	3/13/20	1. Converted to MaxLinear format. 2. Updated Ordering Information and moved to end.

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Features

Receiver

- R^3 Technology (Reconfigurable, Relayless, Redundancy)
- On chip clock and data recovery circuit for high input jitter tolerance
- Meets E3, DS3, and STS-1 jitter tolerance requirement
- Detects and clears LOS as per G.775
- Receiver monitor mode handles up to 20dB flat loss with 6dB cable attenuation
- On chip B3ZS and HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288MHz clock
- Provides low jitter output clock

Transmitter

- R^3 Technology (Reconfigurable, Relayless Redundancy)
- Compliant with Bellcore GR-499, GR-253, and ANSI T1.102 Specifications for transmit pulse
- Tri-state transmit output capability for redundancy applications
- Each transmitter can be independently turned on or off
- Transmitters provide voltage output drive

Jitter Attenuator

- On chip advanced crystal-less jitter attenuator for each channel
- Jitter attenuator can be selected in receive, transmit path or disabled
- Meets ETSI TBR 24 jitter transfer requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- 16 or 32 bits selectable FIFO size

Control and Diagnostics

- Parallel microprocessor interface for control and configuration
- Supports optional internal transmit driver monitoring
- Each channel supports analog, remote and digital loopbacks
- Single 3.3V ± 5% power supply
- 5V-tolerant digital inputs
- Available in 420-pin TBGA thermally enhanced package
- - 40°C to 85°C industrial temperature range

Transmit Interface Characteristics

- Accepts either single-rail or dual-rail data from terminal equipment and generates a bipolar signal to the line
- Integrated pulse shaping circuit
- Built-in B3ZS and HDB3 encoder (which can be disabled)
- Accepts transmit clock with duty cycle of 30% - 70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

Receive Interface Characteristics

- Integrated adaptive receive equalization (optional) for optimal clock and data recovery
- Declares and clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets jitter tolerance requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets jitter tolerance requirements, as specified in Bellcore GR-499-CORE for DS3 applications
- Declares Loss of Lock (LOL) alarm
- Built-in B3ZS / HDB3 decoder (which can be disabled)
- Recovered data can be muted while the LOS condition is declared
- Outputs either single-rail or dual-rail data to the terminal equipment

The product (or product mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

1.0 Pin Information

1.1 Pin Descriptions (by Function)

Table 1: System-Side Transmit Input and Transmit Control Pins

Pin #	Signal Name	Type	Description
P4	TxON	I	**Transmit On / Off Input** Upon power up, the transmitters are powered on. Turning the transmitters on or off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 12 transmitters are powered off. **Note:** TxON is ideal for redundancy applications. See the R^3 Technology section of this datasheet for more details. Internally pulled "High".
F22 AA22 H22 Y23 G26 AA25 G1 AA2 H5 Y4 F5 AA5	TxCLK0 TxCLK1 TxCLK2 TxCLK3 TxCLK4 TxCLK5 TxCLK6 TxCLK7 TxCLK8 TxCLK9 TxCLK10 TxCLK11	I	**Transmit Clock Input** These input pins have three functions: ▪ They function as the timing source for the transmit section of the corresponding channel within the XRT75R12. ▪ They are used by the transmit section of the LIU IC to sample the corresponding TxPOS_n and TxNEG_n input pins. ▪ They are used to clock the PRBS generator. **Note:** The user is expected to supply a 44.736MHz ± 20ppm clock signal (for DS3 applications), 34.368MHz ± 20ppm clock signal (for E3 applications) or a 51.84MHz ± 4.6ppm clock signal (for STS-1, Stratum 3E, or better applications).
E23 AB24 J22 AA23 G25 AA26 G2 AA1 J5 AA4 E4 AB3	TxPOS0 TxPOS1 TxPOS2 TxPOS3 TxPOS4 TxPOS5 TxPOS6 TxPOS7 TxPOS8 TxPOS9 TxPOS10 TxPOS11	I	**Transmit Positive Data Input** The function of these digital input pins depends upon whether the corresponding channel has been configured to operate in the Single-Rail or Dual-Rail Mode. **Single Rail Mode - Transmit Data Input** Operating in the Single-Rail Mode, all transmit input data will be serially applied to this input pin. This signal will be latched into the transmit section circuitry on the active edge of the TxCLK_n signal. The transmit section of the LIU IC will then encode this data into either the B3ZS line code (for DS3 and STS-1 applications) or the HDB3 line code (for E3 applications). **Dual Rail Mode - Transmit Positive Data Input** In the Dual-Rail Mode, the user should apply a pulse to this input pin when a positive-polarity pulse is to be transmitted onto the line. This signal will be latched into the transmit section circuitry upon the active edge of the TxCLK_n signal. The transmit section of the LIU IC will NOT encode this data into either the B3ZS or HDB3 line codes. If the user configures the LIU IC to operate in the Dual-Rail Mode, B3ZS or HDB3 encoding must have already been done prior to this input.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OPS).

Table 1: (Continued) System-Side Transmit Input and Transmit Control Pins

Pin #	Signal Name	Type	Description
C25 AB25 H23 W23 H24 Y26 H3 Y1 H4 W4 C2 AB2	TxNEG0 TxNEG1 TxNEG2 TxNEG3 TxNEG4 TxNEG5 TxNEG6 TxNEG7 TxNEG8 TxNEG9 TxNEG10 TxNEG11	I	**Transmit Negative Data Input** When a channel has been configured to operate in the Dual-Rail Mode, the user should apply a pulse to this input pin anytime the transmit section of the LIU IC to generate a negative-polarity pulse onto the line. This signal will be latched into the transmit section circuitry upon the active edge of the TxCLK_n signal. **Note:** In the Single-Rail Mode, this input pin has no function and should be tied to GND.
B24 AE24 C20 AD20 C16 AD16 C11 AD11 C7 AD7 C3 AD3	TTip0 TTip1 TTip2 TTip3 TTip4 TTip5 TTip6 TTip7 TTip8 TTip9 TTip10 TTip11	O	**Transmit TTIP Output - Positive Polarity Signal** These output pins, along with the corresponding TRING_n output pins, function as the transmit DS3, E3, or STS-1 line output signal drivers for a given channel of the XRT75R12. Connect this signal and the corresponding TRING_n output signal to a 1:1 transformer. Whenever the transmit section of the channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a higher voltage than its corresponding TRING_n output pins. Conversely, whenever the transmit section of the channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a lower voltage than its corresponding TRING_n output pin. **Note:** This output pin will be tri-stated whenever the TxON input pin or bit-field is set to "0".
C24 AD24 B20 AE20 B16 AE16 B11 AE11 B7 AE7 B3 AE3	TRing0 TRing1 TRing2 TRing3 TRing4 TRing5 TRing6 TRing7 TRing8 TRing9 TRing10 TRing11	O	**Transmit Ring Output - Negative Polarity Signal** These output pins, along with the corresponding TTIP_n output pins, function as the transmit DS3, E3, or STS-1 line output signal drivers for a given channel within the XRT75R12. Connect this signal and the corresponding TTIP_n output signal to a 1:1 transformer. Whenever the transmit section of the channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a lower voltage than its corresponding TTIP_n output pin. Conversely, whenever the transmit section of the channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a higher voltage than its corresponding TTIP_n output pin. **Note:** This output pin will be tri-stated whenever the TxON input pin or bit-field is set to "0".

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 1: (Continued) System-Side Transmit Input and Transmit Control Pins

Pin #	Signal Name	Type	Description
C23 AD23 D19 AC19 D15 AC15 E11 AB11 E8 AB8 C4 AD4	MTip0 MTip1 MTip2 MTip3 MTip4 MTip5 MTip6 MTip7 MTip8 MTip9 MTip10 MTip11	I	**Monitor Tip Input - Positive Polarity Signal** These input pins, along with MRing_n, function as the transmit Drive Monitor Output (DMO) input monitoring pins: ▪ To monitor the transmit output line signal. ▪ To perform this monitoring externally. This pin MUST be connected to the corresponding TTIP_n output pin via a 270Ω series resistor. Similarly, the MRING_n input pin MUST also be connected to its corresponding TRING_n output pin via a 270Ω series resistor. The MTIP_n and MRING_n input pins will continuously monitor the transmit output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" in order to denote a possible fault condition in the transmit output line signal path. **Note:** These input pins are inactive if the user chooses to internally monitor the transmit output line signal.
D23 AC23 E19 AB19 E16 AB16 D10 AC10 D8 AC8 D4 AC4	MRing0 MRing1 MRing2 MRing3 MRing4 MRing5 MRing6 MRing7 MRing8 MRing9 MRing10 MRing11	I	**Monitor Ring Input** These input pins, along with MTIP_n, function as the transmit Drive Monitor Output (DMO) input monitoring pins: ▪ To monitor the transmit output line signal. ▪ To perform this monitoring externally. This input pin MUST be connected to the corresponding TRING_n output pin via a 270Ω series resistor. Similarly, the MTIP_n input pin MUST be connected to its corresponding TTIP_n output pin via a 270Ω series resistor. The MTIP_n and MRING_n input pins will continuously monitor the transmit output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" to indicate a possible fault condition in the transmit output line signal path. **Note:** These input pins are inactive if the user chooses to internally monitor the transmit output line signal.
N3 N4 N5 N1 M1 L2 M2 M3 M4 M5 K2 J1	DMO0 DMO1 DMO2 DMO3 DMO4 DMO5 DMO6 DMO7 DMO8 DMO9 DMO10 DMO11	O	**Drive Monitor Output** These output signals are used to indicate a fault condition within the transmit output signal path. This output pin will toggle "High" anytime the transmit Drive Monitor circuitry, either via the corresponding MTIP and MRING input pins or internally, detects no bipolar pulses via the transmit output line signal (for example, via the TTIP_m and TRING_m output pins) for 128 bit periods. This output pin will be driven "Low" anytime the transmit Drive Monitor circuitry has detected at least one bipolar pulse via the transmit output line signal within the last 128 bit periods.

The product (s) mentioned in this data sheet are obsolete and may not be ordered (OBS)

Table 2: System-Side Receive Output and Receive Control Pins

Pin #	Signal Name	Type	Description
D25 AD25 G23 AA24 J24 U24 J3 U3 G4 AA3 D2 AD2	RLOS0 RLOS1 RLOS2 RLOS3 RLOS4 RLOS5 RLOS6 RLOS7 RLOS8 RLOS9 RLOS10 RLOS11	O	**Receive Loss of Signal Output Indicator** This output pin indicates a Loss of Signal (LOS) defect condition for the corresponding channel. "Low" - Indicates that the corresponding channel is NOT currently declaring the LOS defect condition. "High" - Indicates that the corresponding channel is currently declaring the LOS defect condition.
G22 AB26 K22 U22 L24 W25 L3 W2 K5 U5 G5 AB1	RLOL0 RLOL1 RLOL2 RLOL3 RLOL4 RLOL5 RLOL6 RLOL7 RLOL8 RLOL9 RLOL10 RLOL11	O	**Receive Loss of Lock Output Indicator** This output pin indicates a Loss of Lock (LOL) condition for the corresponding channel. "Low" - Indicates that the corresponding channel is NOT declaring the LOL condition. "High" - Indicates that the corresponding channel is currently declaring the LOL condition. **Note:** The receive section of a given channel will declare the LOL condition anytime the frequency of the Recovered Clock (RCLK) signal differs from that of the reference clock programmed for that channel by 0.5% or more.
E25 AD26 G24 Y24 L22 T22 L5 T5 G3 Y3 E2 AD1	RxPOS0 RxPOS1 RxPOS2 RxPOS3 RxPOS4 RxPOS5 RxPOS6 RxPOS7 RxPOS8 RxPOS9 RxPOS10 RxPOS11	O	**Receive Positive Data Output** The function of these output pins depends upon whether the channel has been configured to operate in the Single-Rail or Dual-Rail Mode. **Dual-Rail Mode - Receive Positive Polarity Data Output** If the channel has been configured to operate in the Dual-Rail Mode, then all positive-polarity data will be output via this pin. The negative-polarity data will be output via the corresponding RxNEG_n pin. In other words, the receive section of the corresponding channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a positive-polarity pulse via the RTIP or RRING input pins. The data output via this pin is updated upon the active edge of the RxCLK_n output clock signal. **Single-Rail Mode - Receive Data Output** In the Single-Rail Mode, all receive (or recovered) data will be output via this pin. The data output via this pin is updated upon the active edge of the RxCLK_n output clock signal.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 2: (Continued) System-Side Receive Output and Receive Control Pins

Pin #	Signal Name	Type	Description
F23 AC26 F24 U23 L23 T24 L4 T3 F3 U4 F4 AC1	RxNEG/LCV0 RxNEG/LCV1 RxNEG/LCV2 RxNEG/LCV3 RxNEG/LCV4 RxNEG/LCV5 RxNEG/LCV6 RxNEG/LCV7 RxNEG/LCV8 RxNEG/LCV9 RxNEG/LCV10 RxNEG/LCV11	O	**Receive Negative Data Output and Line Code Violation** The function of these pins depends on whether the XRT75R12 is configured in Single Rail or Dual Rail Mode. **Dual-Rail Mode - Receive Negative Polarity Data Output** In the Dual-Rail Mode, all negative-polarity data will be output via this pin. The positive-polarity data will be output via the corresponding RxPOS_n output pin. In other words, the receive section of the corresponding channel will pulse this output pin "High" for one period of RxCLK_n anytime it receives a negative-polarity pulse via the RTIP or RRING input pins. The data output via this pin is updated upon the active edge of the RCLK_n output clock signal. **Single-Rail Mode - Line Code Violation Indicator Output** In the Single-Rail Mode, this output pin will function as the Line Code Violation indicator output. In this configuration, the receive section of the channel will pulse this output pin "High" for at least one RCLK period whenever it detects either an LCV (Line Code Violation) or an EXZ (Excessive Zero Event). The data that is output via this pin is updated upon the active edge of the RCLK_n output clock signal.
E24 AC25 J23 V23 K24 T23 K3 T4 J4 V4 E3 AC2	RxCLK0 RxCLK1 RxCLK2 RxCLK3 RxCLK4 RxCLK5 RxCLK6 RxCLK7 RxCLK8 RxCLK9 RxCLK10 RxCLK11	O	**Receive Clock Output** This output pin functions as the receive or recovered clock signal. All receive (or recovered) data will output via the RxPOS_n and RxNEG_n outputs upon the active edge of this clock signal. Additionally, if the device or channel has been configured to operate in the Single-Rail Mode, then the RNEG_n/LCV_n output pins will also be updated upon the active edge of this clock signal.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 3: Receive Line Side Pins

Pin #	Signal Name	Type	Description
B22 AE22 B18 AE18 A14 AF14 D13 AC13 B9 AE9 B5 AE5	RTip0 RTip1 RTip2 RTip3 RTip4 RTip5 RTip6 RTip7 RTip8 RTip9 RTip10 RTip11	I	**Receive TIP Input** These input pins, along with the corresponding RRing_n input pin, function as the receive DS3, E3, or STS-1 line input signal for a given channel of the XRT75R12. Connect this signal and the corresponding RRING_n input signal to a 1:1 transformer. Whenever the RTIP or RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a higher voltage than its corresponding RRING_n input pin. Conversely, whenever the RTIP or RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a lower voltage than its corresponding RRING_n input pin.
C22 AD22 C18 AD18 B14 AE14 C13 AD13 C9 AD9 C5 AD5	RRing0 RRing1 RRing2 RRing3 RRing4 RRing5 RRing6 RRing7 RRing8 RRing9 RRing10 RRing11	I	**Receive Ring Input** These input pins, along with the corresponding RTIP_n input pin, function as the receive DS3, E3, or STS-1 line input signal for a given channel of the XRT75R12. Connect this signal and the corresponding RTIP_n input signal to a 1:1 transformer. (See Figure 6). Whenever the RTIP or RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a lower voltage than its corresponding RTIP_n input pin. Conversely, whenever the RTIP or RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a higher voltage than its corresponding RTIP_n input pin.

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Table 4: Clock Interface

Pin #	Signal Name	Type	Description
R5	SFM_EN	I	**Single Frequency Mode Enable** This input pin is used to configure the XRT75R12 to operate in the SFM (Single Frequency Mode). When this feature is invoked, the SFM synthesizer will become active. By applying a 12.288MHz clock signal to the STS-1Clk /12M pin, the XRT75R12 will generate all of the appropriate clock signals (for example, 34.368MHz, 44.736MHz or 51.84MHz). The XRT75R12 internal circuitry will route each of these synthesized clock signals to the appropriate nodes of the corresponding channels in the XRT75R12. "Low" - Disables the Single Frequency Mode. In this setting, the user is required to supply to the E3CLK, DS3CLK or STS-1CLK input pins all of the relevant clock signals that are to be used within the chip. "High" - Enables the Single-Frequency Mode. **Note:** This input pin is internally pulled low.
R1	E3Clk	I	**E3 Clock Input (34.368MHz ± 20ppm)** If any one of the channels is configured in E3 mode, a reference clock of 34.368MHz ± 20ppm is applied to this input pin. If the LIU is used in E3 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. **Note:** SFM mode negates the need for this clock.
T1	DS3Clk	I	**DS3 Clock Input (44.736MHz ± 20ppm)** If any one of the channels is configured in DS3 mode, a reference clock of 44.736MHz ± 20ppm is applied to this input pin. **Note:** SFM mode negates the need for this clock.
U1	STS-1Clk / 12M	I	**STS-1 Clock Input (51.84MHz ± 20ppm)** If any one of the channels is configured in STS-1 mode, a reference clock of 51.84MHz ± 20ppm is applied to this input pin. If the LIU is used in STS-1 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. **Single Frequency Mode Clock Input (12.288MHz ± 20ppm)** In Single Frequency Mode, a reference clock of 12.288MHz ± 20ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the rates (E3, DS3 or STS-1).
C26 W22 K23 W24 J25 V25 J2 V2 K4 W3 C1 W5	CLKOUT0 CLKOUT1 CLKOUT2 CLKOUT3 CLKOUT4 CLKOUT5 CLKOUT6 CLKOUT7 CLKOUT8 CLKOUT9 CLKOUT10 CLKOUT11	O	**Reference Clock Out** A reference clock pin is provided for each channel that will supply a precise data rate frequency derived from either the clock input pin (E3Clk, DS3Clk, or STS-1Clk) or the 12.288MHz input in SFM mode. This frequency will be as stable as the original source. It is designed to provide the attached framer with its appropriate reference clock.

The Product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 5: General Control Pins

Pin #	Signal Name	Type	Description
P3	TEST	****	**Factory Test Mode Input Pin** This pin must be connected to GND for normal operation. **Note:** This input pin is internally pulled "Low".
AE25	TRST	I	**Test Reset** Test boundary scan.
AB23	TMS	I	**Test Mode Select** Test boundary scan.
AB5	TCK	I	**Test Clock** Test boundary scan.
AB4	TDI	I	**Test Data Input** Test boundary scan.
AE2	TDO	O	**Test Data Output** Test boundary scan.

Table 6: Microprocessor Parallel Interface

Pin #	Signal Name	Type	Description
J26	Pmode	I	**Microprocessor Parallel Interface Mode** "High" sets a synchronous clocked interface mode with a clock from the host. "Low" sets an asynchronous mode where a clock internal to the XRT75R12 will time the operations.
P24	PCLK	I	High speed clock supplied by the host to provide timing in the Synchronous Interface Mode. This signal must be a square-wave.
N24	$\overline{CS}$	I	**Chip Select Input (active low)** Initiates a read or write operation. When "High", no parallel communication is active between the LIU and the host.
N22	$\overline{WR}$	I	**Write Input (active low)** Enables the host to write data D[7:0] into the LIU register space at address Addr[7:0].
N23	$\overline{RD}$	I	**Read Input (active low)** Commands the LIU to transfer the contents of a register specified by Addr[7:0] to the host.
N25	$\overline{RDY}$	O	**Ready Line Output (active low)** Provides a handshake between the LIU and the host that communicates when an operation has been completed. **Note:** This pin must be pulled "High" with a 3kΩ ±1% resistor.
K25 M22 M23 M24 K26 L26 M26 N26	Addr0 Addr1 Addr2 Addr3 Addr4 Addr5 Addr6 Addr7	I	An eight bit direct address bus that specifies the source or destination register for a read or write operation.

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Table 6: Microprocessor Parallel Interface (Continued)

Pin #	Signal Name	Type	Description
P22 R26 T26 U26 R25 R24 R23 R22	D0 D1 D2 D3 D4 D5 D6 D7	I/O	An eight bit bi-directional data bus that provides the data into the LIU for a write operation or the data out to the host for a read operation.
P26	$\overline{INT}$	O	**Interrupt Active Output (active low)** Normally, this output pin will be pulled "High". However, if the user enables interrupts within the LIU, and if those conditions occur, the XRT75R12 will signal an interrupt from the microprocessor by pulling this output pin "Low". The host microprocessor must ascertain the source of the interrupt and service it. Reading the source of the interrupt will clear the flag and the $\overline{INT}$ pin will go back high unless another interrupt has gone active. **Notes:** **1.** This pin will remain "Low" until the interrupt has been serviced. **2.** This pin must be pulled "High" with a 3kΩ ± 1% resistor.
N2	$\overline{RESET}$	I	**Reset Input** Pulsing this input "Low" causes the XRT75R12 to reset the contents of the on-chip command registers to their default values. As a consequence, the XRT75R12 will then also be operating in its default condition. For normal operation, this input pin should be at a logic "High". **Note:** This input pin is internally pulled high.

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Table 7: Power Supply Pins

Pin Name	Pin Numbers	Description
RVDD0 RVDD1 RVDD2 RVDD3 RVDD4 RVDD5 RVDD6 RVDD7 RVDD8 RVDD9 RVDD10 RVDD11	D22 AC22 D18 AC18 E15 AB15 E12 AB12 A9 AF9 D5 AC5	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
TVDD0 TVDD1 TVDD2 TVDD3 TVDD4 TVDD5 TVDD6 TVDD7 TVDD8 TVDD9 TVDD10 TVDD11	B23 AE23 B19 AE19 B15 AE15 B10 AE10 A6 AF6 B4 AE4	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
AVDD	M25, T25, AB21, AB18, AF13, AF12, AB9, AB6, R4, K1, E6, E9, A12, A13, E18, E21	**Analog Power Supply (3.3V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
DVDD	D26, F25, H25, P25, W26, V24, Y22, AF21, AF20, AF17, AF16, AD14, AD12, AF11, AF8, AF7, AF24, AD6, AF3, Y5, V3, W1, P5, P2, H2, F2, D1, C6, A7, A3, A8, A11, C12, C14, A16, A17, A20, A21, A24	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

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Table 8: Ground Pins

Pin Name	Pin Numbers	Description
RGND0 RGND1 RGND2 RGND3 RGND4 RGND5 RGND6 RGND7 RGND8 RGND9 RGND10 RGND11	A22 AF22 A18 AF18 E14 AB14 E13 AB13 D9 AC9 A5 AF5	**Receive Analog Ground** It is recommended that all ground pins of this device be tied together.
TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9 TGND10 TGND11	A23 AF23 A19 AF19 A15 AF15 A10 AF10 B6 AE6 A4 AF4	**Transmit Analog Ground** It is recommended that all ground pins of this device be tied together.
AGND	A1, A2, A25, A26, B1, B2, B25, B26, C8, C10, C17, C19, C21, D17, D21, E5, E22, L25, U25, AB22, AB20, AB17, AB10, AB7, R3, L1, E7, E10, B12, B13, E17, E20, T2, U2, AC17, AC21, AD8, AD10, AD15, AD17, AD19, AD21, AE1, AE26, AE12, AE13, AF1, AF2, AF25, AF26, C15	**Analog Ground** It is recommended that all ground pins of this device be tied together.
DGND	E26, F26, H26, P23, , V26, Y25, V22, AC24, AC20, AC16, AC14, AC12, AC11, AE8, AE17, AE21, AC7, AC6, AC3, V5, Y2, V1, R2, P1, H1, F1, E1, D3, D7, B8, D6, D11, D12, D14, D16, B17, D20, B21, D24	**Digital Ground** It is recommended that all ground pins of this device be tied together.

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Table 9: Pin List by Pin Number

Pin	Pin Name
A1	AGND
A2	AGND
A3	DVDD
A4	TGND10
A5	RGND10
A6	TVDD8
A7	DVDD
A8	DVDD
A9	RVDD8
A10	TGND6
A11	DVDD
A12	AVDD
A13	AVDD
A14	RTip4
A15	TGND4
A16	DVDD
A17	DVDD
A18	RGND2
A19	TGND2
A20	DVDD
A21	DVDD
A22	RGND0
A23	TGND0
A24	DVDD
A25	AGND
A26	AGND
B1	AGND
B2	AGND
B3	TRing10
B4	TVDD10
B5	RTip10
B6	TGND8
B7	TRing8
B8	DGND
B9	RTip8
B10	TVDD6
B11	TRing6
B12	AGND
B13	AGND
B14	RRing4
B15	TVDD4
B16	TRing4
B17	DGND
B18	RTip2
B19	TVDD2
B20	TRing2
B21	DGND
B22	RTip0
B23	TVDD0
B24	TTip0
B25	AGND
B26	AGND
C1	CLKOUT10
C2	TxNEG10
C3	TTip10
C4	MTip10
C5	RRing10
C6	DVDD
C7	TTip8
C8	AGND
C9	RRing8
C10	AGND
C11	TTip6
C12	DVDD
C13	RRing6
C14	DVDD
C15	AGND
C16	TTip4
C17	AGND
C18	RRing2
C19	AGND
C20	TTip2
C21	AGND
C22	RRing0
C23	MTip0
C24	TRing0
C25	TxNEG0
C26	CLKOUT0
D1	DVDD
D2	RLOS10
D3	DGND
D4	MRing10
D5	RVDD10
D6	DGND
D7	DGND
D8	MRing8
D9	RGND8
D10	MRing6
D11	DGND
D12	DGND
D13	RTip6
D14	DGND
D15	MTip4
D16	DGND
D17	AGND
D18	RVDD2
D19	MTip2
D20	DGND
D21	AGND
D22	RVDD0
D23	MRing0
D24	DGND
D25	RLOS0
D26	DVDD
E1	DGND
E2	RxPOS10
E3	RxCLK10
E4	TxPOS10
E5	AGND
E6	AVDD
E7	AGND
E8	MTip8
E9	AVDD
E10	AGND
E11	MTip6
E12	RVDD6
E13	RGND6
E14	RGND4
E15	RVDD4
E16	MRing4
E17	AGND
E18	AVDD
E19	MRing2
E20	AGND
E21	AVDD
E22	AGND
E23	TxPOS0
E24	RxCLK0
E25	RxPOS0
E26	DGND
F1	DGND
F2	DVDD
F3	RxNEG / LCV8
F4	RxNEG / LCV10
F5	TxCLK10
F22	TxCLK0
F23	RxNEG / LCV0
F24	RxNEG / LCV2
F25	DVDD
F26	DGND
G1	TxCLK6
G2	TxPOS6
G3	RxPOS8
G4	RLOS8
G5	RLOL10
G22	RLOL0
G23	RLOS2
G24	RxPOS2
G25	TxPOS4
G26	TxCLK4
H1	DGND
H2	DVDD
H3	TxNEG6
H4	TxNEG8
H5	TxCLK8
H22	TxCLK2
H23	TxNEG2
H24	TxNEG4
H25	DVDD
H26	DGND

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Pin	Pin Name
J1	DMO11
J2	CLKOUT6
J3	RLOS6
J4	RxCLK8
J5	TxPOS8
J22	TxPOS2
J23	RxCLK2
J24	RLOS4
J25	CLKOUT4
J26	Pmode
K1	AVDD
K2	DMO10
K3	RxCLK6
K4	CLKOUT8
K5	RLOL8
K22	RLOL2
K23	CLKOUT2
K24	RxCLK4
K25	Addr0
K26	Addr4
L1	AGND
L2	DMO5
L3	RLOL6
L4	RxNEG / LCV6
L5	RxPOS6
L22	RxPOS4
L23	RxNEG / LCV4
L24	RLOL4
L25	AGND
L26	Addr5
M1	DMO4
M2	DMO6
M3	DMO7
M4	DMO8
M5	DMO9
M22	Addr1
M23	Addr2
M24	Addr3
M25	AVDD
M26	Addr6
N1	DMO3

Pin	Pin Name
N2	RESET
N3	DMO0
N4	DMO1
N5	DMO2
N22	WR
N23	RD
N24	CS
N25	RDY
N26	Addr7
P1	DGND
P2	DVDD
P3	TEST
P4	TxON
P5	DVDD
P22	D0
P23	DGND
P24	PCLK
P25	DVDD
P26	INT
R1	E3Clk
R2	DGND
R3	AGND
R4	AVDD
R5	SFM_EN
R22	D7
R23	D6
R24	D5
R25	D4
R26	D1
T1	DS3Clk
T2	AGND
T3	RxNEG / LCV7
T4	RxCLK7
T5	RxPOS7
T22	RxPOS5
T23	RxCLK5
T24	RxNEG / LCV5
T25	AVDD
T26	D2
U1	STS-1Clk / 12M
U2	AGND

Pin	Pin Name
U3	RLOS7
U4	RxNEG / LCV9
U5	RLOL9
U22	RLOL3
U23	RxNEG / LCV3
U24	RLOS5
U25	AGND
U26	D3
V1	DGND
V2	CLKOUT7
V3	DVDD
V4	RxCLK9
V5	DGND
V22	DGND
V23	RxCLK3
V24	DVDD
V25	CLKOUT5
V26	DGND
W1	DVDD
W2	RLOL7
W3	CLKOUT9
W4	TxNEG9
W5	CLKOUT11
W22	CLKOUT1
W23	TxNEG3
W24	CLKOUT3
W25	RLOL5
W26	DVDD
Y1	TxNEG7
Y2	DGND
Y3	RxPOS9
Y4	TxCLK9
Y5	DVDD
Y22	DVDD
Y23	TxCLK3
Y24	RxPOS3
Y25	DGND
Y26	TxNEG5
AA1	TxPOS7
AA2	TxCLK7
AA3	RLOS9

Pin	Pin Name
AA4	TxPOS9
AA5	TxCLK11
AA22	TxCLK1
AA23	TxPOS3
AA24	RLOS3
AA25	TxCLK5
AA26	TxPOS5
AB1	RLOL11
AB2	TxNEG11
AB3	TxPOS11
AB4	TDI
AB5	TCK
AB6	AVDD
AB7	AGND
AB8	MTip9
AB9	AVDD
AB10	AGND
AB11	MTip7
AB12	RVDD7
AB13	RGND7
AB14	RGND5
AB15	RVDD5
AB16	MRing5
AB17	AGND
AB18	AVDD
AB19	MRing3
AB20	AGND
AB21	AVDD
AB22	AGND
AB23	TMS
AB24	TxPOS1
AB25	TxNEG1
AB26	RLOL1
AC1	RxNEG / LCV11
AC2	RxCLK11
AC3	DGND
AC4	MRing11
AC5	RVDD11
AC6	DGND
AC7	DGND
AC8	MRing9

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Pin	Pin Name
AC9	RGND9
AC10	MRing7
AC11	DGND
AC12	DGND
AC13	RTip7
AC14	DGND
AC15	MTip5
AC16	DGND
AC17	AGND
AC18	RVDD3
AC19	MTip3
AC20	DGND
AC21	AGND
AC22	RVDD1
AC23	MRing1
AC24	DGND
AC25	RxCLK1
AC26	RxNEG / LCV1
AD1	RxPOS11
AD2	RLOS11
AD3	TTip11
AD4	MTip11
AD5	RRing11
AD6	DVDD
AD7	TTip9
AD8	AGND
AD9	RRing9
AD10	AGND
AD11	TTip7
AD12	DVDD
AD13	RRing7
AD14	DVDD
AD15	AGND
AD16	TTip5
AD17	AGND
AD18	RRing3
AD19	AGND
AD20	TTip3
AD21	AGND
AD22	RRing1
AD23	MTip1

Pin	Pin Name
AD24	TRing1
AD25	RLOS1
AD26	RxPOS1
AE1	AGND
AE2	TDO
AE3	TRing11
AE4	TVDD11
AE5	RTip11
AE6	TGND9
AE7	TRing9
AE8	DGND
AE9	RTip9
AE10	TVDD7
AE11	TRing7
AE12	AGND
AE13	AGND
AE14	RRing5
AE15	TVDD5
AE16	TRing5
AE17	DGND
AE18	RTip3
AE19	TVDD3
AE20	TRing3
AE21	DGND
AE22	RTip1
AE23	TVDD1
AE24	TTip1
AE25	TRST
AE26	AGND
AF1	AGND
AF2	AGND
AF3	DVDD
AF4	TGND11
AF5	RGND11
AF6	TVDD9
AF7	DVDD
AF8	DVDD
AF9	RVDD9
AF10	TGND7
AF11	DVDD
AF12	AVDD

Pin	Pin Name
AF13	AVDD
AF14	RTip5
AF15	TGND5
AF16	DVDD
AF17	DVDD
AF18	RGND3
AF19	TGND3
AF20	DVDD
AF21	DVDD
AF22	RGND1
AF23	TGND1
AF24	DVDD
AF25	AGND
AF26	AGND

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2.0 Functional Description

The XRT75R12 is a twelve channel fully integrated Line Interface Unit featuring MaxLinear's R^3 Technology (Reconfigurable, Relayless Redundancy) for E3, DS3, and STS-1 applications. The LIU incorporates 12 independent receivers, transmitters and jitter attenuators in a single 420-lead TBGA package. Each channel can be independently programmed to support E3, DS-3 or STS-1 line rates using one input clock reference of 12.288MHz in Single Frequency Mode (SFM). The LIU is responsible for providing the physical connection between a line interface and an aggregate mapper or framing device. Along with the analog-to-digital processing, the LIU offers monitoring and diagnostic features to help optimize network design implementation. A key characteristic within the network topology is Automatic Protection Switching (APS). MaxLinear's proven expertise in providing redundancy solutions has paved the way for R^3 Technology.

3.0 R^3 Technology (Reconfigurable, Relayless, Redundancy)

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. MaxLinear's R^3 technology has re-defined E3, DS-3, and STS-1 LIU design for 1:1 and 1+1 redundancy applications. Without relays and with one bill of materials, MaxLinear offers multi-port, integrated LIU solutions to assist in high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R^3 Technology with MaxLinear's world leading line interface units.

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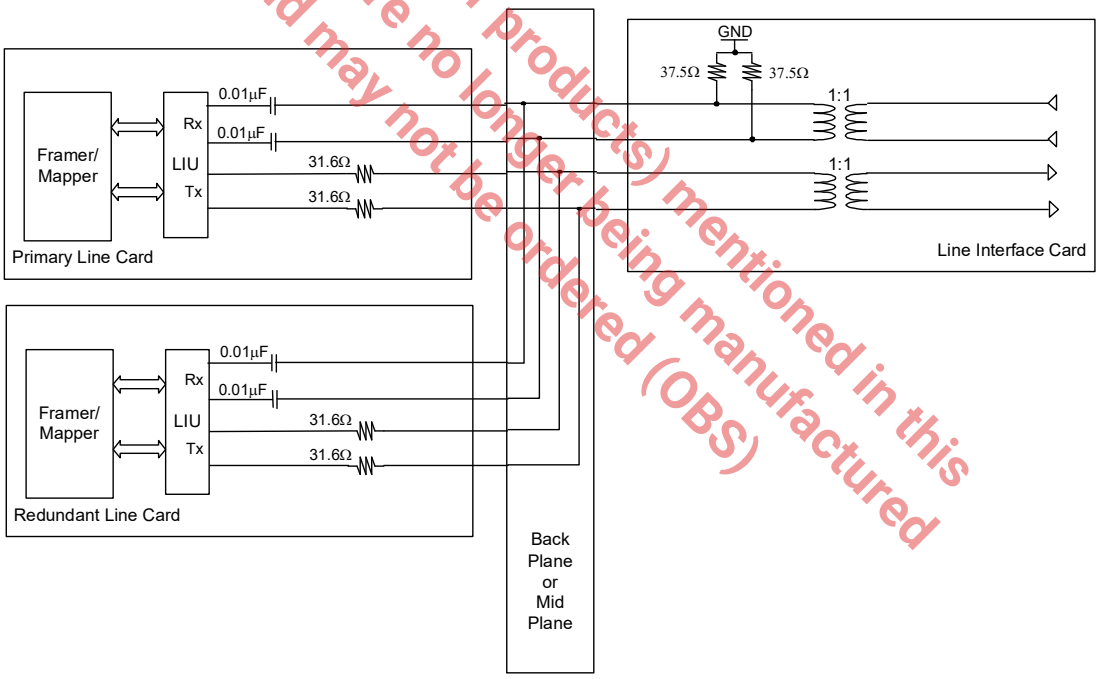


Figure 2: Network Redundancy Architecture

3.1 Network Architecture

A common network design that supports 1:1 or 1+1 redundancy consists of N primary cards along with N backup cards that connect into a mid-plane or back-plane architecture without transformers installed on the network cards. In addition to the network cards, the design has a line interface card with one source of transformers, connectors, and protection components that are common to both network cards. With this design, the bill of materials is reduced to the fewest amount of components. See Figure 2. for a simplified block diagram of a typical redundancy design.

4.0 Clock Synthesizer

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 3. Reference clock performance specifications can be found on Table 10 below.

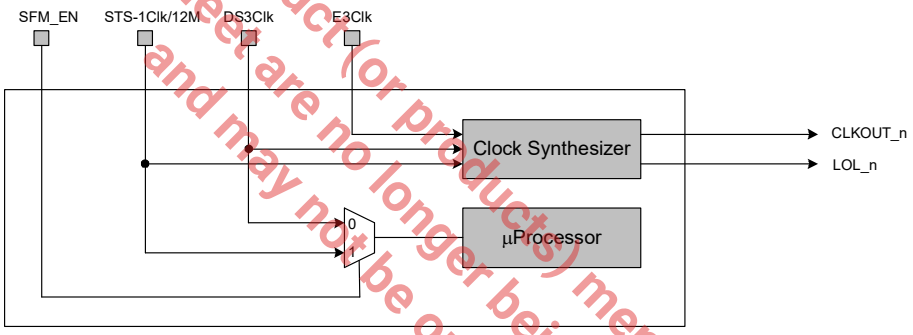


Figure 3: Simplified Block Diagram of the Input Clock Circuitry Driving the Microprocessor

The product(or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 10: Reference Clock Performance Specifications

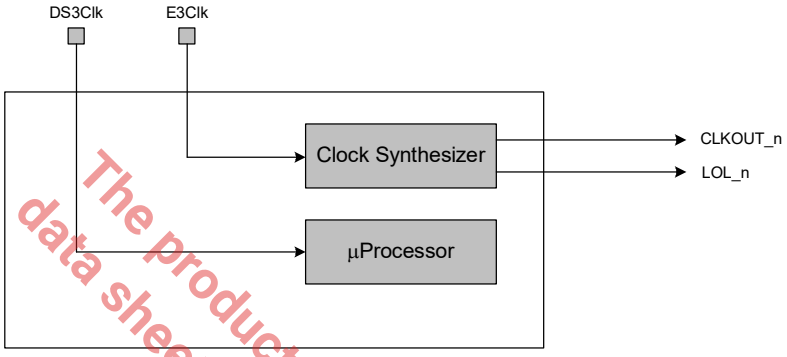
Symbol	Parameter	Min	Typ	Max	Units
REF_{DUTY}	Reference clock duty cycle	40		60	%
REF_{E3}	E3 reference clock frequency tolerance(1)	-20		+20	ppm
REF_{DS3}	DS3 reference clock frequency tolerance(1)	-20		+20	ppm
REF_{STS1}	STS-1 reference clock frequency tolerance(1)	-20		+20	ppm
REF_{SFM}	SFM reference clock frequency tolerance(1)	-20		+20	ppm
t_{RISE_REFCLK}	Reference clock rise time (10% to 90%)			5	ns
t_{FALL_REFCLK}	Reference clock fall time (90% to 10%)			5	ns
CLK_{JIT}	Reference clock jitter stability(2)			0.005	UI_{P2P}

1. Required to meet Bellcore GR-499 specification on frequency stability requirements. However, the LIU can functionally operate with ±100 ppm without meeting the required specifications.

2. Reference clock jitter limits are required for the transmit output to meet ITU-T and Bellcore system level jitter requirements.

4.1 Clock Distribution

Network cards that are designed to support multiple line rates which are not configured for Single Frequency Mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. However if multiple line rates will not be supported, for example E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.



1. For one input clock reference, the single frequency mode should be used.

Figure 4: Clock Distribution Configured in E3 Mode without Using SFM

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5.0 Receiver

The receiver is designed so that the LIU can recover clock and data from an attenuated line signal caused by cable loss or flat loss according to industry specifications. Once data is recovered, it is processed and presented at the receiver outputs according to the format chosen to interface with a Framer and Mapper or ASIC. This section describes the detailed operation of various blocks within the receive path. A simplified block diagram of the receive path is shown in Figure 5.

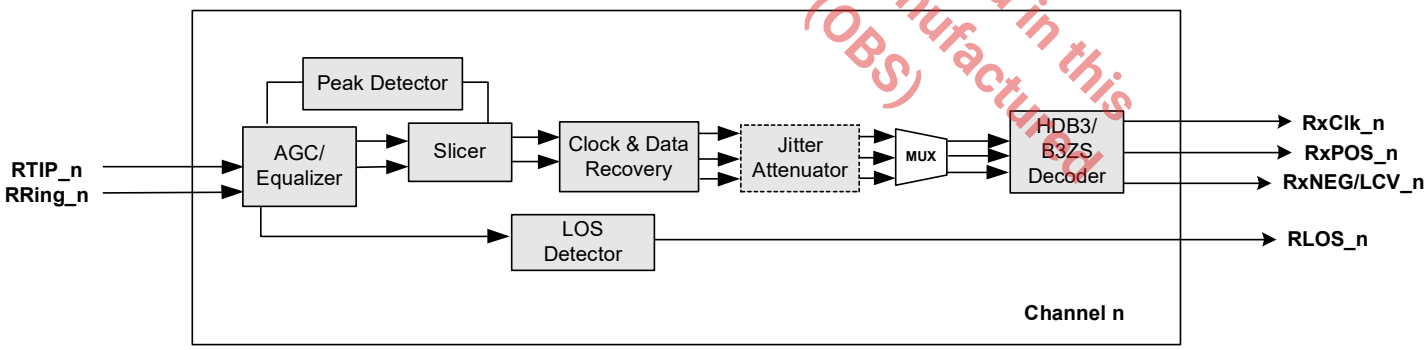

Figure 5: Receive Path Block Diagram

5.1 Receive Line Interface

Physical Layer devices are AC coupled to a line interface through a 1:1 transformer. The transformer provides isolation and a level shift by blocking the DC offset of the incoming data stream. The typical medium for the line interface is a 75Ω coaxial cable. Whether using E3, DS3 or STS-1, the LIU requires the same bill of materials, see Figure 6.

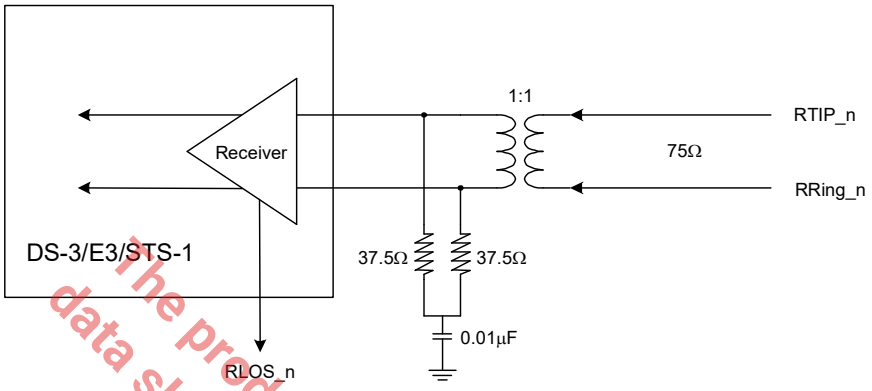

Figure 6: Receive Line Interface Connection

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5.2 Adaptive Gain Control (AGC)

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30dB. The peak detector provides feedback to the equalizer before slicing occurs.

5.3 Receive Equalizer

The equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The equalizer also boosts the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate positive and negative data. The equalizer can be disabled by programming the appropriate register.

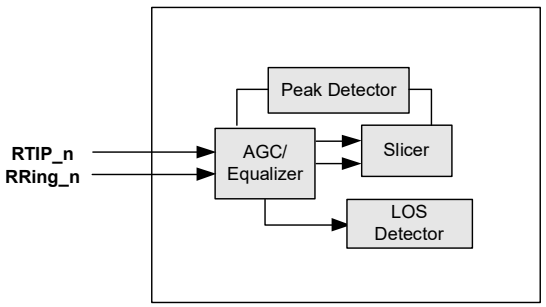

Figure 7: AGC and Equalizer Block Diagram

5.3.1 Recommendations for Equalizer Settings

The equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3 and STS-1 pulses (pulses that meet the template requirements) that have been driven through 0 to 900 feet of cable, the equalizer can be enabled. However, for square-shaped pulses such as E3 or for DS3 and STS-1 high pulses (that do not meet the pulse template requirements), it is recommended that the equalizer be disabled for cable length less than 300 feet. This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics. The equalizer also contains an additional 20dB gain stage to provide the line monitoring capability (Receive Monitor Mode) of the resistively attenuated signals which may have 20dB of flat loss. The equalizer and the equalizer gain mode can be enabled by programming the appropriate register. However, enabling the Equalizer Gain Mode (Receive Monitor Mode) suppresses the internal LOS circuitry and LOS will never assert nor LOS be declared when operating with Receive Monitor Mode enabled.

Note: The results of extensive testing indicate that even when the Equalizer was enabled, regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12dB cable loss at industrial temperature.

5.4 Clock and Data Recovery

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream, and provides the retimed data to the B3ZS (HDB3) decoder. The Clock Recovery PLL can be in one of the following two modes:

5.4.1 Data and Clock Recovery Mode

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the recovered clock signal.

5.4.2 Training Mode

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin "High" or setting the RLOL_n bit to "1" in the control register. Also, the clock output on the RxClk_n pins are the same as the reference channel clock.

5.5 LOS (Loss of Signal) Detector

5.5.1 DS3 and STS-1 LOS Condition

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ±75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to "1" in the Status Control Register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ±75 pulses. An Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 11.The status of the ALOS condition is reflected in the ALOS_n Status Control Register. RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs, the RLOS_n output pin is toggled "High" and the RLOS_n bit is set to "1" in the Status Control Register.

5.5.2 Disabling ALOS and DLOS Detection

For debugging purposes it is useful to disable the ALOS and / or DLOS detection. Writing a "1" to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

5.5.3 E3 LOS Condition

If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal is defined as no transitions for 10 to 255 consecutive zeros. No transitions is defined as a signal level between 15 and 35dB below the normal. This is illustrated in Figure 8. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 8 also shows the LOS declaration and clearance conditions.

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Table 11: ALOS Declaration and Clearance Thresholds for Given REQEN Settings (DS3 and STS-1 Applications)

Application	REQEN Setting	Signal Level to Declare ALOS Defect	Signal Level to Clear ALOS Defect
DS3	0	< 41mVpk	> 102mVpk
	1	< 52mVpk	> 117mVpk
STS-1	0	< 51mVpk	> 114mVpk
	1	< 58mVpk	> 133mVpk

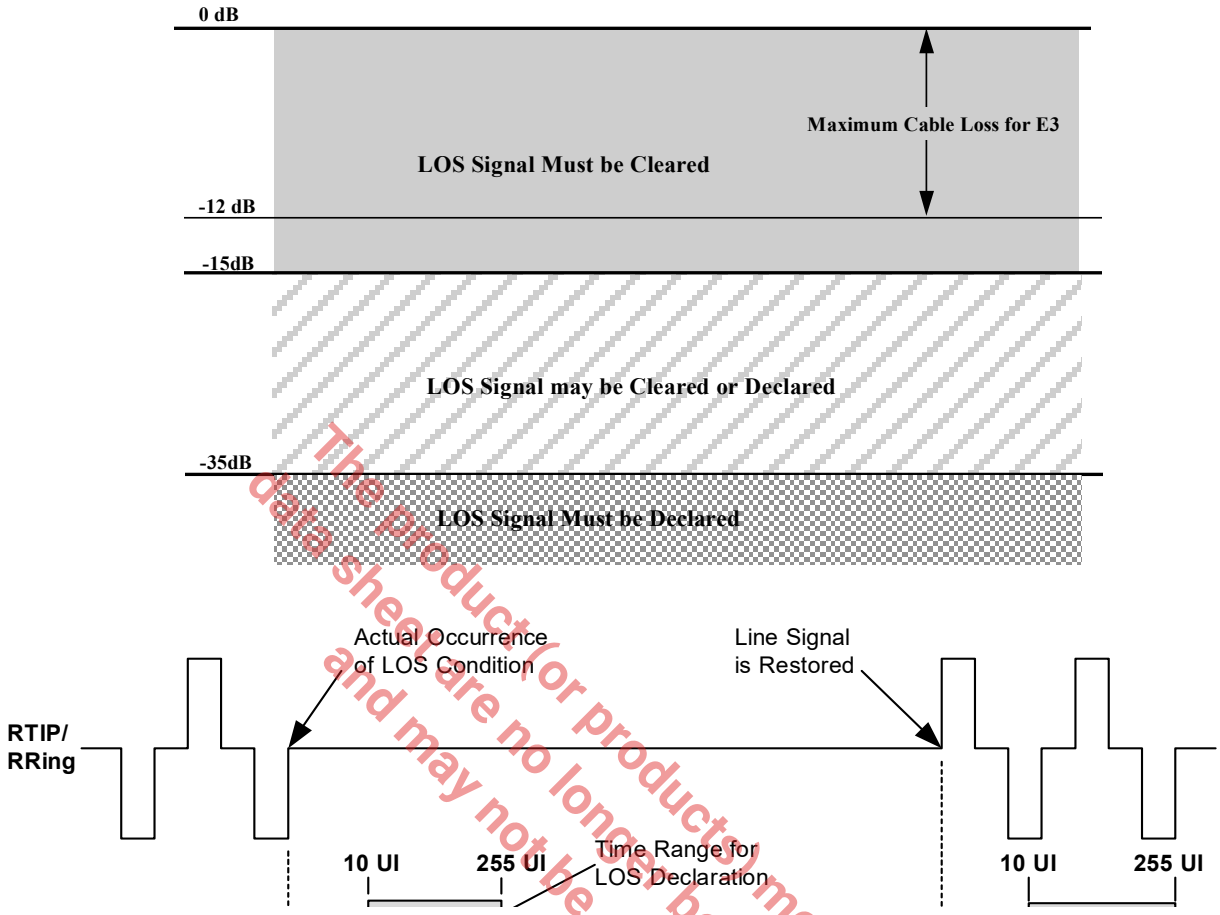

Figure 8: Loss of Signal Definition for E3 as per ITU-T G.775

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5.5.4 Interference Tolerance

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 9 shows the configuration to test the interference margin for DS3 and STS1. Figure 10 shows the set up for E3.

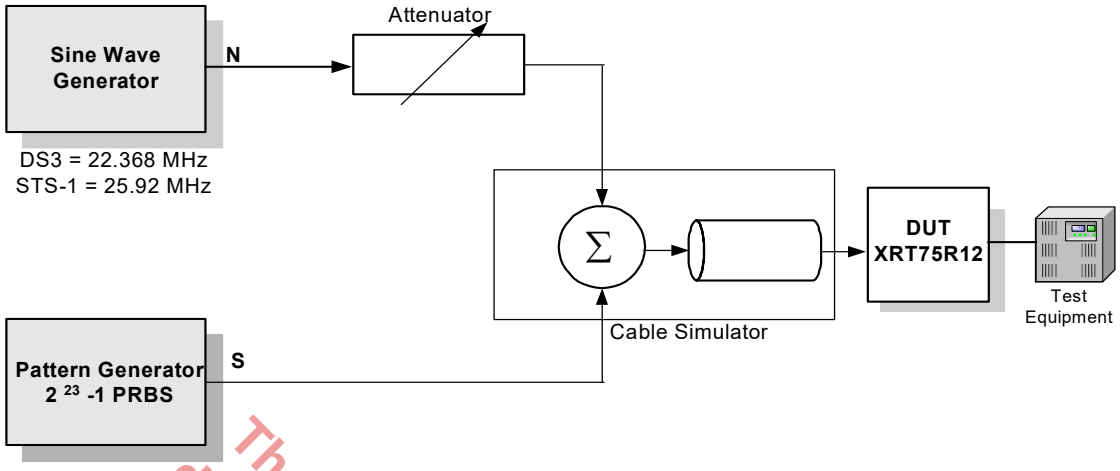

Figure 9: Interference Margin Test Set Up for DS3 and STS-1

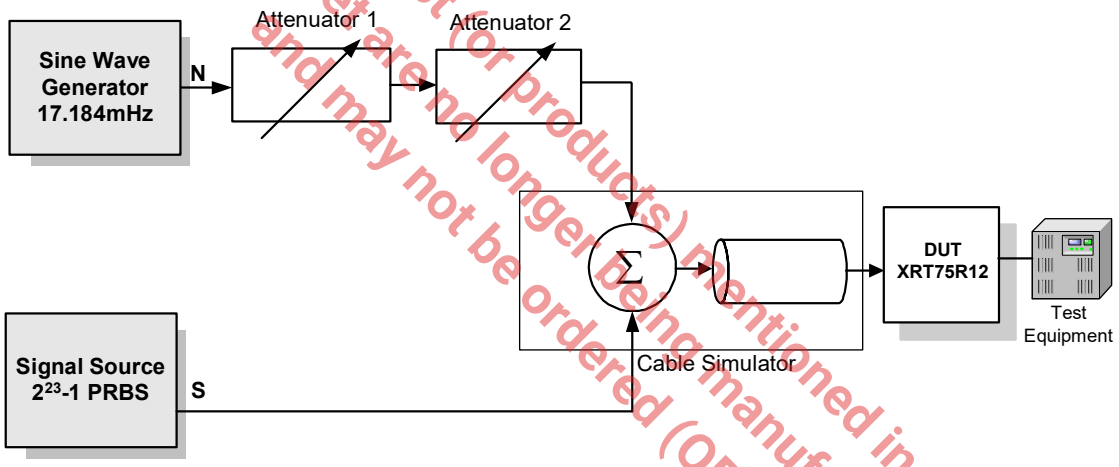

Figure 10: Interference Margin Test Set Up for E3

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Table 12: Interference Margin Test Results

Mode	Cable Length (Attenuation)	Interference Tolerance
E3	0dB	Equalizer "IN"
		–17dB
	12dB	–14dB
DS3	0ft	–15dB
	225ft	–15dB
	450ft	–14dB
STS-1	0ft	–15dB
	225ft	–14dB
	450ft	–14dB

5.5.5 Muting the Recovered Data with LOS Condition

When the LOS condition is declared, the Clock Recovery circuit locks into the reference clock applied to the internal master clock outputs this clock onto the RxClk_n output pin. The data on the RxPOS_n and RxNEG_n pins can be forced to zero by setting the LOSMUT_n bits in the individual channel control register to “1”.

Note: When the LOS condition is cleared, the recovered data is output on RxPOS_n and RxNEG_n pins.

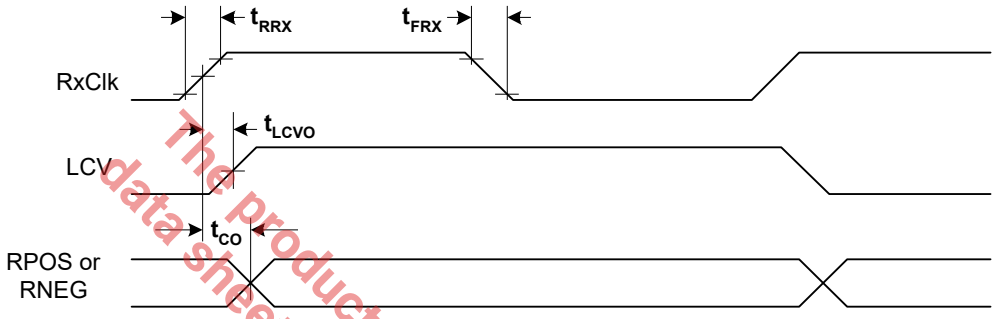

Figure 11: Receiver Data Output and Code Violation Timing

Table 13: Receiver Data Output and Code Violation Timing

Symbol	Parameter	Min	Typ	Max	Units
RxClk	Duty Cycle	45	50	55	%
	RxClk Frequency				
	E3		34.368		MHz
	DS3		44.736		MHz
	STS-1		51.84		MHz
t_{RRX}	RxClk rise time (10% to 90%)		2	4	ns
t_{FRX}	RxClk fall time (10% to 90%)		2	4	ns
t_{CO}	RxClk to RPOS or RNEG delay time			4	ns
t_{LCVO}	RxClk to rising edge of LCV output delay		2.5		ns

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5.6 B3ZS and HDB3 Decoder

The decoder block takes the output from the clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream. Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active “High” pulse is generated on the RLCV_n output pins to indicate line code violation.

6.0 Transmitter

The transmitter is designed so that the LIU can accept serial data from a local device, encode the data properly, and then output an analog pulse according to the pulse shape chosen in the appropriate registers. This section describes the detailed operation of various blocks within the transmit path. A simplified block diagram of the transmit path is shown in Figure 12.

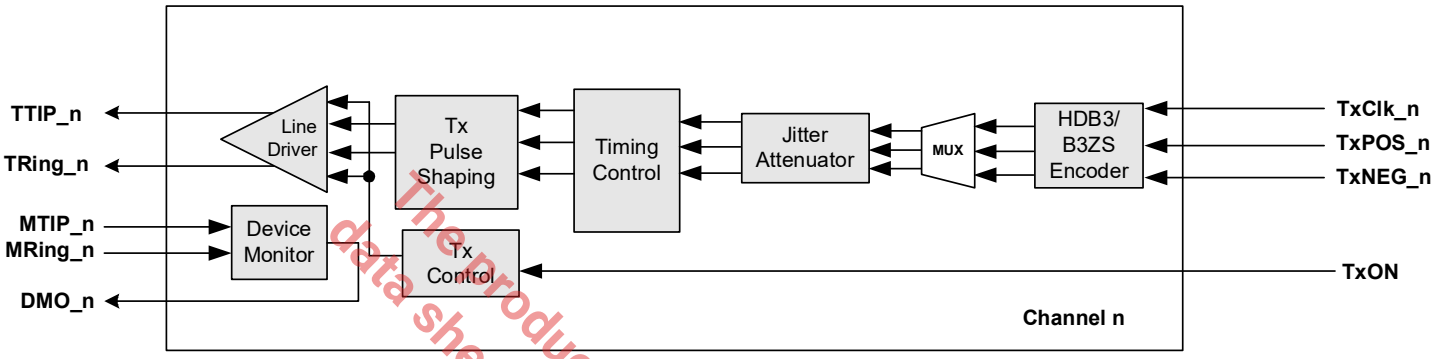

Figure 12: Transmit Path Block Diagram

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6.1 Transmit Digital Input Interface

The method for applying data to the transmit inputs of the LIU is a serial interface consisting of TxClk, TxPOS, and TxNEG. For single rail mode, only TxClk and TxPOS are necessary for providing the local data from a framer device or ASIC. Data can be sampled on either edge of the input clock signal by programming the appropriate register. A typical interface is shown in Figure 13.

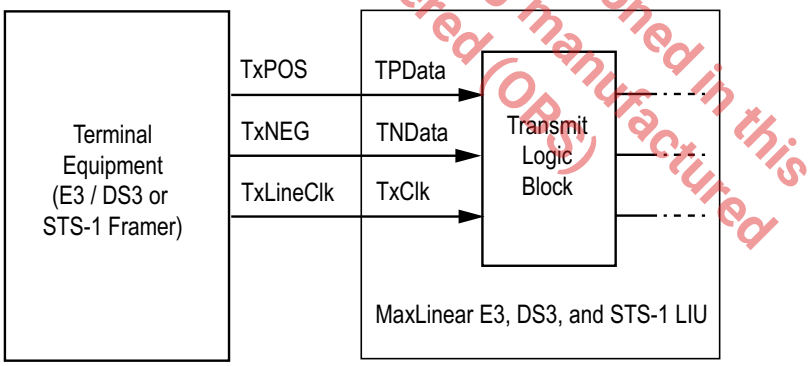

Figure 13: Typical Interface Between Terminal Equipment and the XRT75R12 (Dual-Rail Data)

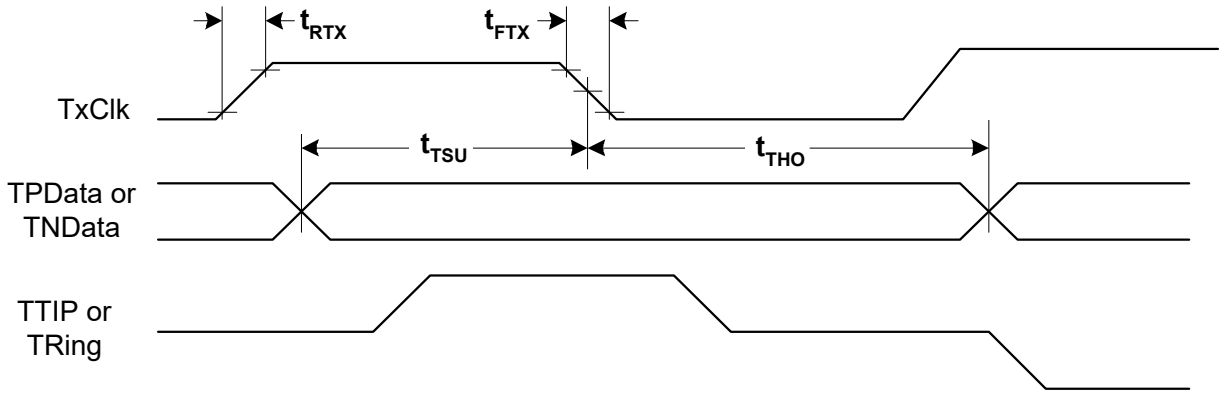

Figure 14: Transmitter Terminal Input Timing

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Table 14: Transmitter Terminal Input Timing

Symbol	Parameter	Min	Typ	Max	Units
TxClk	Duty Cycle	30	50	70	%
	TxClk Frequency				
	E3		34.368		MHz
	DS3		44.736		MHz
	STS-1		51.84		MHz
t_{RTX}	TxClk rise time (10% to 90%)			4	ns
t_{FTX}	TxClk fall time (10% to 90%)			4	ns
t_{TSU}	TPData or TNData to TxClk falling set up time	3			ns
t_{THO}	TPData or TNData to TxClk falling hold time	3			ns

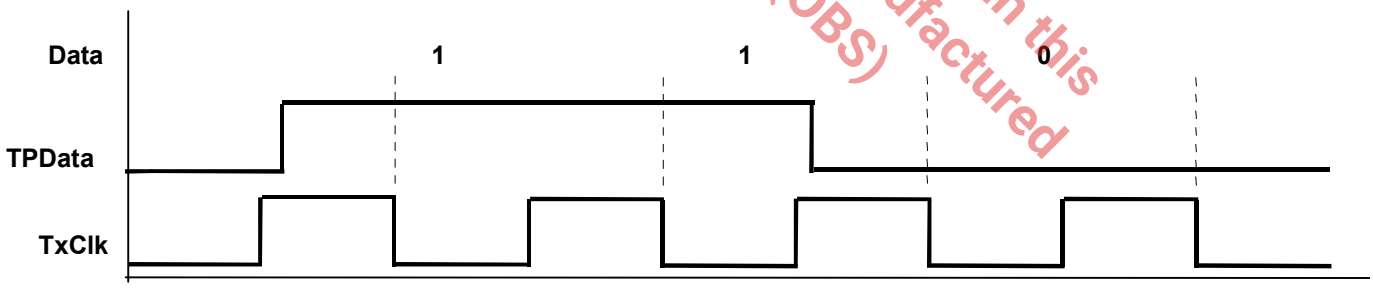

Figure 15: Single-Rail or NRZ Data Format (Encoder and Decoder are Enabled)

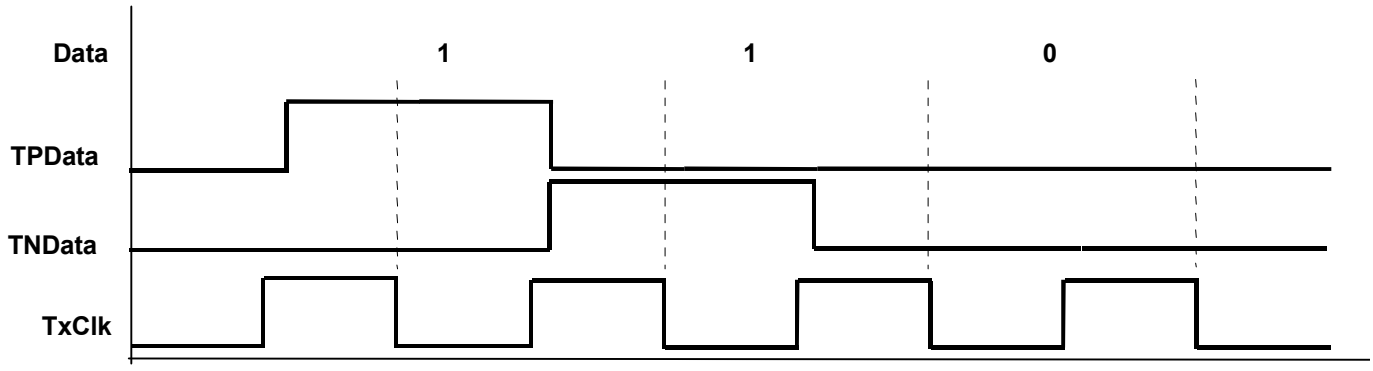

Figure 16: Dual-Rail Data Format (Encoder and Decoder are Disabled)

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

6.2 Transmit Clock

The transmit clock applied via TxClk_n pins, for the selected data rate (E3 = 34.368MHz, DS3 = 44.736MHz, or STS-1 = 51.84MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle transmit clock to be supplied.

6.3 B3ZS and HDB3 Encoder

When the Single-Rail (NRZ) data format is selected, the encoder block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

6.3.1 B3ZS Encoding

An example of B3ZS encoding is shown in Figure 17. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (for example, a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

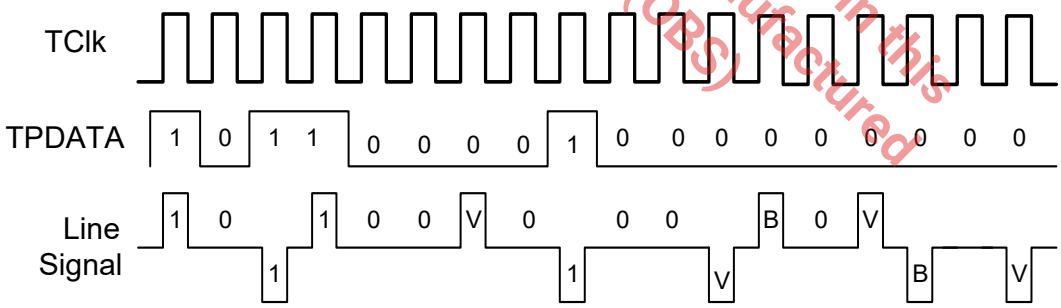

Figure 17: B3ZS Encoding Format

6.3.2 HDB3 Encoding

An example of the HDB3 encoding is shown in Figure 18. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either a 000V or B00V pattern. The substitution code is made in such a way that an odd number of pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

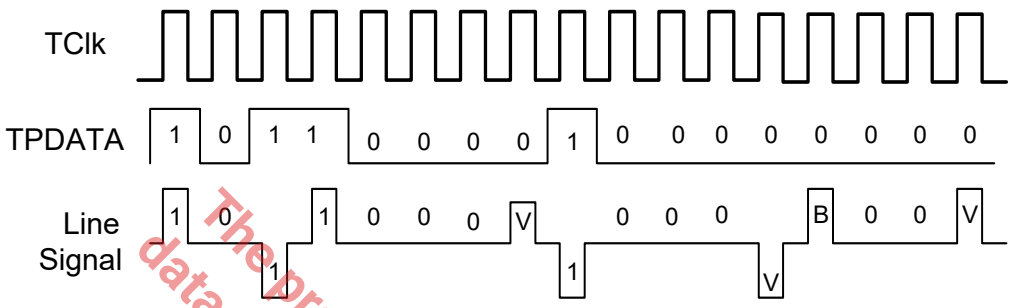

Figure 18: HDB3 Encoding Format

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6.4 Transmit Pulse Shaper

The transmit pulse shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meets the industry standard mask template requirements for STS-1 and DS3. For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. The pulse shaper block also includes a transmit build out circuit, which can either be disabled or enabled by setting the TxLEV_n bit to “1” or “0” in the control register. For DS3 or STS-1 rates, the transmit build out circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet. For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the transmit build out circuit is always disabled. The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 19.

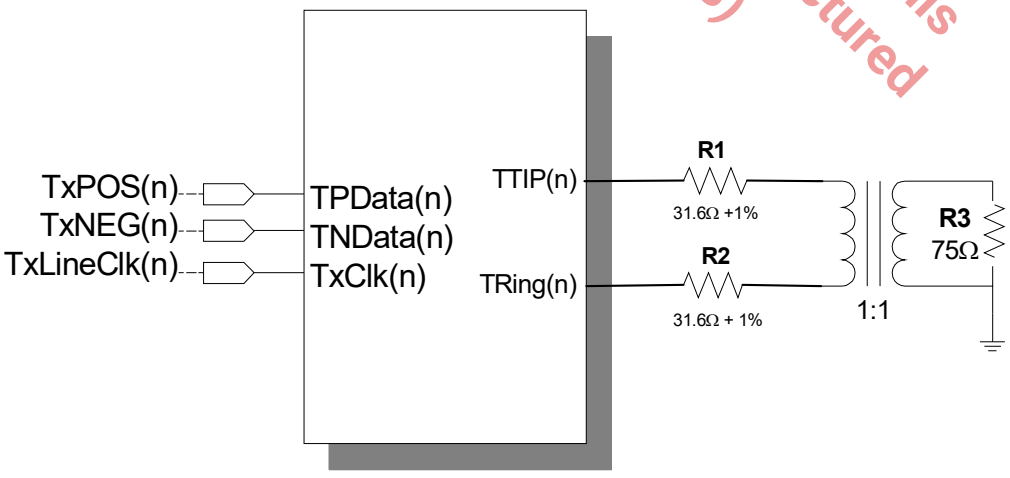

Figure 19: Transmit Pulse Shape Test Circuit

6.4.1 Guidelines for Using Transmit Build Out Circuit

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system is less than 225 feet, enable the transmit build out circuit by setting the TxLEV_n control bit to “0”. If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the transmit build out circuit.

6.5 E3 Line Side Parameters

The XRT75R12 line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368Mbps operation. The pulse mask as specified in ITU-T G.703 for 34.368Mbps is shown in Figure 20.

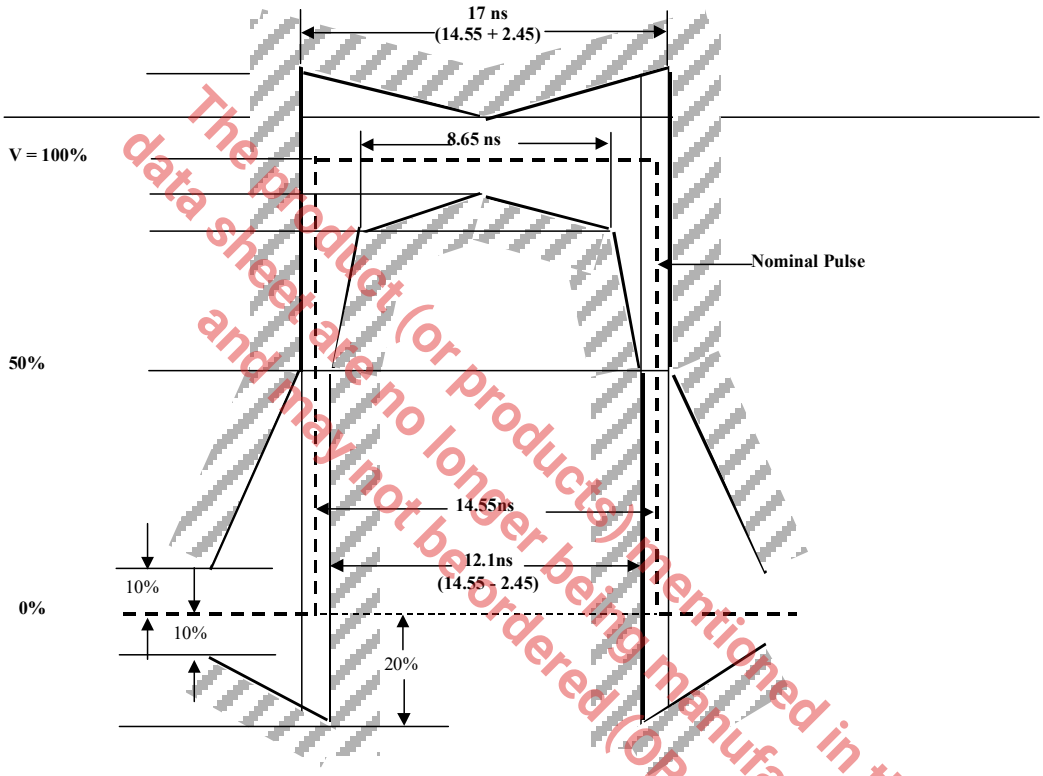

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Figure 20: Pulse Mask for E3 (34.368Mbps) Interface per ITU-T G.703

Table 15: E3 Transmitter Line Side Output and Receiver Line Side Input Specifications

Parameter	Min	Typ	Max	Units
Transmitter Line Side Output Characteristics				
Transmit output pulse amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit output pulse amplitude ratio	0.95	1.00	1.05	
Transmit output pulse width	12.5	14.55	16.5	ns
Transmit intrinsic jitter		0.02	0.05	UI_{PP}
Receiver Line Side Input Characteristics				
Receiver sensitivity (length of cable)	900	1200		feet
Interference margin	-20	-14		dB
Jitter tolerance at jitter frequency 800kHz	0.15	0.28		UI_{PP}
Signal level to declare Loss of Signal			-35	dB
Signal level to clear Loss of Signal	-15			dB
Occurrence of LOS to LOS declaration time	10		255	UI
Termination of LOS to LOS clearance time	10		255	UI

1. The above values are at T_A = 25°C and V_{DD} = 3.3V ±5%.

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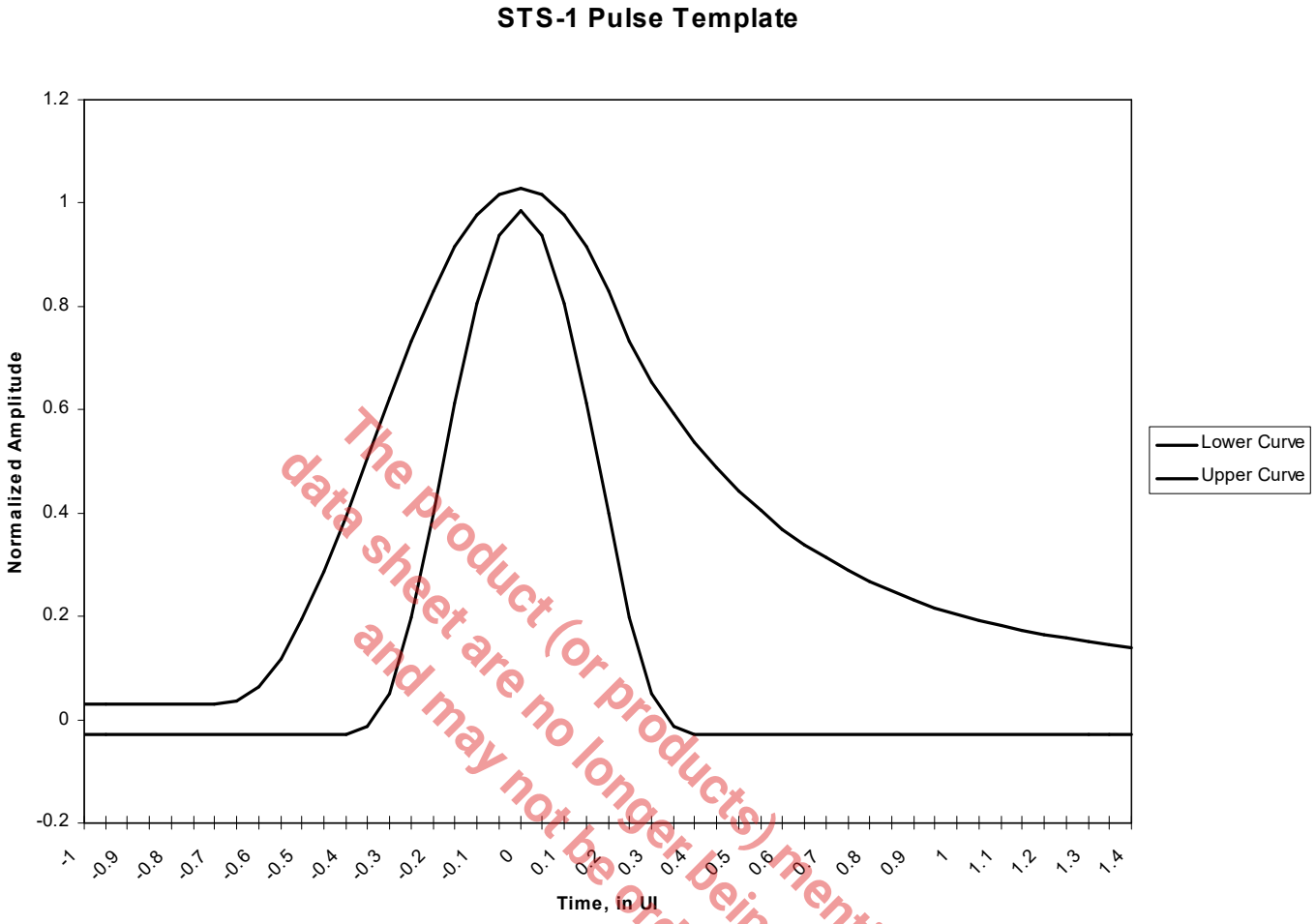

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Figure 21: Bellcore GR-253 Core Transmit Output Pulse Template for SONET STS-1 Applications

Table 16: STS-1 Pulse Mask Equations

Time in Unit Intervals	Normalized Amplitude
Lower Curve	
–0.85 ≤ T ≤ –0.38	–0.03
–0.38 ≤ T ≤ 0.36	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
0.36 ≤ T ≤ 1.4	–0.03
Upper Curve	
–0.85 ≤ T ≤ –0.68	0.03
–0.68 ≤ T ≤ –0.26	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
0.26 ≤ T ≤ 1.4	$0.1 + 0.61 \times e^{-2.4[T - 0.26]}$

Table 17: STS-1 Transmitter Line Side Output and Receiver Line Side Input Specifications (GR-253)

Parameter	Min	Typ	Max	Units
Transmitter Line Side Output Characteristics				
Transmit output pulse amplitude (Measured with TxLEV = 0)	0.65	0.75	0.90	V_{pk}
Transmit output pulse amplitude (Measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit output pulse width	8.6	9.65	10.6	ns
Transmit output pulse amplitude ratio	0.90	1.00	1.10	
Transmit intrinsic jitter		0.02	0.05	UI_{PP}
Receiver Line Side Input Characteristics				
Receiver sensitivity (length of cable)	900	1100		feet
Jitter tolerance at jitter frequency 400kHz	0.15			UI_{PP}
Signal level to declare Loss of Signal	Refer to Table 11			
Signal level to clear Loss of Signal	Refer to Table 11			

1. The above values are at T_A = 25°C and V_{DD} = 3.3V ±5%.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

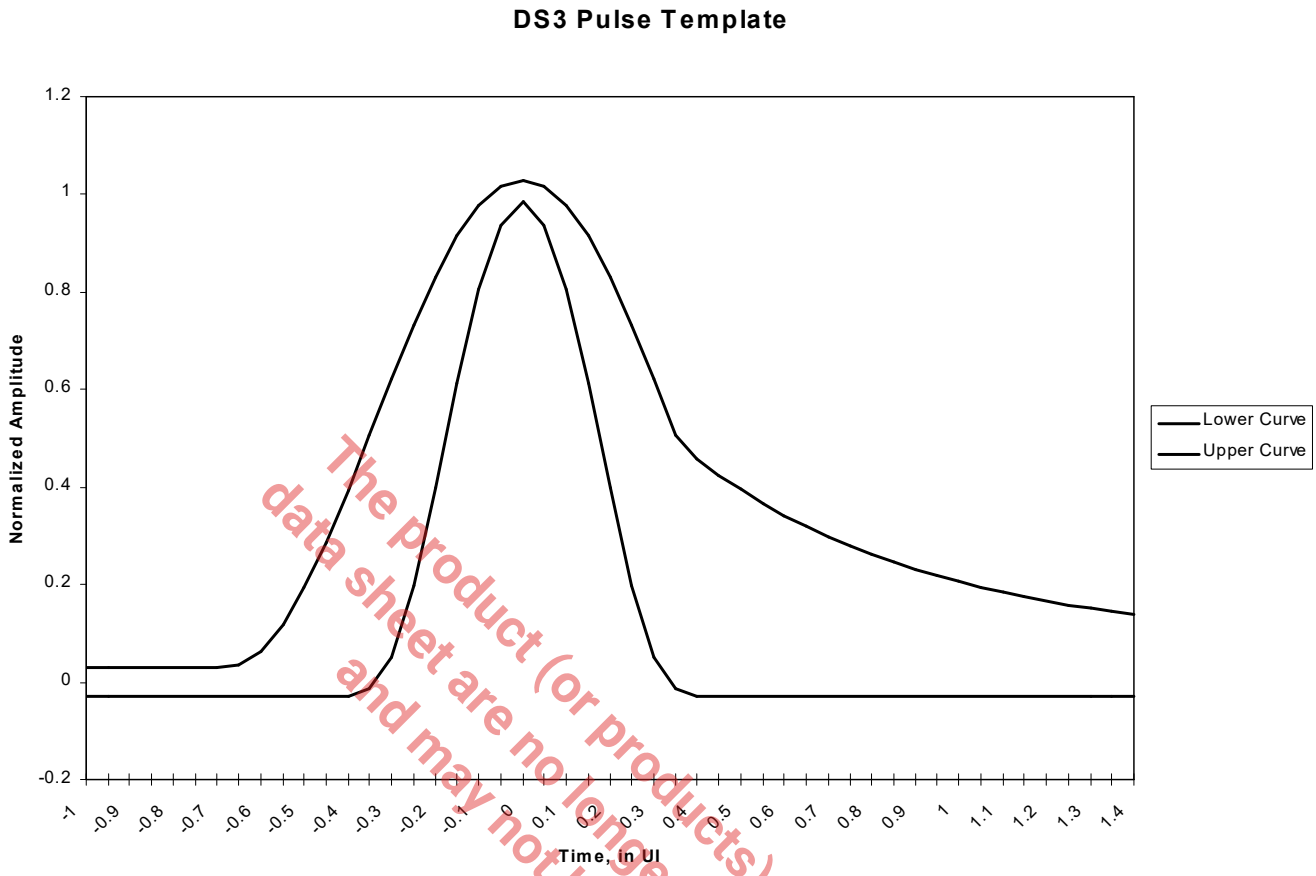

Figure 22: Transmit Output Pulse Template for DS3 as per Bellcore GR-499

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 18: DS3 Pulse Mask Equations

Time in Unit Intervals	Normalized Amplitude
Lower Curve	
–0.85 ≤ T ≤ –0.36	–0.03
–0.36 ≤ T ≤ 0.36	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
0.36 ≤ T ≤ 1.4	–0.03
Upper Curve	
–0.85 ≤ T ≤ –0.68	0.03
–0.68 ≤ T ≤ 0.36	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
0.36 ≤ T ≤ 1.4	$0.08 + 0.407 \times e^{-1.84[T - 0.36]}$

Table 19: DS3 Transmitter Line Side Output and Receiver Line Side Input Specifications (GR-499)

Parameter	Min	Typ	Max	Units
Transmitter Line Side Output Characteristics				
Transmit output pulse amplitude (Measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit output pulse amplitude (Measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit output pulse width	10.10	11.18	12.28	ns
Transmit output pulse amplitude ratio	0.90	1.00	1.10	
Transmit intrinsic jitter		0.02	0.05	UI_{PP}
Receiver Line Side Input Characteristics				
Receiver sensitivity (length of cable)	900	1100		feet
Jitter tolerance at 400kHz (Cat II)	0.15			UI_{PP}
Signal level to declare Loss of Signal	Refer to Table 11			
Signal level to clear Loss of Signal	Refer to Table 11			

1. The above values are at T_A = 25°C and V_{DD} = 3.3V ±5%.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

6.6 Transmit Drive Monitor

This feature is used for monitoring the transmit line for occurrence of fault conditions such as a short circuit on the line or a defective line driver. To activate this function, connect MTIP_n pins to the TTIP_n lines via a 270Ω resistor and MRing_n pins to TRing_n lines via 270Ω resistor as shown in Figure 23.

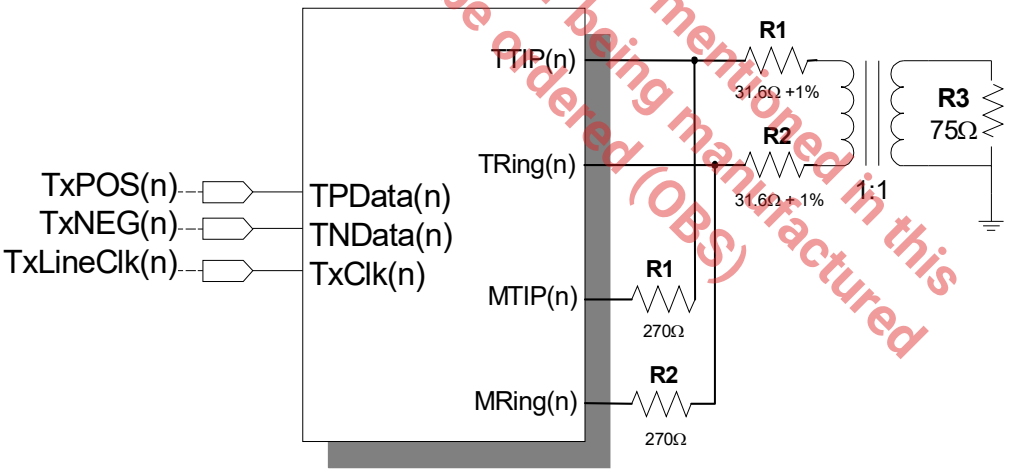

Figure 23: Transmit Driver Monitor Set Up

When the MTIP_n and MRing_n are connected to the TTIP_n and TRing_n lines, the Drive Monitor circuit monitors the line for transitions. The DMO_n (Drive Monitor Output) will be asserted “Low” as long as the transitions on the line are detected via MTIP_n and MRing_n. If no transitions on the line are detected for 128 ±32 TxClk_n periods, the DMO_n output toggles “High” and when the transitions are detected again, DMO_n toggles “Low”.

Note: The Drive Monitor circuit is only for diagnostic purpose and does not have to be used to operate the transmitter.

6.7 Transmitter Section On or Off

The transmitter section of each channel can either be turned on or off. To turn on the transmitter, set the input pin TxON to “High” and write a “1” to the TxON_n control bit. When the transmitter is turned off, TTIP_n and TRing_n are tri-stated.

Notes:

1. This feature provides support for redundancy.
2. If the XRT75R12 is configured in Host Mode, to permit a system designed for redundancy to quickly shut off the defective line card and turn on the back-up line card, writing a “1” to the TxON_n control bits transfers the control to the TxON pin.

7.0 Jitter

There are three fundamental parameters that describe circuit performance relative to jitter:

- Jitter Tolerance
- Jitter Transfer
- Jitter Generation

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

7.1 Jitter Tolerance

Jitter tolerance is a measure of how well a clock and data recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 24, jitter is introduced by the sinusoidal modulation of the serial data bit sequence. Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points. Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

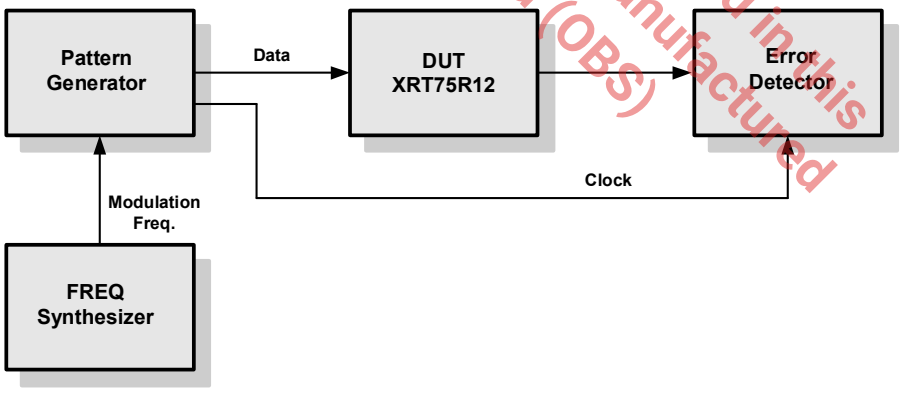

Figure 24: Jitter Tolerance Measurements

7.1.1 DS3 and STS-1 Jitter Tolerance Requirements

Bellcore GR-499 CORE specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 25 shows the jitter tolerance curve as per GR-499 specification.

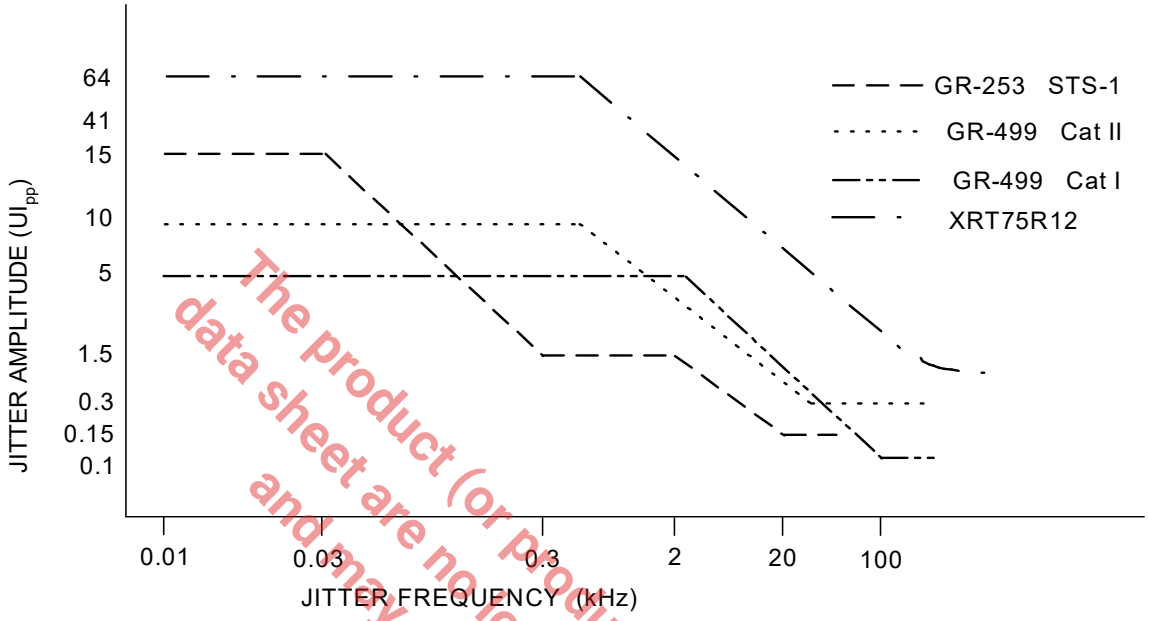

Figure 25: Input Jitter Tolerance for DS3 and STS-1

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7.1.2 E3 Jitter Tolerance Requirements

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to tolerate jitter up to certain specified limits. Figure 26 shows the tolerance curve.

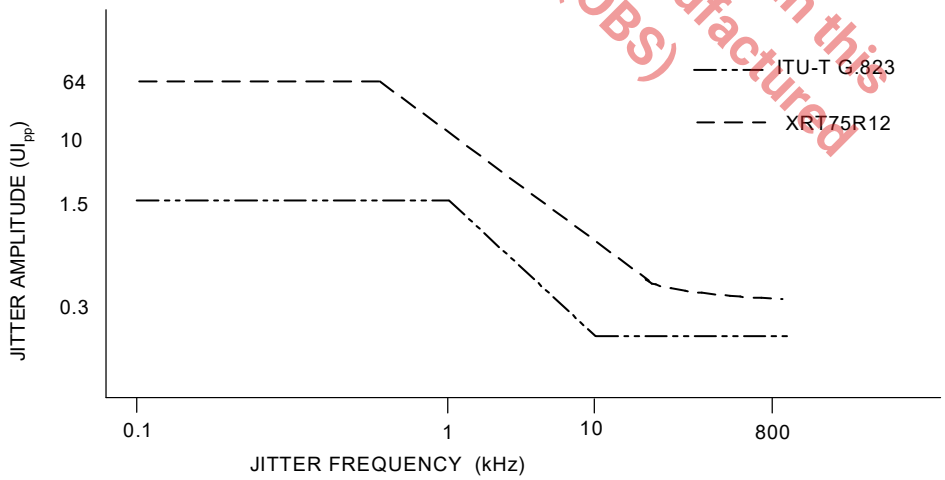

Figure 26: Input Jitter Tolerance for E3

As shown in the jitter tolerance measurement, of the figures above, the dark line indicates the minimum level of jitter that the E3, DS3 and STS-1 compliant component must tolerate. Table 20 below shows the jitter amplitude versus the modulation frequency for various standards.

Table 20: Jitter Amplitude versus Modulation Frequency (Jitter Tolerance)

Bit Rate (kbps)	Standard	Input Jitter Amplitude (UI_{P-P})			Modulation Frequency				
		A1	A2	A3	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (Hz)	f5 (Hz)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	-
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20

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7.2 Jitter Transfer

Jitter Transfer Function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency. There are two distinct characteristics in jitter transfer: jitter gain (jitter peaking), defined as the highest ratio above 0dB and jitter transfer bandwidth. The overall jitter transfer bandwidth is controlled by a low bandwidth loop, typically using a voltage-controlled crystal oscillator (VCXO).

The Jitter Transfer Function is a ratio between the jitter output and jitter input for a component or system, often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. Table 21 shows the jitter transfer characteristics and jitter attenuation specifications for various data rates:

Table 21: Jitter Transfer Specification and Reference

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

1. The above specifications can be met only with a jitter attenuator that supports E3, DS3, and STS-1 rates.

7.3 Jitter Attenuator

An advanced crystal-less jitter attenuator per channel is included in the XRT75R12. The jitter attenuator requires no external crystal nor high-frequency reference clock. Clearing or setting the JATx_n or JARx_n bits in the channel control registers selects the jitter attenuator either in the receive or transmit path on a per channel basis. The FIFO size can be either 16-bit or 32-bit. The bits JA0_n and JA1_n can be set to an appropriate combination to select the different FIFO sizes or to disable the jitter attenuator on a per channel basis. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the de-jittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit FL_n is set to “1” in the Alarm Status Register. Reading this bit clears the FIFO and resets the bit into a default state.

Note: It is recommended to select the 16-bit FIFO for delay sensitive applications as well as for removing smaller amounts of jitter. Table 22 specifies the jitter transfer mask requirements for various data rates:

Table 22: Jitter Transfer Pass Masks

Rate (kbps)	Mask	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (Hz)	A1 (dB)	A2 (dB)
34368	G.823 ETSI-TBR-24	100	300	3k	800k	0.5	–19.5
44736	GR-499, Cat I	10	10k	-	15k	0.1	-
	GR-499, Cat II	10	56.6k	-	300k	0.1	-
	GR-253 CORE	10	40	-	15k	0.1	-
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator within the XRT75R12 meets the latest jitter attenuation specifications and jitter transfer characteristics as shown in the Figure 27.

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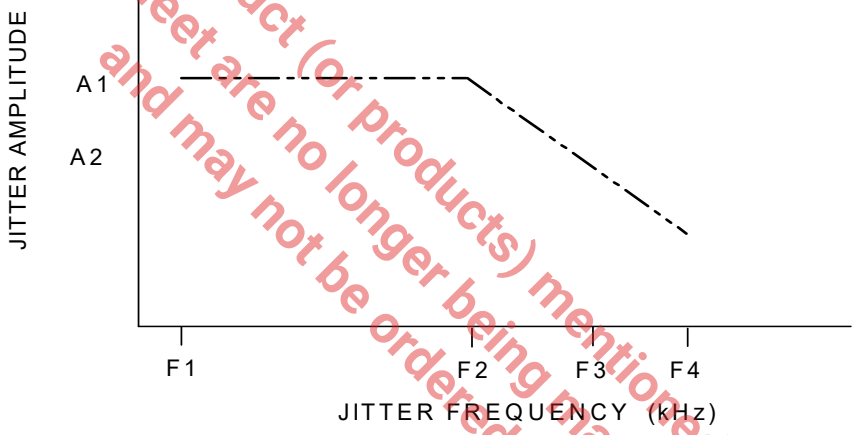

Figure 27: Jitter Transfer Requirements and Jitter Attenuator Performance

7.3.1 Jitter Generation

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

8.0 Diagnostic Features

8.1 PRBS Generator and Detector

The XRT75R12 contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purposes. With the PRBSEN_n bit = "1", the transmitter will send out a PRBS of 2^{23} - 1 in E3 rate or 2^{15} - 1 in STS-1 or DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync, the PRBSLS bit will be set to "1" and the RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling the "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at the RNEG/LCV pin will pulse "High" for one RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to the INSPRBS bit, and followed by a "1".

Figure 28 shows the status of the RNEG/LCV pin when the XRT75R12 is configured in PRBS mode.

Note: In PRBS mode, the device is forced to operate in Single-Rail Mode.

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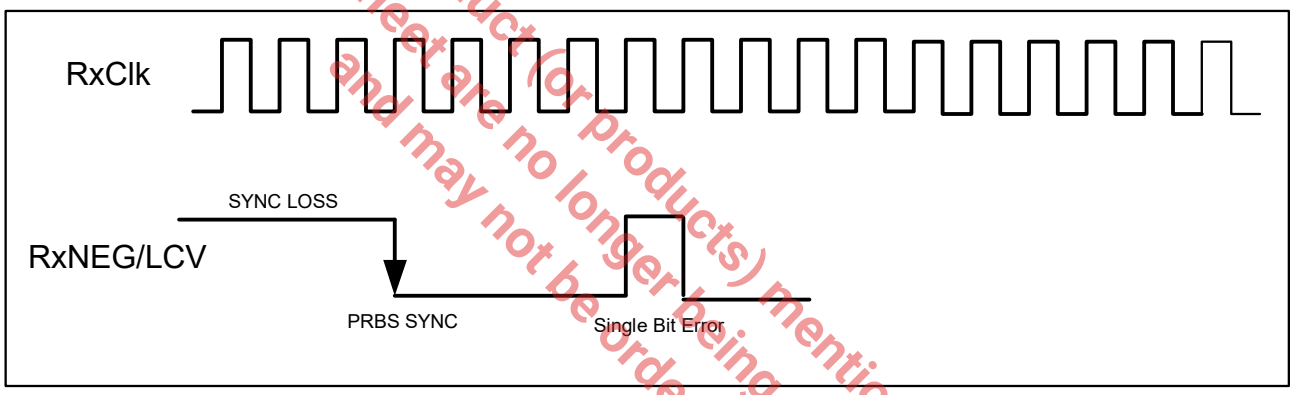

Figure 28: PRBS Mode

8.2 Loopbacks

The XRT75R12 offers three loopback modes for diagnostic purposes. The loopback modes are selected via the RLB_n and LLB_n bits and the channel control registers select the loopback modes.

8.2.1 Analog Loopback

In this mode, the transmitter outputs TTIP_n and TRing_n are internally connected to the receiver inputs RTIP_n and RRing_n as shown in Figure 29. Data and clock are output at the RxClk_n, RxPOS_n and RxNEG_n pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device, including the jitter attenuator which can be selected in either the transmit or receive path.

Notes:

1. In the Analog Loopback Mode, data is also output via TTIP_n and TRing_n pins.
2. Signals on the RTIP_n and RRing_n pins are ignored during analog loopback.

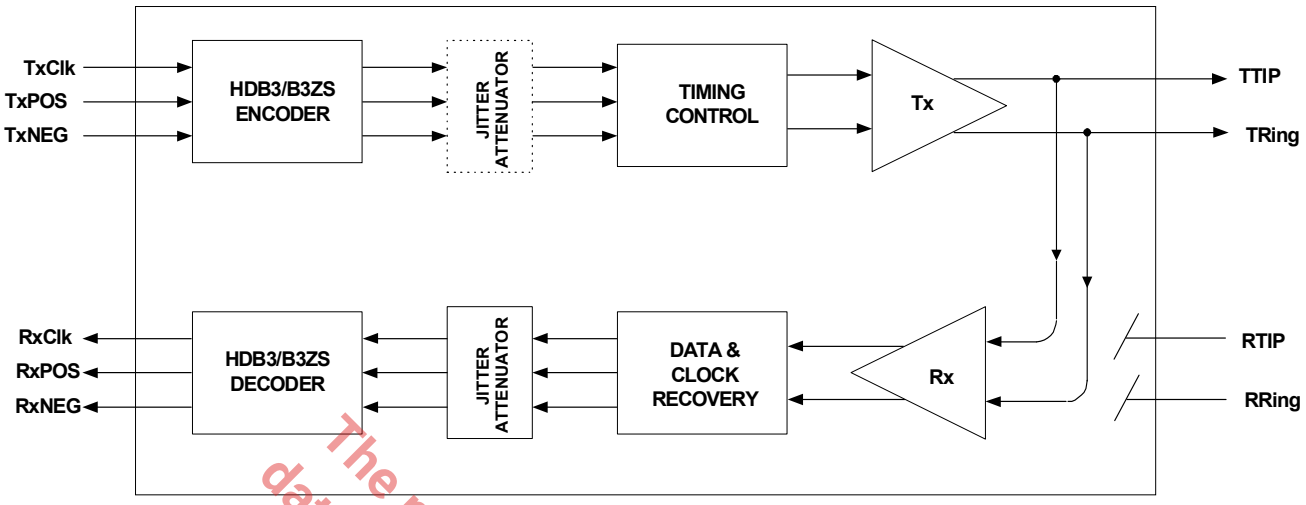

Figure 29: Analog Loopback

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8.2.2 Digital Loopback

When the digital loopback is selected, the transmit clock TxClk_n and transmit data inputs (TxPOS_n & TxNEG_n are looped back and output onto the RxClk_n, RxPOS_n and RxNEG_n pins as shown in Figure 30.

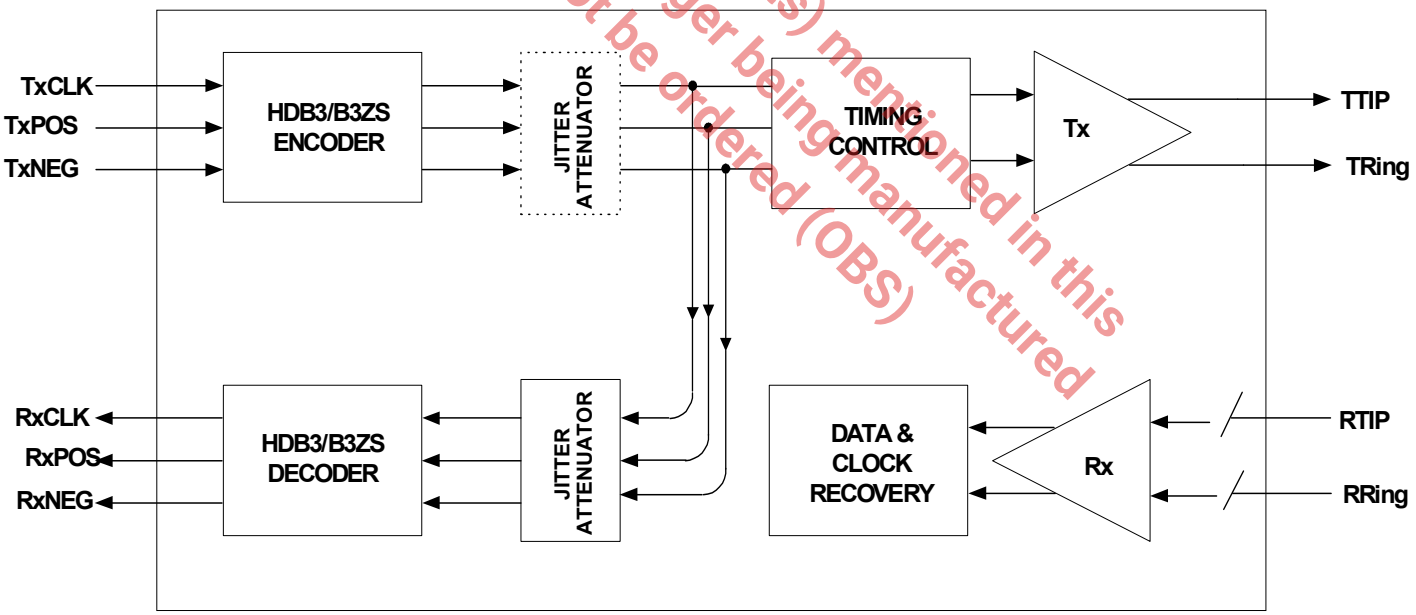

Figure 30: Digital Loopback

8.2.3 Remote Loopback

With remote loopback activated as shown in Figure 31, the receive data on RTIP and RRing is looped back after the jitter attenuator (if selected in the receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RxPOS and RxNEG pins.

Note: Input signals on TxClk, TxPOS and TxNEG are ignored during remote loopback.

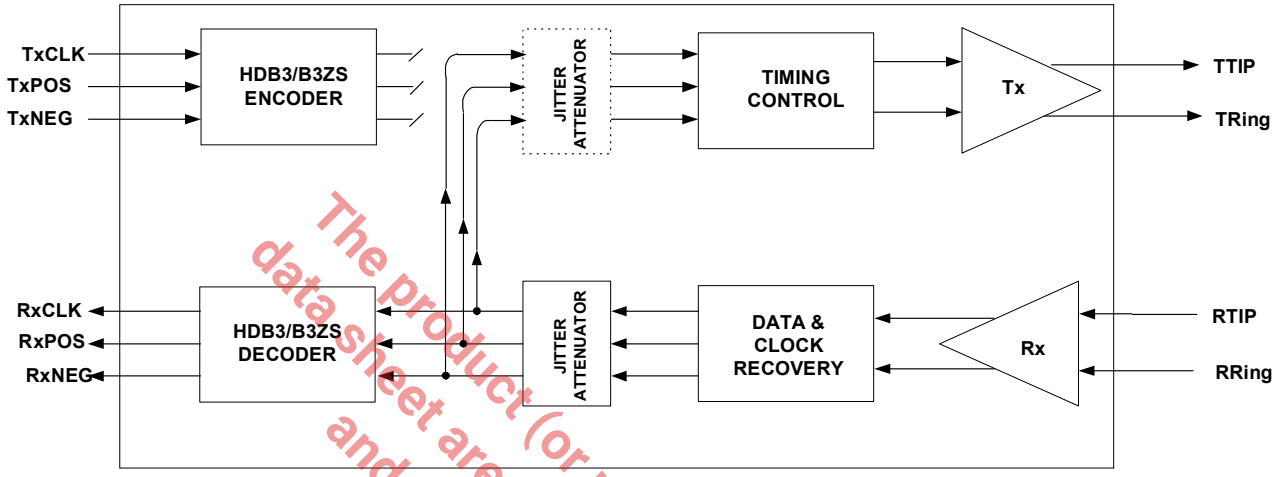

Figure 31: Remote Loopback

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8.3 Transmit All Ones (TAOS)

Transmit All Ones (TAOS) can be selected by setting the TAOS_n control bits to “1” in the channel control registers. When the TAOS is set, the transmit section generates and transmits a continuous AMI all “1’s” pattern on the TTIP_n and TRing_n pins. The frequency of this ones pattern is determined by TxClk_n. The TAOS data path is shown in Figure 32. TAOS does not operate in Analog Loopback or Remote Loopback Modes, however will function in Digital Loopback Mode.

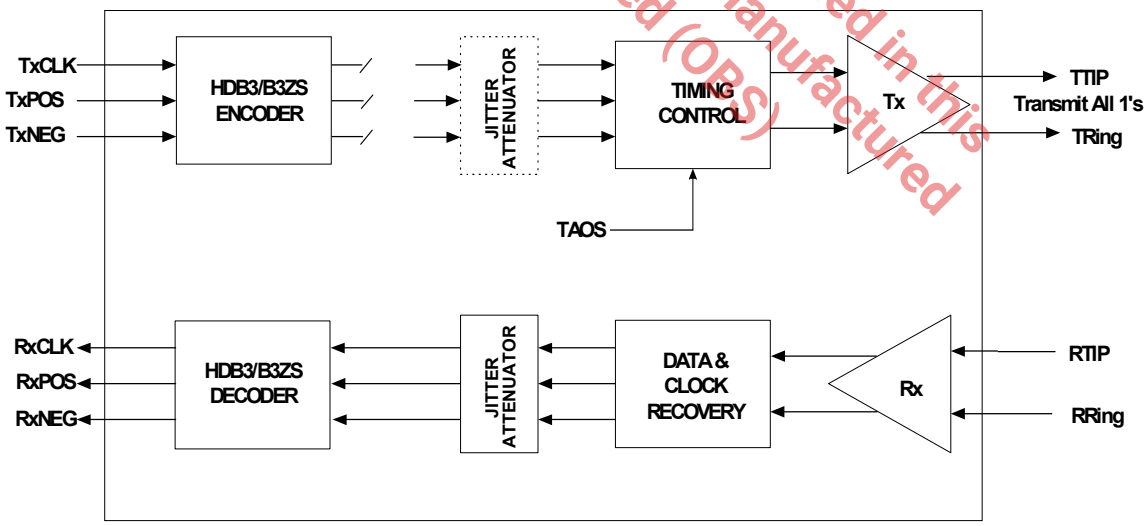

Figure 32: Transmit All Ones (TAOS)

9.0 Microprocessor Interface Block

The microprocessor interface section supports communication between the local microprocessor (µP) and the LIU. The XRT75R12 supports a parallel interface asynchronously or synchronously timed to the LIU. The microprocessor interface is selected by the state of the Pmode input pin. Selecting the microprocessor interface mode is shown in Table 23.

Table 23: Selecting the Microprocessor Interface Mode

Pmode	Microprocessor Mode
"Low"	Asynchronous mode
"High"	Synchronous mode

The local µP configures the LIU by writing data into specific addressable, on-chip read and write registers. The µP provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The µP also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor interface is shown in Figure 33.

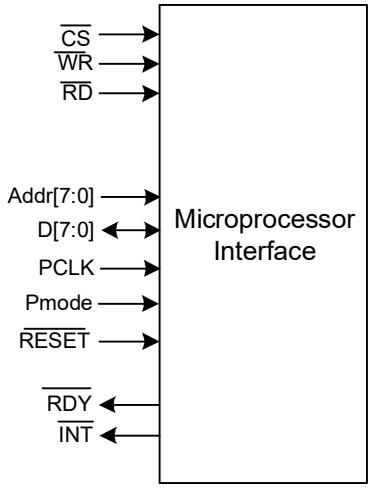

Figure 33: Simplified Block Diagram, Microprocessor Interface

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9.1 Microprocessor Interface Signals

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address, and control signals. These interface signals are described below in Table 24. The microprocessor interface can be configured to operate in Asynchronous Mode or Synchronous Mode.

Table 24: XRT75R12 Microprocessor Interface Signals

Pin Name		Type	Description
Pmode	Mode select input pin	I	This pin is used to specify the microprocessor interface mode.
D[7:0]	Bi-Directional data bus	I/O	For register "read" or "write" operations.
Addr[7:0]	Eight-bit address bus inputs	I	The XRT75R12 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for read and write access.
$\overline{CS}$	Chip select input	I	This active low signal selects the microprocessor interface of the XRT75R12 LIU and enables read and write operations with the on-chip register locations.
$\overline{RD}$	Read signal	I	This active low input functions as the read signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”), the LIU is informed that a read operation has been requested and begins the process of the read cycle.
$\overline{WR}$	Write signal	I	This active low input functions as the write signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”), the LIU is informed that a write operation has been requested and begins the process of the write cycle.
$\overline{RDY}$	Ready output	O	This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.
$\overline{INT}$	Interrupt output	O	This active low signal is provided by the LIU to alert the local µP that a change in alarm status has occurred. This pin is Reset Upon Read (RUR) once the alarm status registers have been cleared.
$\overline{RESET}$	Reset input	I	This active low input pin is used to Reset the LIU.

9.2 Asynchronous and Synchronous Description

Whether the LIU is configured for Asynchronous or Synchronous Mode, the following descriptions apply. The Synchronous Mode requires an input clock (PCLK) to be used as the microprocessor timing reference. Read and write operations are described below.

Read Cycle (For Pmode = "0" or "1")

Whenever the local µP wishes to read the contents of a register, it should do the following:

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables communication between the µP and the LIU microprocessor interface block.
3. Next, the µP should indicate that this current bus cycle is a read operation by toggling the $\overline{RD}$ input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
4. After the µP toggles the read signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
5. After the µP detects the $\overline{RDY}$ signal and has read the data, it can terminate the read cycle by toggling the $\overline{RD}$ input pin "High".
6. The $\overline{CS}$ input pin must be pulled "High" before a new command can be issued.

Write Cycle (For Pmode = "0" or "1")

Whenever a local µP wishes to write a byte or word of data into a register within the LIU, it should do the following:

1. Place the address of the target register on the address bus input pins Addr[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables communication between the µP and the LIU microprocessor interface block.
3. The µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus D[7:0].
4. Next, the µP should indicate that this current bus cycle is a write operation by toggling the $\overline{WR}$ input pin "Low". This action enables the bi-directional data bus input drivers of the LIU.
5. After the µP toggles the write signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.
6. The $\overline{CS}$ input pin must be pulled "High" before a new command can be issued.

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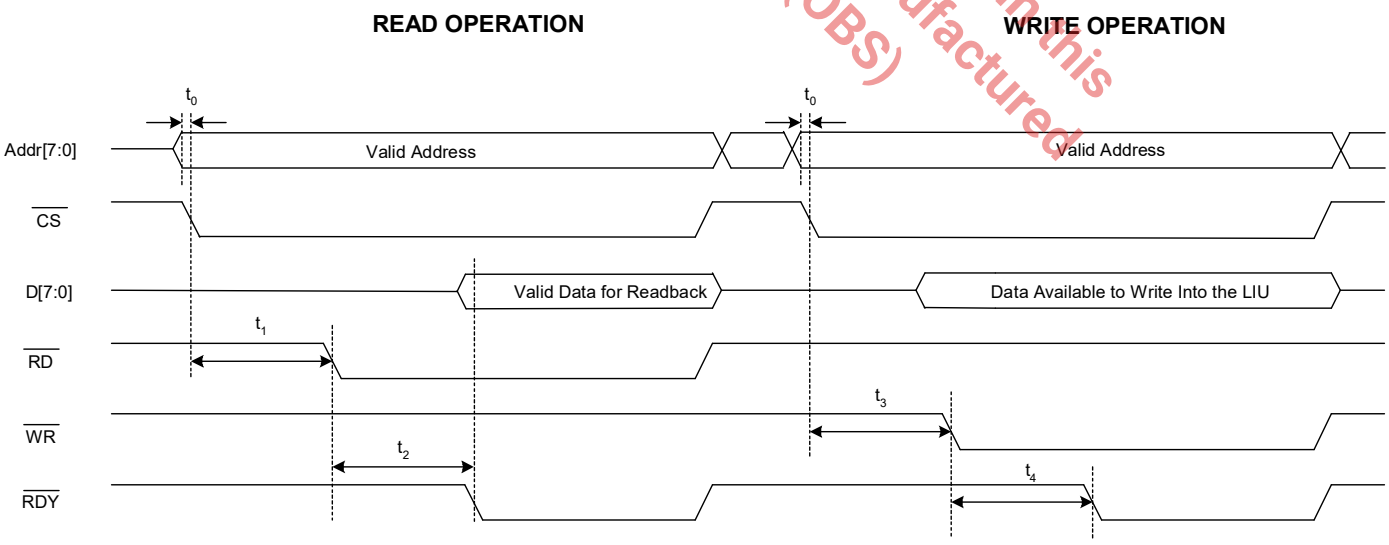

Figure 34: Asynchronous µP Interface Signals During Programmed I/O Read and Write Operations

Table 25: Asynchronous Timing Specifications

Symbol	Parameter	Min	Max	Units
t_0	Valid address to $\overline{CS}$ falling edge	0	-	ns
t_1	$\overline{CS}$ falling edge to $\overline{RD}$ assert	0	-	ns
t_2	$\overline{RD}$ assert to $\overline{RDY}$ assert	-	65	ns
NA	$\overline{RD}$ pulse width (t_2)	70	-	ns
t_3	$\overline{CS}$ falling edge to $\overline{WR}$ assert	0	-	ns
t_4	$\overline{WR}$ assert to $\overline{RDY}$ assert	-	65	ns
NA	$\overline{WR}$ pulse width (t_4)	70	-	ns

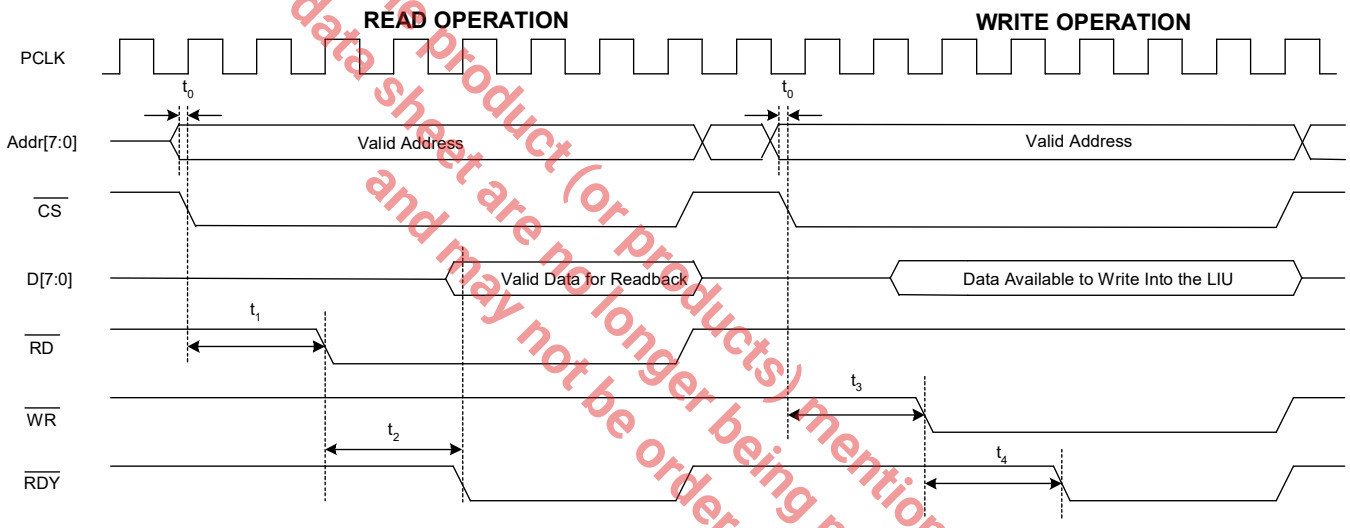

Figure 35: Synchronous µP Interface Signals During Programmed I/O Read and Write Operations

Table 26: Synchronous Timing Specifications

Symbol	Parameter	Min	Max	Units
t_0	Valid address to $\overline{CS}$ falling edge	0	-	ns
t_1	$\overline{CS}$ falling edge to $\overline{RD}$ assert	0	-	ns
t_2	$\overline{RD}$ assert to $\overline{RDY}$ assert	-	35	ns(1)
NA	$\overline{RD}$ pulse width (t_2)	40	-	ns
t_3	$\overline{CS}$ falling edge to $\overline{WR}$ assert	0	-	ns
t_4	$\overline{WR}$ assert to $\overline{RDY}$ assert	-	35	ns(1)
NA	$\overline{WR}$ pulse width (t_4)	40	-	ns
	PCLK period	15		ns
	PCLK duty cycle			
	PCLK "High / Low" time			

1. This timing parameter is based on the frequency of the synchronous clock (PCLK). To determine the access time, use the following formula: ($PCLK_{period}$ * 2) + 5ns

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

9.3 Register Map

Table 27: XRT75R12 Command Register Address Map

Address (Hex)	Command Register (Decimal)	Label	Type	Register Name
0x00	CR0	APST	R/W	APS transmit redundancy control register 0-5
Channel 0 Control Registers				
0x01	CR1	IER0	R/W	Source Level Interrupt Enable Register - Ch 0
0x02	CR2	ISR0	RUR	Source Level Interrupt Status Register - Ch 0
0x03	CR3	AS0	R/O	Alarm Status Register - Ch 0
0x04	CR4	TC0	R/W	Transmit Control Register - Ch 0
0x05	CR5	RC0	R/W	Receive Control Register - Ch 0
0x06	CR6	CC0	R/W	Channel Control Register - Ch 0
0x07	CR7	JA0	R/W	Jitter Attenuator Control Register - Ch 0
0x08	CR8	APSR	R/W	APS Receive Redundancy Control Register 0-5
0x09				
0x0A	CR10	EM0	R/W	Error Counter MS Byte Ch 0
0x0B	CR11	EL0	R/W	Error Counter LS Byte
0x0C	CR12	EH0	R/W	Error Counter Holding Register
0x0D				
0x0E				
0x0F				
0x10				
Channel 1 Control Registers				
0x11	CR17	IER1	R/W	Source Level Interrupt Enable Register - Ch 1
0x12	CR18	ISR1	RUR	Source Level Interrupt Status Register - Ch 1
0x13	CR19	AS1	R/O	Alarm Status Register - Ch 1
0x14	CR20	TC0	R/W	Transmit Control Register - Ch 1
0x15	CR21	RC1	R/W	Receive Control Register - Ch 1
0x16	CR22	CC1	R/W	Channel Control Register - Ch 1
0x17	CR23	JA1	R/W	Jitter Attenuator Control Register - Ch 1
0x18				
0x19				
0x1A	CR26	EM1	R/W	Error Counter MS Byte Ch 1
0x1B	CR27	EL1	R/W	Error Counter LS Byte
0x1C	CR28	EH1	R/W	Error Counter Holding Register
0x1D				
0x1E				
0x1F				
0x20				
Channel 2 Control Registers				
0x21	CR33	IER2	R/W	Source Level Interrupt Enable Register - Ch 2
0x22	CR34	ISR2	RUR	Source Level Interrupt Status Register - Ch 2
0x23	CR35	AS2	R/O	Alarm Status Register - Ch 2

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 27: XRT75R12 Command Register Address Map (Continued)

Address (Hex)	Command Register (Decimal)	Label	Type	Register Name
0x24	CR36	TC2	R/W	Transmit Control Register - Ch 2
0x25	CR37	RC2	R/W	Receive Control Register - Ch 2
0x26	CR38	CC2	R/W	Channel Control Register - Ch 2
0x27	CR39	JA2	R/W	Jitter Attenuator Control Register - Ch 2
0x28				
0x29				
0x2A	CR42	EM2	R/W	Error Counter MS Byte Ch 2
0x2B	CR43	EL2	R/W	Error Counter LS Byte
0x2C	CR44	EH2	R/W	Error Counter Holding Register
0x2D				
0x2E				
0x2F				
0x30				
Channel 3 Control Registers				
0x31	CR49	IER3	R/W	Source Level Interrupt Enable Register - Ch 3
0x32	CR50	ISR3	RUR	Source Level Interrupt Status Register - Ch 3
0x33	CR51	AS3	R/O	Alarm Status Register - Ch 3
0x34	CR52	TC3	R/W	Transmit Control Register - Ch 3
0x35	CR53	RC3	R/W	Receive Control Register - Ch 3
0x36	CR54	CC3	R/W	Channel Control Register - Ch 3
0x37	CR55	JA3	R/W	Jitter Attenuator Control Register - Ch 3
0x38				
0x39				
0x3A	CR58	EM3	R/W	Error Counter MS Byte Ch 3
0x3B	CR59	EL3	R/W	Error Counter LS Byte
0x3C	CR60	EH3	R/W	Error Counter Holding Register
0x3D				
0x3E				
0x3F				
0x40				
Channel 4 Control Registers				
0x41	CR65	IER4	R/W	Source Level Interrupt Enable Register - Ch 4
0x42	CR66	ISR4	RUR	Source Level Interrupt Status Register - Ch 4
0x43	CR67	AS4	R/O	Alarm Status Register - Ch 4
0x44	CR68	TC4	R/W	Transmit Control Register - Ch 4
0x45	CR69	RC4	R/W	Receive Control Register - Ch 4
0x46	CR70	CC4	R/W	Channel Control Register - Ch 4
0x47	CR71	JA4	R/W	Jitter Attenuator Control Register - Ch 4
0x48				
0x49				
0x4A	CR74	EM4	R/W	Error Counter MS Byte Ch 4

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 27: XRT75R12 Command Register Address Map (Continued)

Address (Hex)	Command Register (Decimal)	Label	Type	Register Name
0x4B	CR75	EL4	R/W	Error Counter LS Byte
0x4C	CR76	EH4	R/W	Error Counter Holding Register
0x4D				
0x4E				
0x4F				
0x50				
Channel 5 Control Registers				
0x51	CR81	IER5	R/W	Source Level Interrupt Enable Register - Ch 5
0x52	CR82	ISR5	RUR	Source Level Interrupt Status Register - Ch 5
0x53	CR83	AS5	R/O	Alarm Status Register - Ch 5
0x54	CR84	TC5	R/W	Transmit Control Register - Ch 5
0x55	CR85	RC5	R/W	Receive Control Register - Ch 5
0x56	CR86	CC5	R/W	Channel Control Register - Ch 5
0x57	CR87	JA5	R/W	Jitter Attenuator Control Register - Ch 5
0x58				
0x59				
0x5A	CR90	EM5	R/W	Error Counter MS Byte Ch 5
0x5B	CR91	EL5	R/W	Error Counter LS Byte
0x5C	CR92	EH5	R/W	Error Counter Holding Register
0x5D				
0x5E				
0x5F				
0x60	CR96	CIE	R/W	Channel 0-5 Interrupt Enable Flags
0x61	CR97	CIS	R/O	Channel 0-5 Interrupt Status Flags
0x62				
0x63				
0x64				
0x65				
0x66				
0x67				
0x68				
0x65				
0x69				
0x6A				
0x6B				
0x6C				
0x6D				
0x6E	CR110	PN	R/O	Device Part Number Register
0x6F	CR111	VN	R/O	Chip Revision Number Register
0x70				
0x71				

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 27: XRT75R12 Command Register Address Map (Continued)

Address (Hex)	Command Register (Decimal)	Label	Type	Register Name
0x72				
0x73				
0x74				
0x75				
0x76				
0x77				
0x78				
0x75				
0x79				
0x7A				
0x7B				
0x7C				
0x7D				
0x7E				
0x7F				
0x80	CR128	APST	R/W	APS Transmit Redundancy Control Register 6-11
Channel 6 Control Registers				
0x81	CR129	IER6	R/W	Source Level Interrupt Enable Register - Ch 6
0x82	CR130	ISR6	RUR	Source Level Interrupt Status Register - Ch 6
0x83	CR131	AS6	R/O	Alarm Status Register - Ch 6
0x84	CR132	TC6	R/W	Transmit Control Register - Ch 6
0x85	CR133	RC6	R/W	Receive Control Register - Ch 6
0x86	CR134	CC6	R/W	Channel Control Register - Ch 6
0x87	CR135	JA6	R/W	Jitter Attenuator Control Register - Ch 6
0x88	CR136	APSR	R/W	APS Receive Redundancy Control Register 6-11
0x89				
0x8A	CR138	EM6	R/W	Error Counter MS Byte Ch 6
0x8B	CR139	EL6	R/W	Error Counter LS Byte
0x8C	CR140	EH6	R/W	Error Counter Holding Register
0x8D				
0x8E				
0x8F				
0x90				
Channel 7 Control Registers				
0x91	CR145	IER7	R/W	Source Level Interrupt Enable Register - Ch 7
0x92	CR146	ISR7	RUR	Source Level Interrupt Status Register - Ch 7
0x93	CR147	AS7	R/O	Alarm Status Register - Ch 7
0x94	CR148	TC7	R/W	Transmit Control Register - Ch 7
0x95	CR149	RC7	R/W	Receive Control Register - Ch 7
0x96	CR150	CC7	R/W	Channel Control Register - Ch 7
0x97	CR151	JA7	R/W	Jitter Attenuator Control Register - Ch 7

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 27: XRT75R12 Command Register Address Map (Continued)

Address (Hex)	Command Register (Decimal)	Label	Type	Register Name
0x98				
0x99				
0x9A	CR154	EM7	R/W	Error Counter MS Byte Ch 7
0x9B	CR155	EL7	R/W	Error Counter LS Byte
0x9C	CR156	EH7	R/W	Error Counter Holding Register
0x9D				
0x9E				
0x9F				
0xA0				
Channel 8 Control Registers				
0xA1	CR161	IER8	R/W	Source Level Interrupt Enable Register - Ch 8
0xA2	CR162	ISR8	RUR	Source Level Interrupt Status Register - Ch 8
0xA3	CR163	AS8	R/O	Alarm Status Register - Ch 8
0xA4	CR164	TC8	R/W	Transmit Control Register - Ch 8
0xA5	CR165	RC8	R/W	Receive Control Register - Ch 8
0xA6	CR166	CC8	R/W	Channel Control Register - Ch 8
0xA7	CR167	JA8	R/W	Jitter Attenuator Control Register - Ch 8
0xA8				
0xA9				
0xAA	CR170	EM8	R/W	Error Counter MS Byte Ch 8
0xAB	CR171	EL8	R/W	Error Counter LS Byte
0xAC	CR172	EH8	R/W	Error Counter Holding Register
0xAD				
0xAE				
0xAF				
0xB0				
Channel 9 Control Registers				
0xB1	CR177	IER9	R/W	Source Level Interrupt Enable Register - Ch 9
0xB2	CR178	ISR9	RUR	Source Level Interrupt Status Register - Ch 9
0xB3	CR179	AS9	R/O	Alarm Status Register - Ch 9
0xB4	CR180	TC9	R/W	Transmit Control Register - Ch 9
0xB5	CR181	RC9	R/W	Receive Control Register - Ch 9
0xB6	CR182	CC9	R/W	Channel Control Register - Ch 9
0xB7	CR183	JA9	R/W	Jitter Attenuator Control Register - Ch 9
0xB8				
0xB9				
0xBA	CR186	EM9	R/W	Error Counter MS Byte Ch 9
0xBB	CR187	EL9	R/W	Error Counter LS Byte
0xBC	CR188	EH9	R/W	Error Counter Holding Register
0xBD				
0xBE				

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 27: XRT75R12 Command Register Address Map (Continued)

Address (Hex)	Command Register (Decimal)	Label	Type	Register Name
0xBF				
0xC0				
Channel 10 Control Registers				
0xC1	CR193	IER10	R/W	Source Level Interrupt Enable Register - Ch 10
0xC2	CR194	ISR10	RUR	Source Level Interrupt Status Register - Ch 10
0xC3	CR195	AS10	R/O	Alarm Status Register - Ch 10
0xC4	CR196	TC10	R/W	Transmit Control Register - Ch 10
0xC5	CR197	RC10	R/W	Receive Control Register - Ch 10
0xC6	CR198	CC10	R/W	Channel Control Register - Ch 10
0xC7	CR199	JA10	R/W	Jitter Attenuator Control Register - Ch 10
0xC8				
0xC9				
0xCA	CR202	EM10	R/W	Error Counter MS Byte Ch 10
0xCB	CR203	EL10	R/W	Error Counter LS Byte
0xCC	CR204	EH10	R/W	Error Counter Holding Register
0xCD				
0xCE				
0xCF				
0xD0				
Channel 11 Control Registers				
0xD1	CR209	IER11	R/W	Source Level Interrupt Enable Register - Ch 11
0xD2	CR210	ISR11	RUR	Source Level Interrupt Status Register - Ch 11
0xD3	CR211	AS11	R/O	Alarm Status Register - Ch 11
0xD4	CR212	TC11	R/W	Transmit Control Register - Ch 11
0xD5	CR213	RC11	R/W	Receive Control Register - Ch 11
0xD6	CR214	CC11	R/W	Channel Control Register - Ch 11
0xD7	CR215	JA11	R/W	Jitter Attenuator Control Register - Ch 11
0xD8				
0xD9				
0xDA	CR218	EM11	R/W	Error Counter MS Byte Ch 11
0xDB	CR219	EL11	R/W	Error Counter LS Byte
0xDC	CR220	EH11	R/W	Error Counter Holding Register
0xDD				
0xDE				
0xDF				
0xE0	CR224	CIE	R/W	Channel 6-11 Interrupt Enable Flags
0xE1	CR225	CIS	R/O	Channel 6-11 Interrupt Status Flags
0xE2				
0xE3				
0xE4				
0xE5				

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 27: XRT75R12 Command Register Address Map (Continued)

Address (Hex)	Command Register (Decimal)	Label	Type	Register Name
0xE6				
0xE7				
0xE8				
0xE5				
0xE9				
0xEA				
0xEB				
0xEC				
0xED				
0xEE				
0xEF				
0xF0				
0xF1				
0xF2				
0xF3				
0xF4				
0xF5				
0xF6				
0xF7				
0xF8				
0xF5				
0xF9				
0xFA				
0xFB				
0xFC				
0xFD				
0xFE				
0xFF				

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

9.4 Global Chip-Level Registers

The register set within the XRT75R12 contains ten global or chip-level registers. These registers control operations in more than one channel or apply to the complete chip. This section will present detailed information on the global registers.

Table 28: Global Register List and Address Locations

Address	Command Register	Label	Type	Register Name
0x00	CR0	APST	R/W	APS Transmit Redundancy Control Register 0-5
0x08	CR8	APSR	R/W	APS Receive Redundancy Control Register 0-5
0x80	CR128	APST	R/W	APS Transmit Redundancy Control Register 6-11
0x88	CR136	APSR	R/W	APS Receive Redundancy Control Register 6-11
0x60	CR96	CIE	R/W	Channel 0-5 Interrupt Enable Flags
0x61	CR97	CIS	R/O	Channel 0-5 Interrupt Status Flags
0xE0	CR224	CIE	R/W	Channel 6-11 Interrupt Enable Flags
0xE1	CR225	CIS	R/O	Channel 6-11 Interrupt Status Flags
0x6E	CR110	PN	ROM	Device Part Number Register
0x6F	CR111	VN	ROM	Chip Revision or Version Number Register

9.4.1 Global Register Descriptions

Table 29: APS / Redundancy Transmit Control Register - CR0 (Address Location 0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		TxON Ch5	TxON Ch4	TxON Ch3	TxON Ch2	TxON Ch1	TxON Ch0
		R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Name	Type	Description
7, 6	Reserved		
5	TxON Ch 5	R/W	**Transmit Section On - Channel n** This read and write bit-field is used to turn on or turn off the transmit driver associated with channel n. If the user turns on the transmit driver, then channel n will transmit DS3, E3 or STS-1 pulses on the line via the TTIP_n and TRING_n output pins. Conversely, if the user turns off the transmit driver, then the TTIP_n and TRING_n output pins will be tri-stated. ■ 0 - Shuts off the transmit driver associated with channel n and tri-states the TTIP_n and TRING_ n output pins. ■ 1 - Turns on the transmit driver associated with channel n. **Note:** The master TxON control pin (pin # P4) **must** be in a high state (logic 1) for this operation to turn on any channel.
4	TxON Ch 4	R/W	
3	TxON Ch 3	R/W	
2	TxON Ch 2	R/W	
1	TxON Ch 1	R/W	
0	TxON Ch 0	R/W	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 30: APS / Redundancy Receive Control Register - CR8 (Address Location 0x08)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RxON Ch5	RxON Ch4	RxON Ch3	RxON Ch2	RxON Ch1	RxON Ch0
		R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Name	Type	Description
7, 6	Reserved		
5	RxON Ch 5	R/W	**Receive Section On - Channel n** This read and write bit-field is used to turn on or turn off the receiver associated with channel n on a per channel basis. If the user turns on the receiver, then channel n will receive DS3, E3 or STS-1 pulses on the line via the RTIP_n and RRING_n input pins. Conversely, if the user turns off the receiver driver (for channel n), then the RTIP_n and RRING_n input pins will be in a high impedance state. ■ 0 - Shuts off the receiver driver associated with channel n and puts the RTIP_n and RRING_ n input pins in a high impedance state. ■ 1 - Turns on the receive driver associated with channel n.
4	RxON Ch 4	R/W	
3	RxON Ch 3	R/W	
2	RxON Ch 2	R/W	
1	RxON Ch 1	R/W	
0	RxON Ch 0	R/W	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 31: APS / Redundancy Transmit Control Register - CR128 (Address Location = 0x80)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		TxON Ch11	TxON Ch10	TxON Ch9	TxON Ch8	TxON Ch7	TxON Ch6
		R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Name	Type	Description
7, 6	Reserved		
5	TxON Ch 11	R/W	**Transmit Section On - Channel n** This read and write bit-field is used to turn on or turn off the transmit driver associated with channel n. If the user turns on the transmit driver, then channel n will transmit DS3, E3 or STS-1 pulses on the line via the TTIP_n and TRING_n output pins. Conversely, if the user turns off the transmit driver, then the TTIP_n and TRING_n output pins will be tri-stated. ■ 0 - Shuts off the transmit driver associated with channel n and tri-states the TTIP_n and TRING_ n output pins. ■ 1 - Turns on the transmit driver associated with channel n. **Note:** The master TxON control pin (pin # P4) **must** be in a high state (logic 1) for this operation to turn on any channel.
4	TxON Ch 10	R/W	
3	TxON Ch 9	R/W	
2	TxON Ch 8	R/W	
1	TxON Ch 7	R/W	
0	TxON Ch 6	R/W	

Table 32: APS / Redundancy Receive Control Register - CR136 (Address Location 0x88)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RxON Ch11	RxON Ch10	RxON Ch9	RxON Ch8	RxON Ch7	RxON Ch6
		R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Name	Type	Description
7, 6	Reserved		
5	RxON Ch 11	R/W	**Receive Section On - Channel n** This read and write bit-field is used to turn on or turn off the receiver associated with channel n on a per channel basis. If the user turns on the receiver, then channel n will receive DS3, E3 or STS-1 pulses on the line via the RTIP_n and RRING_n input pins. Conversely, if the user turns off the receiver driver (for channel n), then the RTIP_n and RRING_n input pins will be in a high impedance state. ■ 0 - Shuts off the receiver driver associated with channel n and puts the RTIP_n and RRING_ n input pins in a high impedance state. ■ 1 - Turns on the receive driver associated with channel n.
4	RxON Ch 10	R/W	
3	RxON Ch 9	R/W	
2	RxON Ch 8	R/W	
1	RxON Ch 7	R/W	
0	RxON Ch 6	R/W	

Table 33: Channel Level Interrupt Enable Register - CR96 (Address Location = 0x60)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Channel 5 Interrupt Enable	Channel 4 Interrupt Enable	Channel 3 Interrupt Enable	Channel 2 Interrupt Enable	Channel 1 Interrupt Enable	Channel 0 Interrupt Enable
		R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Name	Type	Description
7, 6	Reserved		
5	Channel 5 Interrupt Enable	R/W	**Channel n Interrupt Enable Bit:** This read and write bit is used to: ■ To enable channel n for interrupt generation at the channel level. ■ To disable all interrupts associated with channel n within the XRT75R12. This is a "master" enable bit for **each** channel. This bit allows control on a per channel basis to signal the host for selected error conditions. If a bit is cleared, no interrupts from that channel will be sent to the host via the $\overline{INT}$ pin. If the bit is set (logic 1), any generated interrupt in channel n that has been enabled in the Interrupt Enable Register (IERn) for the channel will activate the $\overline{INT}$ pin to the host. ■ 0 - Disables all channel n related Interrupts. ■ 1 - Enables channel n-related interrupts. The user **must enable** individual channel n related interrupts at the source level, before they can generate an interrupt.
4	Channel 4 Interrupt Enable	R/W	
3	Channel 3 Interrupt Enable	R/W	
2	Channel 2 Interrupt Enable	R/W	
1	Channel 1 Interrupt Enable	R/W	
0	Channel 0 Interrupt Enable	R/W	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OPS).

Table 34: Channel Level Interrupt Status Register - CR97 (Address Location = 0x61)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Channel 5 Interrupt Status	Channel 4 Interrupt Status	Channel 3 Interrupt Status	Channel 2 Interrupt Status	Channel 1 Interrupt Status	Channel 0 Interrupt Status
		R/O	R/O	R/O	R/O	R/O	R/O

Bit Number	Name	Type	Description
7, 6	Reserved		
5	Channel 5 Interrupt Status	R/O	**Channel n Interrupt Status Bit:** This read-only bit-field indicates whether the XRT75R12 has a pending channel n related interrupt that is awaiting service. The first six channels are serviced through this location and the other six at address 0xE1. These two registers are used by the host to identify the source channel of an active interrupt. ■ 0 - Indicates that there is NO channel n-related Interrupt awaiting service. ■ 1 - Indicates that there is at least one channel n-related Interrupt awaiting service. In this case, the user's interrupt service routine should be written such that the microprocessor will now proceed to read out the contents of the Source-Level Interrupt Status Register — channel n (address locations = 0xn2) to determine the exact source of the interrupt request. **Note:** Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit that corresponds to the interrupt request channel.
4	Channel 4 Interrupt Status	R/O	
3	Channel 3 Interrupt Status	R/O	
2	Channel 2 Interrupt Status	R/O	
1	Channel 1 Interrupt Status	R/O	
0	Channel 0 Interrupt Status	R/O	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 35: Channel Level Interrupt Enable Register - CR224 (Address Location = 0xE0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Channel 11 Interrupt Enable	Channel 10 Interrupt Enable	Channel 9 Interrupt Enable	Channel 8 Interrupt Enable	Channel 7 Interrupt Enable	Channel 6 Interrupt Enable
		R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	Name	Type	Description
7, 6	Reserved		
5	Channel 11 Interrupt Enable	R/W	**Channel n Interrupt Enable Bit:** This read and write bit is used to: ■ To enable channel n for interrupt generation at the channel level. ■ To disable all interrupts associated with channel n within the XRT75R12. This is a "master" enable bit for **each** channel. This bit allows control on a per channel basis to signal the host for selected error conditions. If a bit is cleared, no interrupts from that channel will be sent to the host via the $\overline{INT}$ pin. If the bit is set (logic 1), any generated interrupt in channel n that has been enabled in the Interrupt Enable Register (IERn) for the channel will activate the $\overline{INT}$ pin to the host. ■ 0 - Disables all channel n related Interrupts. ■ 1 - Enables channel n-related interrupts. The user **must enable** individual channel n related interrupts at the source level, before they can generate an interrupt.
4	Channel 10 Interrupt Enable	R/W	
3	Channel 9 Interrupt Enable	R/W	
2	Channel 8 Interrupt Enable	R/W	
1	Channel 7 Interrupt Enable	R/W	
0	Channel 6 Interrupt Enable	R/W	

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 36: Channel Level Interrupt Status Register - CR225 (Address Location = 0xE1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Channel 11 Interrupt Status	Channel 10 Interrupt Status	Channel 9 Interrupt Status	Channel 8 Interrupt Status	Channel 7 Interrupt Status	Channel 6 Interrupt Status
		R/O	R/O	R/O	R/O	R/O	R/O

Bit Number	Name	Type	Description
7, 6	Reserved		
5	Channel 11 Interrupt Status	R/O	**Channel n Interrupt Status Bit:** This read-only bit-field indicates whether the XRT75R12 has a pending channel n related interrupt that is awaiting service. The last six channels are serviced through this location and the other six at address 0x61. These two registers are used by the host to identify the source channel of an active interrupt. ■ 0 - Indicates that there is NO channel n-related Interrupt awaiting service. ■ 1 - Indicates that there is at least one channel n-related Interrupt awaiting service. In this case, the user's interrupt service routine should be written such that the microprocessor will now proceed to read out the contents of the Source-Level Interrupt Status Register — channel n (address locations = 0xn2) to determine the exact source of the interrupt request. **Note:** Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit that corresponds to the interrupt request channel.
4	Channel 10 Interrupt Status	R/O	
3	Channel 9 Interrupt Status	R/O	
2	Channel 8 Interrupt Status	R/O	
1	Channel 7 Interrupt Status	R/O	
0	Channel 6 Interrupt Status	R/O	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 37: Device or Part Number Register - CR110 (Address Location = 0x6E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Part Number ID Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	0	0	0

Bit Number	Name	Type	Default Value	Description
7 - 0	Part Number ID Value	R/O	0x78	**Part Number ID Value:** This read-only register contains a unique value for the XRT75R12. This value will always be 0x78 (0111 1000).

Table 38: Chip Revision Number Register - CR111 (Address Location = 0x6F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Chip Revision Number Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	X	X	X	X

Bit Number	Name	Type	Default Value	Description
7 - 0	Chip Revision Number Value	R/O	0x0#	**Chip Revision Number Value:** This read-only register contains a value that represents the current revision of this XRT75R12. This revision number will always be in the form of "0x0#", where "#" is a hexadecimal value that specifies the current revision of the chip. For example, the very first revision of this chip will contain the value "0x01".

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

9.5 Per-Channel Registers

The XRT75R12 consists of 120 per-channel registers (12 channels and 10 registers per channel). Table 39 presents the overall Register Map with the per-channel registers unshaded.

9.5.1 Per-Channel Register Descriptions

Table 39: XRT75R12 Register Map Showing Interrupt Enable Registers (IER_n)

Address Location	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

Table 40: Source-Level Interrupt Enable Register - Channel n Address Location = 0xm1 (n = [0:11] & m = 0-5, 8-D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				Change of FL Condition Interrupt Enable Ch n	Change of LOL Condition Interrupt Enable Ch n	Change of LOS Condition Interrupt Enable Ch n	Change of DMO Condition Interrupt Enable Ch n
				R/W	R/W	R/W	R/W

Bit Number	Name	Type	Description
7 - 4	Reserved	R/O	
3	Change of FL Condition Interrupt Enable - Ch n	R/W	**Change of FL (FIFO Limit Alarm) Condition Interrupt Enable - Ch n:** This read and write bit-field is used to enable or disable the change of the FIFO Limit Alarm condition interrupt. If the user enables this interrupt, the XRT75R12 will generate an interrupt if any of the following events occur: ▪ Whenever the jitter attenuator (within channel n) declares the FL (FIFO Limit Alarm) condition. ▪ Whenever the jitter attenuator (within channel n) clears the FL (FIFO Limit Alarm) condition. 0 - Disables the change in FL condition interrupt. 1 - Enables the change in FL condition interrupt.
2	Change of LOL Condition Interrupt Enable	R/W	**Change of Receive LOL (Loss of Lock) Condition Interrupt Enable - Ch n:** This read and write bit-field is used to enable or disable the change of the receive LOL condition interrupt. If the user enables this interrupt, then the XRT75R12 will generate an interrupt any time any of the following events occur: ▪ Whenever the receive section (within channel n) declares the Loss of Lock condition. ▪ Whenever the receive section (within channel n) clears the Loss of Lock condition. 0 - Disables the change in receive LOL condition interrupt. 1 - Enables the change in receive LOL condition interrupt.
1	Change of LOS Condition Interrupt Enable	R/W	**Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable - Ch 0:** This read and write bit-field is used to enable or disable the change of the receive LOS defect condition interrupt. If the user enables this interrupt, then the XRT75R12 will generate an interrupt any time any of the following events occur: ▪ Whenever the receive section (within channel n) declares the LOS defect condition. ▪ Whenever the receive section (within channel n) clears the LOS defect condition. 0 - Disables the change in the LOS defect condition interrupt. 1 - Enables the change in the LOS defect condition interrupt.
0	Change of DMO Condition Interrupt Enable	R/W	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable - Ch n**: This read and write bit-field is used to enable or disable the change of transmit DMO condition interrupt. If the user enables this interrupt, then the XRT75R12 will generate an interrupt any time any of the following events occur: ▪ Whenever the transmit section toggles the DMO output pin (or bit-field) to "1". ▪ Whenever the transmit section toggles the DMO output pin (or bit-field) to "0". 0 - Disables the change in the DMO condition interrupt. 1 - Enables the change in the DMO condition interrupt.

The product (or product) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

Table 41: XRT75R12 Register MAP Showing Interrupt Status Registers (ISR_n)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				Change of FL Condition Interrupt Status Ch n	Change of LOL Condition Interrupt Status Ch n	Change of LOS Condition Interrupt Status Ch n	Change of DMO Condition Interrupt Status Ch n
				RUR	RUR	RUR	RUR

Table 42: Source Level Interrupt Status Registers (ISR_n) - Channel n Address Location = 0xm2 (n = [0:11] & m = 05, 8-D)

Bit Number	Name	Type	Description
7 - 4	Reserved		
3	Change of FL Condition Interrupt Status	RUR	**Change of FL (FIFO Limit Alarm) Condition Interrupt Status - Ch n:** This reset-upon-read bit-field indicates whether or not the change of FL condition interrupt (for channel n) has occurred since the last read of this register. ■ 0 - Indicates that the change of FL condition interrupt has NOT occurred since the last read of this register. ■ 1 - Indicates that the change of FL condition interrupt has occurred since the last read of this register. **Note:** The user can determine the current state of the FIFO Alarm condition by reading out the contents of bit 3 (FL Alarm declared) within the Alarm Status Register (n).
2	Change of LOL Condition Interrupt Status	RUR	**Change of Receive LOL (Loss of Lock) Condition Interrupt Status - Ch n:** This reset-upon-read bit-field indicates whether or not the change of receive LOL condition interrupt (for channel n) has occurred since the last read of this register. ■ 0 - Indicates that the change of receive LOL condition interrupt has NOT occurred since the last read of this register. ■ 1 - Indicates that the change of receive LOL condition interrupt has occurred since the last read of this register. **Note:** The user can determine the current state of the receive LOL defect condition by reading out the contents of bit 2 (receive LOL defect declared) within the Alarm Status Register (n).
1	Change of LOS Condition Interrupt Status	RUR	**Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status: Ch n** This reset-upon-read bit-field indicates whether or not the change of the receive LOS defect condition interrupt (for channel n) has occurred since the last read of this register. ■ 0 - Indicates that the change of the receive LOS defect condition interrupt has NOT occurred since the last read of this register. ■ 1 - Indicates that the change of the receive LOS defect condition interrupt has occurred since the last read of this register. **Note:** The user can determine the current state of the receive LOS defect condition by reading out the contents of bit 1 (receive LOS defect declared) within the Alarm Status Register (n).

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Table 42: Source Level Interrupt Status Registers (ISR_n) - Channel n Address Location = 0xm2 (n = [0:11] & m = 05, 8-D)

Bit Number	Name	Type	Description
0	Change of DMO Condition Interrupt Status	RUR	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status - Ch n:** This reset-upon-read bit-field indicates whether or not the change of the transmit DMO condition interrupt (for channel n) has occurred since the last read of this register. ■ 0 - Indicates that the change of the transmit DMO condition interrupt has NOT occurred since the last read of this register. ■ 1 - Indicates that the change of the transmit DMO condition interrupt has occurred since the last read of this register. **Note:** The user can determine the current state of the transmit DMO condition by reading out the contents of bit 0 (transmit DMO condition) within the Alarm Status Register (n).

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Table 43: XRT75R12 Register Map Showing Alarm Status Registers (AS_n)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Loss of PRBS Pattern Sync	Digital LOS Defect Declared	Analog LOS Defect Declared	FL (FIFO Limit) Alarm Declared	Receive LOL Defect Declared	Receive LOS Defect Declared	Transmit DMO Condition
	R/O	R/O	R/O	R/O	R/O	R/O	R/O

Table 44: Alarm Status Registers (AS_n) - Channel n Address Location = 0xm3 (n=[0:11] & m= 0-5, 8-D)

Bit Number	Name	Type	Description
7	Reserved		
6	Loss of PRBS Pattern Lock	R/O	**Loss of PRBS Pattern Lock Indicator:** This read-only bit-field indicates whether or not the PRBS receiver (within the receive section of channel n) is declaring PRBS Lock within the incoming PRBS pattern. If the PRBS receiver detects a very large number of bit-errors within its incoming data stream, then it will declare the Loss of PRBS Lock condition. Conversely, if the PRBS receiver were to detect its pre-determined PRBS pattern with the incoming DS3, E3 or STS-1 data stream, (with little or no bit errors) then the PRBS receiver will clear the Loss of PRBS Lock condition. ■ 0 - Indicates that the PRBS receiver is currently declaring the PRBS Lock condition within the incoming DS3, E3 or STS-1 data stream. ■ 1 - Indicates that the PRBS receiver is currently declaring the Loss of PRBS Lock condition within the incoming DS3, E3 or STS-1 data stream. **Note:** This register bit is only valid if all of the following are true: **a.** The PRBS generator block (within the transmit section of the chip) is enabled. **b.** The PRBS receiver is enabled. **c.** The PRBS pattern (that is generated by the PRBS generator) is somehow looped back into the receive path (via the line-side), and in turn routed to the receive input of the PRBS receiver.
5	Digital LOS Defect Declared	R/O	**Digital LOS Defect Declared:** This read-only bit-field indicates whether or not the digital LOS (Loss of Signal) detector is declaring the LOS defect condition. For DS3 and STS-1 applications, the digital LOS detector will declare the LOS defect condition whenever it detects an absence of pulses (within the incoming DS3 or STS-1 data stream) for 160 consecutive bit-periods. Further, (again for DS3 and STS-1 applications) the digital LOS detector will clear the LOS defect condition whenever it determines that the pulse density (within the incoming DS3 or STS-1 signal) is at least 33%. ■ 0 - Indicates that the digital LOS detector is NOT declaring the LOS defect condition. ■ 1 - Indicates that the digital LOS detector is currently declaring the LOS defect condition. **Notes:** **1.** LOS detection (within each channel of the XRT75R12) is performed by both an analog LOS detector and a digital LOS detector. The LOS state of a given channel is simply a wired-OR of the LOS defect declared states of these two detectors. **2.** The current LOS defect condition (for the channel) can be determined by reading out the contents of bit 1 (receive LOS defect declared) within this register.

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Table 44: (Continued) Alarm Status Registers (AS_n) - Channel n Address Location = 0xm3 (n=[0:11] & m= 0-5, 8-D)

Bit Number	Name	Type	Description
4	Analog LOS Defect Declared	R/O	**Analog LOS Defect Declared:** This read-only bit-field indicates whether or not the analog LOS (Loss of Signal) detector is declaring the LOS defect condition. For DS3 and STS-1 applications, the analog LOS detector will declare the LOS defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3 or STS-1 line signal) drops below a certain analog LOS defect declaration threshold level. Conversely, (again for DS3 and STS-1 applications) the analog LOS Detector will clear the LOS defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3 or STS-1 line signal) has risen above a certain analog LOS defect clearance threshold level. It should be noted that, in order to prevent "chattering" within the analog LOS detector output, there is some built-in hysteresis between the analog LOS defect declaration and the analog LOS defect clearance threshold levels. ■ 0 - Indicates that the analog LOS detector is NOT declaring the LOS defect condition. ■ 1 - Indicates that the analog LOS Detector is currently declaring the LOS defect condition. **Notes:** 1. LOS detection (within each channel of the XRT75R12) is performed by both an analog LOS detector and a digital LOS detector. The LOS state of a given channel is simply a wired-OR of the LOS defect declared states of these two detectors. 2. The current LOS defect condition (for the channel) can be determined by reading out the contents of bit 1 (receive LOS defect declared) within this register.
3	FL Alarm Declared	R/O	**FL (FIFO Limit) Alarm Declared:** This read-only bit-field indicates whether or not the jitter attenuator block (within channel_n) is currently declaring the FIFO Limit Alarm. The jitter attenuator block will declare the FIFO Limit Alarm anytime the jitter attenuator FIFO comes within two bit-periods of either overflowing or under-running. Conversely, the jitter attenuator block will clear the FIFO Limit Alarm anytime the jitter attenuator FIFO is no longer within two bit-periods of either overflowing or under-running. Typically, this alarm will only be declared whenever there is a very serious problem with timing or jitter in the system. ■ 0 - Indicates that the jitter attenuator block (within channel_n) is NOT currently declaring the FIFO Limit Alarm condition. ■ 1 - Indicates that the Jitter Attenuator block (within channel_n) is currently declaring the FIFO Limit Alarm condition. **Note:** This bit-field is only active if the jitter attenuator (within channel_n) has been enabled.

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Table 44: (Continued) Alarm Status Registers (AS_n) - Channel n Address Location = 0xm3 (n=[0:11] & m= 0-5, 8-D)

Bit Number	Name	Type	Description
2	Receive LOL Condition Declared	R/O	**Receive LOL (Loss of Lock) Condition Declared:** This read-only bit-field indicates whether or not the receive section (within channel_n) is currently declaring the LOL (Loss of Lock) condition. The receive section (of channel_n) will declare the LOL condition, if the frequency of the recovered clock signal differs from that of the reference clock programmed for that channel (from the appropriate oscillator or the SFM clock synthesizer, if in that mode) by 0.5% (or 5000ppm) or more. ■ 0 - Indicates that the receive section of channel_n is NOT currently declaring the LOL condition. ■ 1 - Indicates that the receive section of channel_n is currently declaring the LOL condition and the recovered clock differs by more than 0.5%.
1	Receive LOS Defect Condition Declared	R/O	**Receive LOS (Loss of Signal) Defect Condition Declared:** This read-only bit-field indicates whether or not the receive section (within channel_n) is currently declaring the LOS defect condition. The receive section (of channel_n) will declare the LOS defect condition, if any one of the following conditions is met: ■ If the digital LOS detector declares the LOS defect condition (for DS3 or STS-1 applications) ■ If the analog LOS detector declares the LOS defect condition (for DS3 or STS-1 applications) ■ If the ITU-T G.775 LOS detector declares the LOS defect condition (for E3 applications). 0 - Indicates that the receive section of channel_n is NOT currently declaring the LOS defect condition. 1 - Indicates that the receive section of channel_n is currently declaring the LOS defect condition.
0	Transmit DMO Condition Declared	R/O	**Transmit DMO (Drive Monitor Output) Condition Declared:** This read-only bit-field indicates whether or not the transmit section of channel_n is currently declaring the DMO alarm condition. As configured, the transmit section will either internally (via the TTIP_n and TRING_n) or externally (via the MTIP_n and MRING_n) check the transmit output DS3, E3, or STS-1 line signal for bipolar pulses. If the transmit section were to detect no bipolar for 128 consecutive bit-periods, then it will declare the transmit DMO alarm condition. This particular alarm can be used to check for fault conditions on the transmit output line signal path. The transmit section will clear the transmit DMO alarm condition upon detecting bipolar activity on the transmit output line signal. ■ 0 - Indicates that the transmit section of channel_n is NOT currently declaring the transmit DMO alarm condition. ■ 1 - Indicates that the transmit section of channel_n is currently declaring the transmit DMO alarm condition.

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Table 45: XRT75R12 Register Map Showing Transmit Control Registers (TC_n)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Internal Transmit Drive Monitor	Insert PRBS Error	Reserved	TAOS	TxCLKINV	TxLEV
		R/W	R/W		R/W	R/W	R/W

Table 46: Transmit Control Registers (TC_n) - Channel n Address Location=0xm4 (n=[0:11] & m=0-5,8-D)

Bit Number	Name	Type	Description
7 - 6	Reserved		
5	Internal Transmit Drive Monitor Enable	R/W	**Internal Transmit Drive Monitor Enable - Channel_n:** This read and write bit-field is used to configure the transmit section of channel_n to either internally or externally monitor the TTIP_n and TRING_n output pins for bipolar pulses, in order to determine whether to declare the transmit DMO alarm condition. If the user configures the transmit section to externally monitor the TTIP_n and TRING_n output pins (for bipolar pulses), then the user must connect the MTIP_n and MRING_n input pins to their corresponding TTIP_n and TRING_n output pins (via a 270Ω series resistor). If the user configures the transmit section to internally monitor the TTIP_n and TRING_n output pins (for bipolar pulses), the user does NOT need to connect the MTIP_n and MRING_n input pins. This monitoring will be performed internally at the TTIP_n and TRING_n pads. ■ 0 - Configures the transmit Drive Monitor to externally monitor the TTIP_n and TRING_n output pins for bipolar pulses. ■ 1 - Configures the transmit Drive Monitor to internally monitor the TTIP_n and TRING_n output pins for bipolar pulses.
4	Insert PRBS Error	R/W	**Insert PRBS Error - Channel_n:** A "0 to 1" transition within this bit-field causes the PRBS generator (within the transmit section of channel_n) to generate a single bit error within the outbound PRBS pattern-stream. **Note:** 1. This bit-field is only active if the PRBS Generator and receiver have been enabled within the corresponding channel. 2. After writing the "1" into this register, the user must execute a write operation to clear this particular register bit to "0" in order to facilitate the next "0 to 1" transition in this bit-field.
3	Reserved		

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Table 46: (Continued)Transmit Control Registers (TC_n) - Channel n Address Location=0xm4 (n=[0:11] & m=0-5,8-D)

Bit Number	Name	Type	Description
2	TAOS	R/W	**Transmit All OneS Pattern - Channel_n:** This read and write bit-field is used to command the transmit section of channel_n to generate and transmit an unframed, all ones pattern via the DS3, E3 or STS-1 line signal (to the remote terminal equipment). Whenever the user implements this configuration setting, the transmit section will ignore the data that it is accepting from the system-side equipment and output the "All Ones" pattern. ■ 0 - Configures the transmit section to transmit the data that it accepts from the system-side interface. ■ 1 - Configures the transmit section to generate and transmit the unframed, all ones pattern.
1	TxCLKINV	R/W	**Transmit Clock Invert Select - Channel_n:** This read and write bit-field is used to select the edge of the TxCLK_n input that the transmit section of channel_n will use to sample the TxPOS_n and TxNEG_n input pins, as described below: ■ 0 - Configures the transmit section (within the corresponding channel) to sample the TxPOS_n and TxNEG_n input pins upon the falling edge of TxCLK_n. ■ 1 - Configures the transmit section (within the corresponding channel) to sample the TxPOS_n and TxNEG_n input pins upon the rising edge of TxCLK_n. **Note:** This is done on a per-channel basis.
0	TxLEV	R/W	**Transmit Line Build-Out Select - Channel_n:** This read and write bit-field is used to enable or disable the transmit line build-out (for example, pulse-shaping) circuit within the corresponding channel. The user should set this bit-field to either "0" or to "1" based upon the following guidelines: ■ 0 - If the cable length between the transmit output (of the corresponding channel) and the DSX-3 or STSX-1 location is 225 feet or less. ■ 1 - If the cable length between the transmit output (of the corresponding channel) and the DSX-3 or STSX-1 location is more than 225 feet. The user must follow these guidelines in order to insure that the transmit section (of channel_n) will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE, or an STS-1 pulse that complies with the Pulse Template requirements per Telcordia GR-253-CORE. **Note:** This bit-field is ignored if the channel has been configured to operate in the E3 Mode.

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Table 47: XRT75R12 Register Map Showing Receive Control Registers (RC_n)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Disable DLOS Detector	Disable ALOS Detector	RxCLKINV	LOSMUT Enable	Receive Monitor Mode Enable	Receive Equalizer Enable
		R/W	R/W	R/W	R/W	R/W	R/W

Table 48: Receive Control Registers (RC_n) - Channel n Address Location=0xm5 (n=[0:11] & m=0-5, 8-D)

Bit Number	Name	Type	Description
7 - 6	Reserved		
5	Disable DLOS Detector	R/W	**Disable Digital LOS Detector - Channel_n:** This read and write bit-field is used to enable or disable the digital LOS (Loss of Signal) detector within channel_n, as described below: ■ 0 - Enables the digital LOS detector within channel_n. ■ 1 - Disables the digital LOS detector within channel_n. **Note:** This bit-field is only active if channel_n has been configured to operate in the DS3 or STS-1 modes.
4	Disable ALOS Detector	R/W	**Disable Analog LOS Detector - Channel_n:** This read and write bit-field is used to either enable or disable the analog LOS (Loss of Signal) detector within channel_n, as described below: ■ 0 - Enables the analog LOS detector within channel_n. ■ 1 - disables the analog LOS detector within channel_n. **Note:** This bit-field is only active if channel_n has been configured to operate in the DS3 or STS-1 modes.
3	RxCLKINV	R/W	**Receive Clock Invert Select - Channel_n:** This read and write bit-field is used to select the edge of the RxCLK_n output that the receive section of channel_n will use to output the recovered data via the RxPOS_n and RxNEG_n output pins, as described below: ■ 0 - Configures the receive section (within the corresponding channel) to output the recovered data via the RxPOS_n and RxNEG_n output pins upon the rising edge of RCLK_n. ■ 1 - Configures the receive section (within the corresponding channel) to output the recovered data via the RxPOS_n and RxNEG_n output pins upon the falling edge of RCLK_n.
2	LOSMUT Enable	R/W	**Muting upon LOS Enable - Channel_n:** This read and write bit-field is used to configure the receive section (within channel_n) to automatically pull their corresponding recovered data output pins (e.g., RxPOS_n and RxNEG_n) to GND for the duration that the receive section declares the LOS defect condition. In other words, this feature (if enabled) will cause the receive channel to automatically mute the recovered data anytime the receive section declares the LOS defect condition. ■ 0 - Disables the muting upon the LOS feature. In this setting, the receive section will NOT automatically mute the recovered data whenever it is declaring the LOS defect condition. ■ 1 - Enables the muting upon the LOS feature. In this setting, the receive section will automatically mute the recovered data whenever it is declaring the LOS defect condition.

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Table 48: Receive Control Registers (RC_n) - Channel n Address Location=0xm5 (n=[0:11] & m=0-5, 8-D)

Bit Number	Name	Type	Description
1	Receive Monitor Mode Enable	R/W	**Receive Monitor Mode Enable - Channel_n:** This read and write bit-field is used to configure the receive section of channel_n to operate in the Receive Monitor Mode. If the user configures the receive section to operate in the Receive Monitor Mode, then it will be able to receive a nominal DSX-3 or STSX-1 signal that has been attenuated by 20dB of flat loss along with 6dB of cable loss, in an error-free manner. However, internal LOS circuitry is suppressed and LOS will never assert nor will LOS be declared when operating under this mode. ■ 0 - Configures the corresponding channel to operate in the normal mode. ■ 1 - Configure the corresponding channel to operate in the Receive Monitor Mode.
0	Receive Equalizer Enable	R/W	**Receive Equalizer Enable - Channel_n:** This read and write register bit is used to enable or disable the receive equalizer block within the receive section of channel_n, as listed below: ■ 0 - Disables the receive equalizer within the corresponding channel. ■ 1 - Enables the receive equalizer within the corresponding channel. **Note:** For virtually all applications, it is recommended that the user set this bit-field to "1" (for all channels) and enable the receive equalizer.

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Table 49: XRT75R12 Register Map Showing Channel Control Registers (CC_n)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1 / $\overline{DS3}$_n	SR / $\overline{DR}$_n
		R/W	R/W	R/W	R/W	R/W	R/W

Table 50: Channel Control Registers (CC_n) - Channel n Address Location=0xm6 (n=[0:11] & m=0-5, 8-D)

Bit Number	Name	Type	Description
7 - 6	Reserved		
5	PRBS Enable	R/W	**PRBS Generator and Receiver Enable - Channel_n:** This read and write bit-field is used to enable or disable the PRBS Generator and Receiver within a given channel of the XRT75R12. If the user enables the PRBS Generator and Receiver, then the following will happen: 1. The PRBS Generator (which resides within the transmit section of the channel) will begin to generate an unframed, 2^{15}-1 PRBS pattern (for DS3 and STS-1 applications) and an unframed, 2^{23}-1 PRBS pattern (for E3 applications). 2. The PRBS Receiver (which resides within the receive section of the channel) will now be enabled and will begin to search the incoming data for the above-mentioned PRBS patterns. ■ 0 - Disables both the PRBS Generator and PRBS Receiver within the corresponding channel. ■ 1 - Enables both the PRBS Generator and PRBS Receiver within the corresponding channel. **Notes:** 1. To check and monitor PRBS bit errors, DR (Dual Rail) Mode will be overridden and Single Rail Mode forced for the duration of this mode. This will configure the RNEG/LCV_n output pin to function as a PRBS error indicator. All errors will be flagged on this pin. The errors will also be accumulated in the 16-bit error counter for the channel. 2. If the user enables the PRBS Generator and PRBS Receiver, the channel will ignore the data that is being accepted from the system-side equipment (via the TxPOS_n and TxNEG_n input pins) and will overwrite this outbound data with the PRBS pattern. 3. The system must provide an accurate and stable data-rate clock to the TxClk_n pin during this operation.
4	RLB_n	R/W	**Loop-Back Select - RLB Bit - Channel_n:** This read and write bit-field along with the corresponding LLB_n bit-field is used to configure a given channel into various loopback modes as shown by the following table. **LLB_n / RLB_n / Loop-back Mode** 0 / 0 / Normal (No Loop-back) Mode 0 / 1 / Remote Loop-back Mode 1 / 0 / Analog Local Loop-back Mode 1 / 1 / Digital Local Loop-back Mode
3	LLB_n	R/W	**Loop-Back Select - LLB Bit-field - Channel_n:** See the table (above) for RLB_n.

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Table 50: (Continued) Channel Control Registers (CC_n) - Channel n Address Location=0xm6 (n=[0:11] & m=0-5, 8-D)

Bit Number	Name	Type	Description
2	E3_n	R/W	**E3 Mode Select - Channel_n:** This read and write bit-field, along with bit 1 (STS-1/$\overline{DS3}$_n) within this register, is used to configure a given channel into either the DS3, E3 or STS-1 Modes. ■ 0 - Configures channel_n to operate in either the DS3 or STS-1 Modes, depending upon the state of bit 1 (STS-1/$\overline{DS3}$_n) within this same register. ■ 1- Configures channel_n to operate in the E3 Mode.
1	STS-1 / $\overline{DS3}$_n	R/W	**STS-1 or DS3 Mode Select - Channel_n:** This read and write bit-field, along with bit 2 (E3_n) is used to configure a given channel into either the DS3, E3 or STS-1 Modes. This bit-field is ignored if bit 2 (E3_n) has been set to "1". If bit 2 (E3_n) is a 0: ■ 0 - Configures channel_n to operate in the DS3 Mode. ■ 1 - Configures channel_n to operate in the STS-1 Mode.
0	SR / $\overline{DR}$_n	R/W	**Single-Rail / Dual-Rail Select - Channel_n:** This read and write bit-field is used to configure channel_n to operate in either the Single-Rail or Dual-Rail Mode. If the user configures the channel to operate in the Single-Rail Mode, the following will happen: ■ The B3ZS and HDB3 encoder and decoder blocks (within channel_n) will be enabled. ■ The transmit section of channel_n will accept **all** of the outbound data (from the system-side equipment) via the TxPOS_n input pin. ■ The receive section of each channel will output all of the recovered data (to the system-side equipment) via the RxPOS_n output pin. ■ The corresponding RNEG/LCV_n output pin will now function as the LCV (Line Code Violation or Excessive Zero Event) indicator output pin for channel_n. If the user configures channel_n to operate in the Dual-Rail Mode, the following will happen: ■ The B3ZS and HDB3 encoder and decoder blocks of channel_n will be disabled. ■ The transmit section of channel_n will be configured to accept positive-polarity data via the TxPOS_n input pin and negative-polarity data via the TxNEG_n input pin. ■ The receive section of channel_n will pulse the RxPOS_n output pin "High" (for one period of RCLK_n) for each time a positive-polarity pulse is received via the RTIP_n and RRING_n input pins. Likewise, the receive section of each channel will pulse the RxNEG_n output pin "High" (for one period of RxCLK_n) for each time a negative-polarity pulse is received via the RTIP_n/RRING_n input pins. 0 - Configures channel_n to operate in the Dual-Rail Mode. 1 - Configures channel_n to operate in the Single-Rail Mode.

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 51: XRT75R12 Register Map Showing Jitter Attenuator Control Registers (JA_n)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
				R/W	R/W	R/W	R/W

Table 52: Jitter Attenuator Control Registers (JA_n) - Channel n Address Location = 0xm7 (n = [0:11] & m = 0-5, 8-D)

Bit Number	Name	Type	Description
7 - 4	Reserved		
3	JA RESET Ch_n	R/W	**Jitter Attenuator RESET - Channel_n:** Writing a "0 to 1" transition within this bit-field will configure the jitter attenuator (within channel_n) to execute a reset operation. Whenever the user executes a reset operation, then the following will occur: ▪ The read and write pointers (within the jitter attenuator FIFO) will be reset to their default values. ▪ The contents of the Jitter Attenuator FIFO will be flushed. **Note:** The user must follow up any "0 to 1" transition with the appropriate write operation to set this bit-field back to "0", in order to resume normal operation with the jitter attenuator.
2	JA1 Ch_n	R/W	**Jitter Attenuator Configuration Select Input - Bit 1:** This read and write bit-field, along with bit 0 (JA0 Ch_n), is used to do any of the following: ▪ To enable or disable the jitter attenuator corresponding to channel_n. ▪ To select the FIFO depth for the jitter attenuator within channel_n. The relationship between the settings of these two bit-fields and the enable and disable states, and FIFO depths is presented below:
1	JA in Tx Path Ch_n	R/W	**Jitter Attenuator in Transmit and Receive Path Select Bit:** This input pin is used to configure the jitter attenuator (within channel_n) to operate in either the transmit or receive path, as described below: ▪ 0 - Configures the jitter attenuator (within channel_n) to operate in the receive path. ▪ 1 - Configures the jitter attenuator (within channel_n) to operate in the transmit path.
0	JA0 Ch_n	R/W	**Jitter Attenuator Configuration Select Input - Bit 0:** See the description for bit 2 (JA1 Ch_n).

JA0	JA1	Jitter Attenuator Mode
0	0	FIFO Depth = 16 bits
0	1	FIFO Depth = 32 bits
1	0	Disabled
1	1	Disabled

The product (s) mentioned in this data sheet are no longer part of manufactured and may not be ordered (OBS)

Table 53: XRT75R12 Register Map Showing Error Counter MSByte Registers (EM_n)

Address Location	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

Table 54: Error Counter MSByte Register - Channel n Address Location = 0xmA

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MS bit							9th bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 55: XRT75R12 Register Map Showing Error Counter LSByte Registers (EL_n)

Address Location	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 56: Error Counter LSByte Register - Channel n Address Location = 0xmB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8th bit							LS bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 57: XRT75R12 Register Map Showing Error Counter Holding Registers (EH_n)

Address Location	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			EM3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 58: Error Counter Holding Register - Channel n Address Location = 0xmC

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MS bit							LS bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Each channel contains a dedicated 16 bit PRBS error counter. When enabled, this counter will accumulate PRBS errors (as well as excess zeros and LCVs). The LS byte will "carry" a one over to the MS byte each time it rolls over from 255 to zero until the MS byte also reaches 255. When both counters reach 255, no further errors will be accumulated and "all ones" will signify an overflow condition.

The counter can be read while in the active count mode. Either register may be read "on the fly" and the other byte will be simultaneously transferred into the channel's Error Holding Register. The holding register may then be read to supply the host with a correct 16 bit count (as of the instant of reading). With this mechanism, the host could rapidly cycle through reading all twelve counters in order (storing the read byte in scratch RAM) and then come back and read the second byte from each holding register to form the 16 bit accumulation in the host system.

10.0 Specifications

10.1 Absolute Maximum Ratings

Table 59: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units	Comments
V_{DD}	Supply voltage(1)	–0.5	6.0	V	
V_{IN}	Input voltage at any pin(1)	–0.5	5.5	V	
I_{IN}	Input current at any pin(1)		100	mA	
S_{TEMP}	Storage temperature(1)	–65	150	°C	
A_{TEMP}	Ambient operating temperature	–40	85	°C	Industrial temperature grade
Θ_{JA}	Thermal resistance: junction-to-ambient(3)		7.5	°C/W	Linear air flow 200ft per minute
Θ_{JC}	Thermal resistance: junction-to-case		0.5	°C/W	All conditions
M_{LEVL}	Exposure to moisture	5		level	EIA / JEDEC JESD22-A112-A
ESD	ESD rating(2)	2000		V	

1. Exposure to or operating near the minimum or maximum values for extended period may cause permanent failure and impair reliability of the device.

2. ESD testing method is per MIL-STD-883D,M-3015.7.

3. Linear air flow of 200 ft per minute recommended for industrial applications. Θ_{JA} = 9.4°C/W with 0Lft per minute, Θ_{JA} = 7.1 °C/W with 400Lft per minute.

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10.2 DC Electrical Characteristics

Table 60: DC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
DV_{DD}	Digital supply voltage	3.135	3.3	3.465	V
AV_{DD}	Analog supply voltage	3.135	3.3	3.465	V
I_{CC_DS3}	DS3 current consumption using PRBS 2^{23}-1 pattern(3)		1016	1117	mA
I_{CC_DS3JA}	DS3 current consumption using PRBS 2^{23}-1 pattern(4)		1172	1290	mA
I_{CC_E3}	E3 current consumption using PRBS 2^{23}-1 pattern(3)		1040	1140	mA
I_{CC_E3JA}	E3 current consumption using PRBS 2^{23}-1 pattern(4)		1180	1300	mA
I_{CC_STS1}	STS1 current consumption using PRBS 2^{23}-1 pattern(3)		1100	1210	mA
I_{CC_STS1JA}	STS1 current consumption using PRBS 2^{23}-1 pattern(4)		1300	1430	mA
P_{CC_DS3}	DS3 power consumption(5)		3.35	3.87	W
P_{CC_DS3JA}	DS3 power consumption with jitter attenuator enabled(5)		3.87	4.47	W
P_{CC_E3}	E3 power consumption(5)		3.43	3.95	W
P_{CC_E3JA}	E3 power consumption with jitter attenuator enabled(5)		3.89	4.50	W
P_{CC_STS1}	STS1 power consumption(5)		3.63	4.19	W
P_{CC_STS1JA}	STS1 power consumption with jitter attenuator enabled(5)		4.29	4.95	W
V_{IL}	Input low voltage(2)			0.8	V
V_{IH}	Input high voltage(2)	2.0		5.5	V
V_{OL}	Output low voltage, I_{OUT} = –4mA			0.4	V
V_{OH}	Output high voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input leakage current(1)			±10	µA
C_I	Input capacitance			10	pF
C_L	Load capacitance			10	pF

1. Not applicable for pins with pull-up or pull-down resistors.
2. The digital inputs are TTL 5V compliant.
3. With jitter attenuator disabled.
4. With jitter attenuator enabled.
5. These values are **not** a measure of power dissipation. These values represent the total power consumption. For example:
P_{CC} Consumption = **P_{DD}** Dissipation + **P_{LD}** Delivered to Load

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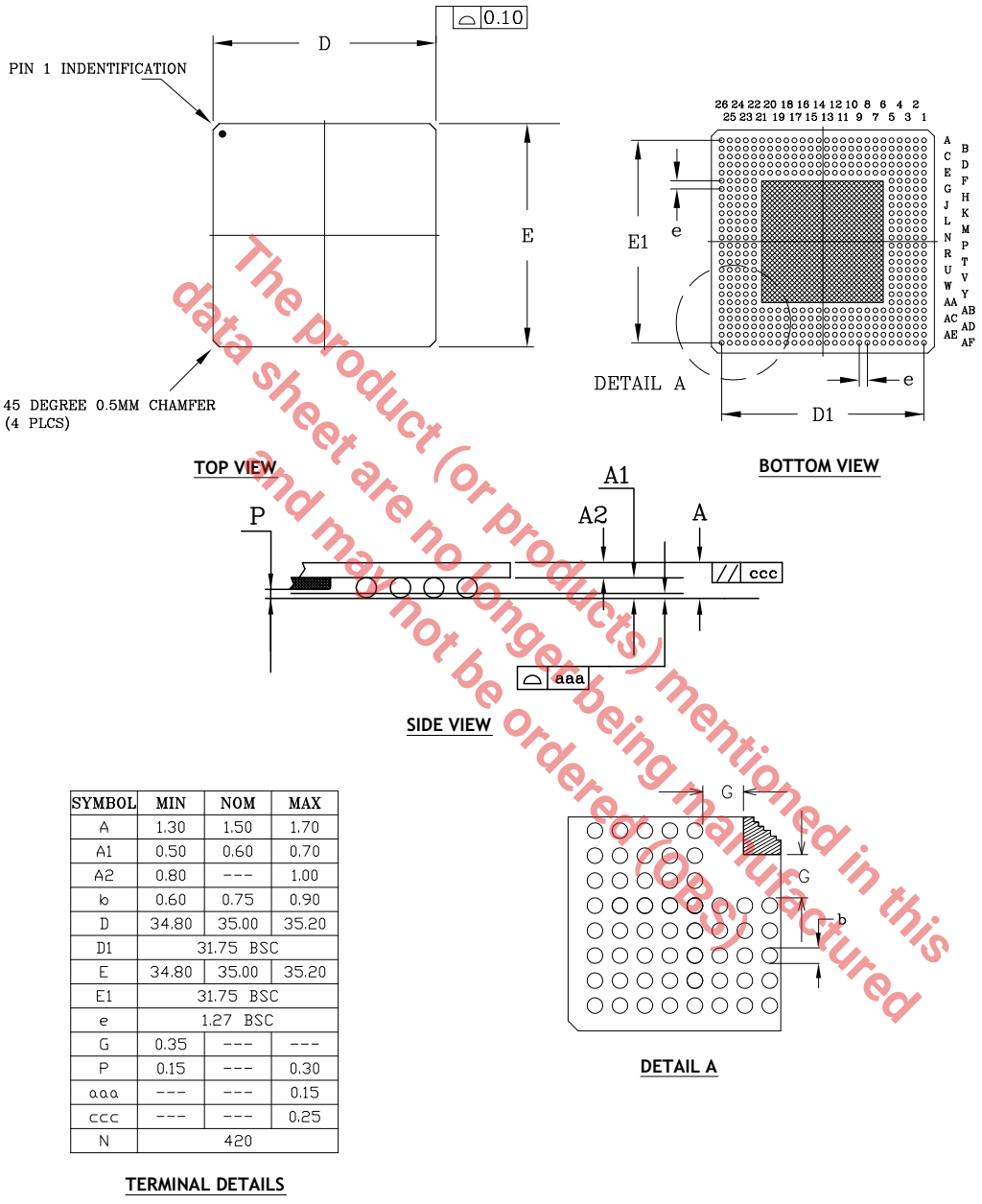
11.0 Mechanical Dimensions

11.1 TBGA420



SYMBOL	MIN	NOM	MAX
A	1.30	1.50	1.70
A1	0.50	0.60	0.70
A2	0.80	---	1.00
b	0.60	0.75	0.90
D	34.80	35.00	35.20
D1	31.75 BSC		
E	34.80	35.00	35.20
E1	31.75 BSC		
e	1.27 BSC		
G	0.35	---	---
P	0.15	---	0.30
aaa	---	---	0.15
ccc	---	---	0.25
N	420		

TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-318.

Drawing No.: POD-000000 153

Revision: A

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Figure 36: Mechanical Dimensions, TBGA420

12.0 Ordering Information

Table 61: Ordering Information(1)

Ordering Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free
XRT75R12IB-L	–40°C to 85°C	TBGA420	Tray	Yes(2)

1. Refer to www.maxlinear.com/XRT75R12 for most up-to-date Ordering Information.

2. Visit www.maxlinear.com for additional information on Environmental Rating.

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