XR68C92/192

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

August 2005

DESCRIPTION

The XR68C92/192 is a Dual Universal Asynchronous Receiver and Transmitter with 8 (XR68C92) / 16 (XR68C192) bytes transmit and receive FIFO. The XR68C92/192 is a pin-to-pin compatible and an improved version of the XR68C681 and the Philips SCC68692 UART with faster data access and other additional features. The operating speed of the receiver and transmitter can be selected independently from a table of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock input. The XR68C92/192 provides a power-down mode in which the oscillator is stopped but the register contents are retained. The XR68C92/192 is fabricated in an advanced CMOS process to achieve low power and high speed requirements.

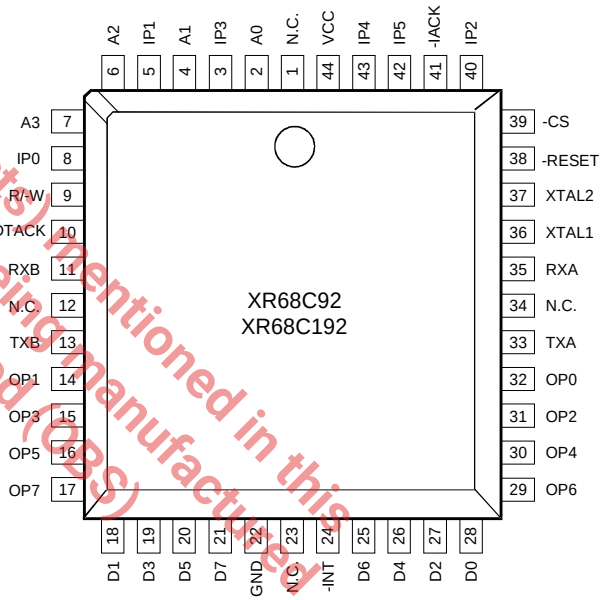
The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FEATURES

Added features in devices with top marking of "D2" and newer:

- 5 volt tolerant inputs
- Pin to pin compatible and improved version of the SCC68692 and XR68C681
- Enhanced Multidrop mode operation with separate storage for address and data tags (9th bit)
- 8 Bytes transmit/receive FIFO (XR68C92)
- 16 Bytes transmit/receive FIFO (XR68C192)
- Standard baud rates from 50bps to 230.4kbps
- Non-standard baud rate of up to 1Mbps
- Transmit and Receive trigger levels
- Watch dog timer
- Programmable clock source for receiver and transmitter of each channel
- Single interrupt output
- 7 Multipurpose inputs, 8 Multipurpose outputs
- 2.97 to 5.5 volt operation
- Programmable character lengths (5, 6, 7, 8)
- Parity, framing, and over run error detection
- Programmable 16-bit timer/counter
- On-chip crystal oscillator
- Power down mode

PLCC Package



ORDERING INFORMATION

Part number	Package	Operating temperature	Device Status
XR68C92CP	40-Lead PDIP	0° C to + 70° C	Active. See the XR68C92CV for new designs.
XR68C92CJ	44-Lead PLCC	0° C to + 70° C	Active
XR68C92CV	44-Lead LQFP	0° C to + 70° C	Active
XR68C92IP	40-Lead PDIP	-40° C to + 85° C	Active. See the XR68C92IV for new designs.
XR68C92IJ	44-Lead PLCC	-40° C to + 85° C	Active
XR68C92IV	44-Lead LQFP	-40° C to + 85° C	Active
XR68C192CJ	44-Lead PLCC	0° C to + 70° C	Active
XR68C192CV	44-Lead LQFP	0° C to + 70° C	Active
XR68C192IJ	44-Lead PLCC	-40° C to + 85° C	Active
XR68C192IV	44-Lead LQFP	-40° C to + 85° C	Active

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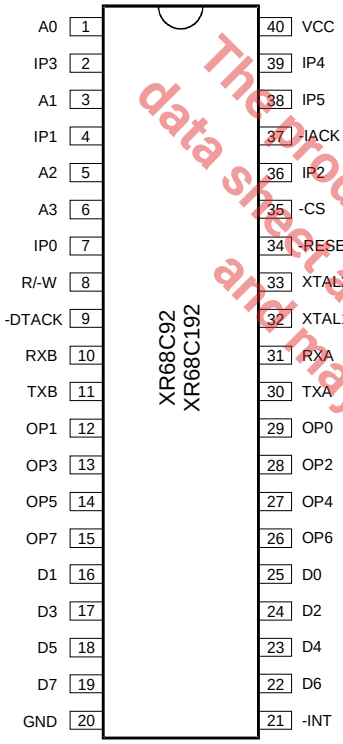
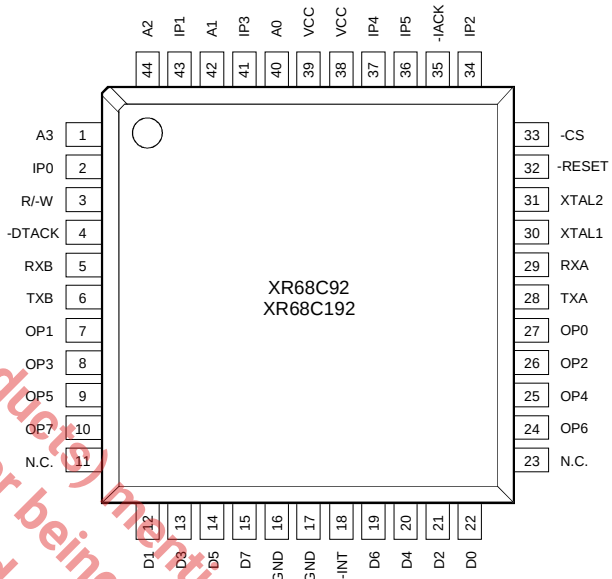
Package Description

40 Pin DIP Package



44 Pin LQFP Package



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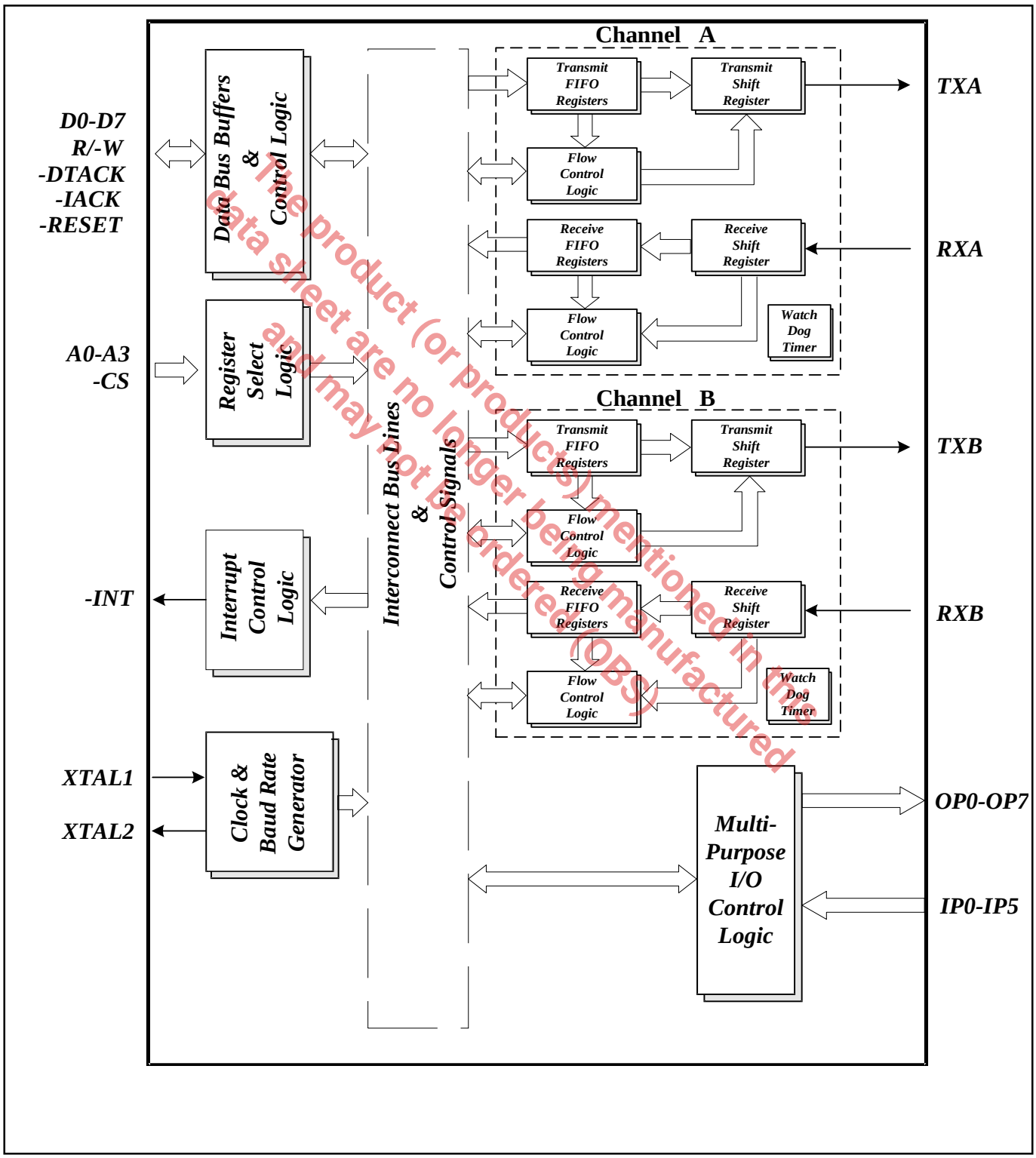
Block Diagram



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SYMBOL DESCRIPTION (* 44 pin LQFP)

Symbol	Pin 44	Pin 40	Pin 44*	Signal type	Pin Description
-RESET	38	34	32	I	Master Reset (active low). A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
A0-A3	2,4, 6,7	1,3, 5,6	40,42, 44,1	I	Address select lines. To select internal registers.
-IACK	41	37	35	I	Interrupt acknowledge (active low). A low on this pin indicates that the CPU has received an interrupt. If not used, this pin should be tied to VCC.
-DACK	10	9	4	O	Data Transfer Acknowledge (three-state active low output). A low on this pin indicates proper transfer of data between the CPU and XR68C92/192 during read, write and interrupt cycles.
-CS	39	35	33	I	Chip select (active low). A low at this pin enables the data bus transfer operation.
D0-D7	28,18 27,19 26,20 25,21	25,16 24,17 23,18 22,19	22,12 21,13 20,14 19,15	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
R/-W	9	8	3	I	Read/Write strobe. When -CS is asserted, a high on this pin transfers the contents of the XR68C92/192 data bus to the CPU, and a low on this pin will transfer the contents of the CPU data bus to the addressed register.
-INT	24	21	18	O	Interrupt output (open drain, active low) This pin goes low upon occurrence of one or more of eight maskable interrupt conditions (when enabled by the interrupt mask register). CPU can read the interrupt status register to determine the interrupting condition(s). This output requires a 10k ohms pull-up resistor.
XTAL1	36	32	30	I	Crystal input 1 or external clock input. A crystal can be connected between this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

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SYMBOL DESCRIPTION (* 44 pin LQFP)

Symbol	Pin 44	Pin 40	Pin 44*	Signal type	Pin Description
XTAL2	37	33	31	O	Crystal input 2 or buffered clock output. See XTAL1.
RXA, RXB	35,11	31,10	29,5	I	Serial data input. The serial information (data) received from serial port to XR68C92/192 receive input circuit. A mark (high) is logic one and a space (low) is logic zero.This input must be held at logic one when idle and during power down.
TXA, TXB	33,13	30,11	28,6	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. This output will be held in mark (high) state during reset, local loop back mode or when the transmitter is disabled.
IP0	8	7	2	I	Multi-purpose input or Channel A Clear-To-Send (-CTSA active low). If not used, this pin should be tied to VCC.
IP1	5	4	43	I	Multi-purpose input or Channel B Clear-To-Send (-CTSB active low). If not used, this pin should be tied to VCC.
IP2	40	36	34	I	Multi-purpose input or Channel B receive external clock input (received data is sampled on the rising edge of the clock) or Timer/Counter External clock input. If not used, this pin should be tied to VCC or GND.
IP3	3	2	41	I	Multi-purpose input or Channel A transmit external clock input. The transmit data is clocked on the falling edge of the clock. If not used, this pin should be tied to VCC or GND.
IP4	43	39	37	I	Multi-purpose input or Channel A receive external clock input. The received data is clocked on the rising edge of the clock. If not used, this pin should be tied to VCC or GND.
IP5	42	38	36	I	Multi-purpose input or Channel B transmit external clock input. The transmit data is clocked on the falling edge of the clock. If not used, this pin should be tied to VCC or GND.
OP0	32	29	27	O	Multi-purpose output. General purpose output or Channel A Request-To-Send (-RTSA active low).
OP1	14	12	7	O	Multi-purpose output. General purpose output or Channel B Request-To-Send (-RTSB active low).
OP2	31	28	26	O	Multi-purpose output. General purpose output or one of the

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SYMBOL DESCRIPTION (* 44 pin LQFP)

Symbol	Pin 44	Pin 40	Pin 44*	Signal type	Pin Description
					following functions can be selected for this output pin by programming the Output Port Confiuration Register bits 1,0; TxAClk1 -Transmit 1X clock. TxAClk16 -Transmit 16X clock RxAClk1 -Receive 1X clock
OP3	15	13	8	O	Multi-purpose output. General purpose output or one of the following functions can be selected for this output pin by programming the Output Port Confiuration Register bits 3,2; C/T -Counter timer output (Open drain output) TxBClk1 -Transmit 1X clock RxBClk1 -Receive 1X clock
OP4	30	27	25	O	Multi-purpose output. General purpose output or one of the following functions can be selected for this output pin by programming the Output Port Confiuration Register bit 4; -RxARDY -Receive ready signal (Open drain output) -RxAFULL - Receive FIFO full signal (Open drain output)
OP5	16	14	9	O	Multi-purpose output. General purpose output or one of the following functions can be selected for this output pin by programming the Output Port Confiuration Register bit 5; -RxBRDY - Receive ready signal (Open drain output) -RxBFULL - Receive FIFO full signal (Open drain output)
OP6	29	26	24	O	Multi-purpose output. General purpose output or Transmit A holding register empty interrupt (-TxARDY Open drain output).
OP7	17	15	10	O	Multi-purpose output. General purpose output or Transmit B holding register empty interrupt (-TxBRDY Open drain output)
GND	22	20	16,17	Pwr	Signal and power ground.
VCC	44	40	38,39	Pwr	Power supply input, 2.97V to 5.5V.
N.C.	1,12 23,34	-	11,23		No Connection.

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INTERNAL CONTROL LOGIC

The internal control logic of the XR68C92/192 receives operation commands from the central processing unit (CPU) and generates appropriate signals to the internal sections to control device operation. The internal control logic takes in the following inputs:

- -CS, which is the XR68C92/192 chip-select;
- R/-W which allows data transfers between the CPU and XR68C92/192via the data bus (D0 to D7);
- four register-select lines (A0 through A3) which are decoded to allow access to the registers within the XR68C92/192;
- -RESET (reset), which initializes or resets all outputs and internal registers.

COMMUNICATION CHANNELS A AND B

Each communication channel includes a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and each transmitter can be selected independently from the baud rate generator, the Counter/Timer (C/T), or from an external clock. The transmitter accepts parallel data from the CPU, converts it to a serial bit stream in the form of a character and outputs it on the Transmit Data output pin (TXA, TXB). The character consists of start, stop, and optional parity bits, The receiver accepts serial data on the Receive Data input pin (RXA, RXB), converts this serial input to parallel format, checks for a start bit, stop bit, parity bit (if any), framing error, overrun or break condition, and transfers the data byte to the CPU during read operations.

TIMING LOGIC

The timing logic consists of

- a crystal oscillator,
- a baud rate generator (BRG),
- clock selector logic, and
- a programmable 16-bit counter/timer (C/T).

The *crystal oscillator* operates directly from a typical 3.6864 MHz crystal connected across the XTAL1 and XTAL2 inputs or from an external clock of the appropriate frequency connected to XTAL1. The XTAL1 clock serves as the basic timing reference for the baud rate generator, the C/T, and other internal circuits.

The *baud rate generator* operates from the XTAL1 clock input and can generate 28 commonly used data communication baud rates (if a typical 3.6864MHz crystal or clock is used) ranging from 50 to 230.4kbps by producing internal clock outputs at 16 times the actual baud rate. In addition, other baud rates can be derived by connecting 16X or 1X clocks to multipurpose input port pins IP3 - IP6 that have alternate functions as receiver or transmitter clock inputs.

Clock selector logic consists of the clock selector register (CSRA, CSRB), bits 0 & 2 of Mode Register 0 (MR0A, MR0B) and bit-7 of Auxilliary Control Register (ACR). These allow various combinations of these baud rates for receiver and transmitter of each channel. See Baud Rate Table on page 18 for more details.

The *programmable 16-bit counter/timer (C/T)* can produce a 16X clock for other baud rates by counting down its programmed clock source. Users can program the 16 bit C/T within the XR68C92/192 to use one of several clock sources as its input. The output of the C/T is available to the internal clock selectors and can also be programmed to appear at output OP3. In the timer mode, the C/T acts as a programmable divider and can generate a square-wave output at OP3. In the counter mode, the C/T can be started and stopped under program control. When stopped, the CPU can read its contents. The counter counts down the number of pulses stored in the concatenation of the C/T upper register and C/T lower register and produces an interrupt. This is a system-oriented feature that can be used to record timeouts when implementing various application protocols.

INTERRUPT CONTROL LOGIC

The following registers are associated with the interrupt control logic:

- Interrupt Mask Register (IMR)
- Interrupt Status Register (ISR)
- Auxiliary Control Register (ACR)
- Interrupt Vector Register (IVR)

A single active-low interrupt output (-INT) can notify the CPU that any of eight internal events has occurred. These eight events are described in the discussion of the interrupt status register (ISR). User can program the interrupt mask register (IMR) to allow only certain conditions to cause -INT to be asserted while the CPU can read the ISR to determine all currently active interrupting conditions. When an active-low interrupt acknowledge signal (-IACK) from the CPU is asserted

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while the XR68C92/192 has an interrupt pending, the XR68C92/192 will place the contents of the interrupt vector register (IVR, address 0x0C) on the data bus and assert the data transfer acknowledge signal (-DACK). If the XR68C92/192 has no pending interrupt, it ignores the -IACK cycles. In addition, users can program the parallel outputs OP3 through OP7 to provide discrete interrupt outputs for the transmitters, the receivers, and the C/T. See 'Multi-purpose Outputs' section for details.

DATA BUS BUFFER (D0 - D7)

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the internal control logic to allow read and write data transfer operations to occur between the controlling CPU and XR68C92/192 by way of the eight parallel data lines (D0 through D7).

MULTI-PURPOSE INPUTS (IP0 - IP5)

The states of the seven multi-purpose inputs (IP0 through IP5) can be read from the internal register IPR (address 0x0D). The bits in this register are the complements of the actual inputs - for example, if the IP0 is low, the corresponding bit in the IPR, bit-0 is a logic '1'. Each of these inputs also has an alternate control function capability. The alternate functions can be enabled/disabled on a bit-by-bit basis. The table below shows how each of these inputs is configured for its special function.

Four change-of-state detectors are associated with inputs IP0, IP1, IP2, and IP3. If a high-to-low or low-to-high transition occurs on any of these inputs, the corresponding bit in the input port change register (IPCR - address 0x04) will be set accordingly. The sampling clock of the change detectors is the XTAL1/96 tap of the baud rate generator, which is 38.4kHz if XTAL1 is 3.6864MHz. A new input level must be sampled on two consecutive sampling clocks to detect a change. Also, users can program the XR68C92/192 to allow a change of state in any of the inputs IP0 through IP3 to generate an interrupt to the CPU. See description of the Interrupt Status Register (ISR, address 0x05) for details. The IPCR bits are cleared when the CPU reads the register. Also see the Baud Rate Table on page 18.

Input	Function	Programming
IP0	-CTSA	Set MR2A bit-4 = 1
IP1	-CTSB	Set MR2B bit-4 = 1
IP2	C/T Ext. Clk	Set ACR[6:4] = 000
IP3	TxA Ext. Clk	Set CSRA[3:0] = 1110 or 1111
IP4	RxA Ext. Clk	Set CSRA[7:4] = 1110 or 1111
IP5	TxB Ext. Clk	Set CSRB[3:0] = 1110 or 1111

MULTI-PURPOSE OUTPUTS (OP0 - OP7)

The eight output pins (OP0 - OP7) can either be used as general purpose outputs or can be used for alternate functions representing various conditions using
- Mode Registers 1 and 2 (MR1A, MR1B, MR2A, MR2B)
- Output Port Configuration Register (OPCR)
- Set Output Port Register (SOPR), and
- Reset Output Port Register (ROPR).

OP0 and OP1:

The output OP0 can function as the channel A request-to-send (-RTSA) output for either the transmitter (MR2A bit-5 = 1) or the receiver (MR1A bit-7 = 1). Note that only one of these bits should be set to '1' at a given time. See the description of the transmitter RTS and receiver RTS in the 'Transmitter' and 'Receiver' sections of this datasheet respectively. The output OP1 acts as the channel B request-to-send (-RTSB) output

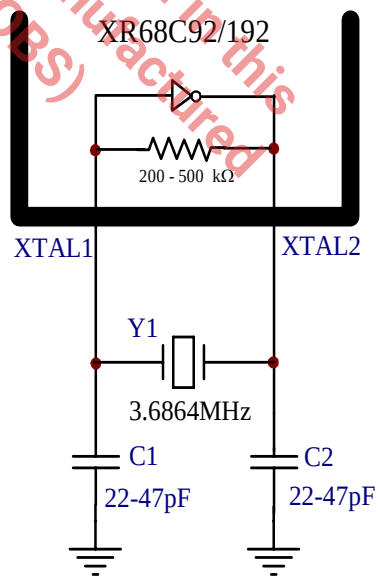

Figure 1: Crystal Connection

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and is controlled in a similar way by the channel B registers.

OP2 - OP7:

The other outputs (OP2 - OP7) are configured via the OPCR. Please see the description under the OPCR register for the details.

CRYSTAL INPUTS (XTAL1 & XTAL2)

If a crystal is used, it is connected between XTAL1 and XTAL2, in which case a capacitor of approximately 22 to 47 pF should be connected from each of these pins to ground (see Figure 1). If an external CMOS-level clock is used, the pin XTAL2 must be left open.

RESET

The XR68C92/192 can be reset by asserting the -RESET signal or by programming the appropriate internal registers. A hardware reset (assertion of -RESET) clears the following registers:

- Status Registers A and B (SRA and SRB)
- Interrupt Mask Register (IMR)
- Interrupt Status Register (ISR)
- Output Port Configuration Register (OPCR)

RESET also performs the following operations:

- Initializes the interrupt vector register (IVR) to 0x0F.
- Places the outputs OP0 through OP7 in the high state
- Places the counter/timer in counter mode
- Places channels A and B in the inactive state with the transmitter serial-data outputs (TXA and TXB) in the mark (high) state.

Reset commands can be programmed through the command registers to reset the receiver, transmitter, error status, or break-change interrupts for each channel.

TRANSMITTER

The transmitter converts the parallel data from the CPU to a serial bit stream on the transmitter output pin (TXA, TXB). It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least-significant bit is sent first. Data is shifted out the transmit serial data output pin (TXA, TXB) on the falling edge of the programmed clock source (XTAL1,

NOTE: The terms assertion and negation will be used extensively to avoid confusion when dealing with a mixture of "active low" and "active high" signals. The term assert or assertion indicates that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation indicates that a signal is inactive or false.

IP3 or IP5: see CSR bits 3:0). After the transmission of the stop bits, and a new character is not available in the transmit FIFO, the transmitter serial data output (TXA, TXB) remains high. Transmission resumes when the CPU loads a new character into the transmit FIFO. If the transmitter receives a disable command (CRA, CRB bits 3:2), it will continue operating until the character in the transmit shift register is completely sent out. Other characters in the FIFO are neither sent nor discarded, but will be sent when the transmitter is re-enabled.

TX RTS Control: Users can program the transmitter to automatically negate the request-to-send (RTS) output (alternate function of OP0 and OP1 for channels A and B respectively) on completion of a message transmission (using MR2A, MR2B bit-5). If the transmitter is programmed to operate with RTS control, the RTS output must be manually asserted before each message is transmitted. Also, the transmitter needs to be disabled after all the required data are loaded into the FIFO. Then, the RTS output will be automatically negated when the transmit-shift register and the TX FIFO are both empty. In automatic RTS mode, no more characters can be written to the FIFO after the transmitter is disabled.

If auto clear-to-send (CTS) control is enabled (using MR2A, MR2B bit-4), the CTS input (alternate function of IP0 and IP1 for channels A and B respectively) must be asserted (low) in order for the character to be transmitted. If it gets negated (high) in the middle of a transmission, the character in the shift register is transmitted and the transmit data output (TXA, TXB) then remains in the marking state until CTSA, CTSB gets asserted again.

The transmitter can also be forced to send a continuous low (space) condition by issuing the start-break command (see CRA, CRB bits 7:4). The state of CTS is ignored by the transmitter when it is set to send a break.

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A start-break is deferred as long as the transmitter has characters to send, but if normal character transmission is inhibited by CTS, the start-break will proceed. The start-break must be terminated by a stop-break or a TX disable + TX reset before normal character transmission can resume.

The channel A and B transmitters are enabled for data transmission through their respective command registers (see CRA, CRB bits 3:2). The transmit FIFO trigger levels (see MR0A, MR0B bits 4 and 5) are used to generate an interrupt request to the CPU on the -INT pin. This is also reflected in the Interrupt Status Register, ISR bit-0 for channel A and bit-4 for channel B. This is different from the TxRDY bit in the status register.

The TxRDY bit in the status register (SRA, SRB bit-2) indicates if the TX FIFO has at least one empty location. This can also be programmed to appear at the output pin OP6/OP7. The TxEMT bit (SRA, SRB bit-3) indicates if both the TX FIFO and the TX Shift Register are empty.

The transmitter can be reset through a software command (CRA, CRB bits 7:4). If it is reset, operation ceases immediately and must be enabled through the command register before resuming operation. Reset also discards any characters in the FIFO.

RECEIVER

The channel A and B receivers are enabled for data reception through the respective channels command register (CRA, CRB bits 1:0). The channels receiver looks for the high-to-low (mark-to-space) transition of a start bit on the receiver serial-data input pin. If operating in 16X clock mode, the serial input data is resampled on the next 7 clocks. If the receiver serial data is sampled high, the start bit is invalid and the search for a valid start bit begins again. If receiver serial data is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals (at the theoretical center of the bit) until the proper number of data bits and the parity bit (if any) have been assembled and one stop bit has been detected. If an 1X clock is used, data is sampled at one bit time intervals throughout, including the start bit. Data on the receiver serial data input pin is sampled on the rising edge of the programmed clock source (XTAL1, IP4 or IP6: see CSR bits 7:4).

In this process, the least significant bit is received first. The receiver buffer is composed of the FIFO (8/16 locations in XR68C92/192 respectively) and a receive shift register connected to the receiver serial-data input. Data is assembled in the shift register and loaded into the bottom most empty FIFO location. If the character length is less than eight bits, the most significant unused bits are set to zero.

If the stop bit is sampled as a 1, the receiver will immediately look for the next start bit. However, if the stop bit is sampled as a 0, either a framing error or a received break has occurred. If the stop bit is 0 and the data and parity (if any) are not all zero, it is a framing error. The damaged character is transferred to the FIFO with the framing error flag set. If the receiver serial data remains low for one-half of the bit period after the stop bit was sampled, the receiver operates as if a new start bit transition has been detected. If the stop bit is 0 and the data and parity (if any) bits are also all zero, it is a break. A character consisting of all zeros will be loaded into the the FIFO with the received-break bit (but not the framing error bit) set to one. The receiver serial-data input must return to a high condition for at least one-half bit time before a search for the next start bit begins. Also, at this time, the received break bit is reset.

The receiver can detect a break that starts in the middle of a character provided the break persists completely through the next character time or longer. When the break begins in the middle of a character, the receiver will place the damaged character in the FIFO with the framing error bit set. Then, provided the break persists through the next character time, the receiver will also place an all-zero character in the FIFO with the received-break bit set. The parity error, framing error, overrun error, and received-break conditions (if any) set error and break flags in the status register at the received character boundary and are valid only when the receiver-ready bit (RXRDY) in the status register is set.

The receiver-ready bit in the status register (SRA, SRB bit-0) is set whenever one or more characters are available to be read by the CPU. A read of the receiver buffer produces an output of data from the top of the FIFO stack. After the read cycle, the data at the top of the FIFO stack and its associated status bits are “popped” and new data can be added at the bottom of the stack by the receive shift register. The FIFO-full status bit (SRA, SRB bit-1) is set if all 8 (or 16) stack positions are filled with data. Either the receiver-ready

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or the FIFO-full status bits can be selected to cause an interrupt (see MR1A, MR1B bit-6).

In addition to the data byte, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO (overrun is not). By programming the error-mode control bit (MR1A, MR1B bit-5), status can be provided for "character" or "block" modes. In the "character" mode, the status register (SRA, SRB) is updated on a character-by-character basis and applies only to the character at the top of the FIFO. Thus, the status must be read before the character is read. Reading the character pops the data byte and its error flags off the FIFO. In the "block" mode, the status provided in the status register for the parity error, framing error, and received-break conditions are the logical OR of these respective bits for all the data bytes in the FIFO stack since the last reset error command (see CRA, CRB bits 7:4) was issued. That is, beginning immediately after the last reset-error command was issued, a continuous logical-OR function of corresponding status bits is produced in the status register as each character enters the FIFO.

The block mode is useful in applications requiring the exchange of blocks of information where the software overhead of checking each character's error flags cannot be tolerated. In this mode, entire messages can be received and only one data integrity check is performed at the end of each message. Although data reception in this manner has speed advantages, there are also disadvantages. If an error occurs within a message the error will not be recognized until the final check is performed. Also, there is no indication of which character(s) is in error within the message.

Reading the status register (SRA, SRB) does not affect the FIFO. The FIFO is "popped" only when the receive buffer is read. If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected, but the character previously in the shift register is lost and the overrun-error status bit will be set upon receipt of the start bit of the new overrunning character.

To support flow control, a receiver can automatically negate and reassert the request-to-send (RTS) output (RX RTS control - see MR1A, MR1B bit-7). The request-to-send output (at OP0 or OP1 for channel A or B respectively) will automatically be negated by the receiver when a valid start bit is received and the FIFO stack is full. When a FIFO position becomes available, the request-to-send output will be reasserted automatically by the receiver. Connecting the request-to-send output to the clear-to send (CTS) input of a transmitting device prevents overrun errors in the receiver. The RTS output must be manually asserted the first time. Thereafter, the receiver will control the RTS output.

If the FIFO stack contains characters and the receiver is then disabled, the characters in the stack can still be read but no additional characters can be received until the receiver is again enabled. If the receiver is disabled while receiving a character, or while there is a character in the shift register waiting for a FIFO opening, these characters are lost. If the receiver is reset, the FIFO stack and all of the receiver status bits, the corresponding output ports, and the interrupt request are reset. No additional characters can be received until the receiver is again enabled.

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LOOPBACK MODES

Besides the normal operation mode in which the receiver and transmitter operate independently, each XR68C92/192 channel can be configured to operate in various looping modes (see MR2A, MR2B bits 7:6) that are useful for local and remote system diagnostic functions.

AUTOMATIC ECHO MODE

In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The local CPU-to-receiver communication continues normally but the CPU-to-transmitter link is disabled.

LOCAL LOOPBACK MODE

In this mode, the transmitter output is internally connected to the receiver input. The external TX pin is held in the mark (high) state in this mode. By sending data to the transmitter and checking that the data assembled by the receiver is the same data that was sent, proper channel operation can be assured. In this mode the CPU-to-transmitter and CPU-to-receiver communications continue normally.

REMOTE LOOPBACK MODE

In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The local CPU-to-receiver and CPU-to-transmitter links are disabled.

This mode is useful in testing the receiver and transmitter operation of a remote channel. This mode requires the remote channel receiver to be enabled.

MULTIDROP MODE - Enhanced with Extra A/D Tag Storage

Users can program the channel to operate in a wake-up mode for Multidrop applications. In this mode of operation (set MR1A, MR1B bits 4:3 = 11), the XR68C92/192, as a master station channel connected to several slave stations (a maximum of 256 unique slave stations), transmits an address character followed by a block of data characters targeted for one or more of the slave stations. The channel receivers within the slave stations are disabled, but they continuously monitor the data stream sent out from the master station. When the slave stations' receivers detect an address character, each receiver notifies its respective CPU by setting receiver ready (-RXRDY) and generating an interrupt, if programmed to do so. Each slave station CPU then compares the received address to its station address and enables its receiver if the addresses match. Slave stations that are not addressed, continue monitoring the data stream for the next address character. An address character marks the beginning of a new block of data. After receiving a block of data, the slave stations CPU may disable the channel receiver and re-initiate the process.

A transmitted character from the master station consists of a start bit, the programmed number of data bits, an address/data (A/D) bit tag (replacing the parity bit used in normal operation), and the programmed number of stop bits. The A/D tag indicates to the slave stations channel whether the character should be interpreted as an address character or a data character. The character is interpreted as an address character if the A/D tag is set to a '1' or interpreted as a data character if it is set to a '0'. The polarity of the transmitted A/D tag is selected by programming MR1A, MR1B bit-2 to a '1' for an address character and to a '0' for data characters. Users should program the mode register prior to loading the corresponding data or address characters into the transmit buffer.

As a slave station, the XR68C92/192 receiver continuously monitors the received data stream regardless of whether it is enabled or disabled. If the receiver is disabled, it sets the receiver ready status bit and loads the character into the FIFO receive holding register stack provided the received A/D tag is a '1' (address tag). The received character is discarded if the received address/data bit is a '0' (data tag). If the receiver is enabled, all received characters are transferred to the CPU during read operations. In either case, the data bits are loaded into the data portion of the FIFO stack while the address/data bit is loaded into the status portion of the FIFO stack normally used for parity error (SRA, SRB bit-5). Framing error, overrun error, and break-detection operate normally regardless of whether the receiver is enabled or disabled. The address/data (A/D) tag takes the place of the parity bit and parity is neither calculated nor checked for characters in this mode.

Extra Storage For The A/D Tag: The unique feature of XR68C92/192 is that the the user need not wait at all in order to change the A/D tag from address to data (whereas in the case of SC26C92, a wait of at least 2 bit-times is required before changing the A/D tag). This allows the user to possibly load the entire polling packet data to the TX FIFO.

WATCHDOG TIMER

Each of the two receivers (channel A & B) has its own 'watchdog timer' which is separate from and independent of the Counter/Timer. The watchdog timer is used to generate a receive ready time-out interrupt. When it is enabled, a counter is started everytime a character is transferred from the receive shift register to the receive FIFO and times out after 64 bit-times, at which point it will generate a receive interrupt. This is a useful feature especially when the incoming data is not a continous stream of data. For example, if RX trigger levels are used and the last set of characters is smaller than the trigger level, a receive time-out interrupt is generated instead of a regular receive interrupt. The watchdog timer, however, is not accurate as it uses the incoming data for its timing. For more accurate timing, the time-out mode in Counter/Timer should be used (see below).

COUNTER/TIMER

The 16-bit counter/timer (C/T) can operate in a counter mode or a timer mode. In either mode, users can program the C/T input clock source to come from several sources (see ACR bits 6:4) and program the C/T output to appear on output port pin OP3 (see OPCR bits 3:2). The value (pre-load value) stored in the concatenation of the C/T upper register (CTPU, address 0x6) and the C/T lower register (CTPL, ad-

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dress 0x7) can be from 0x0001 through 0xFFFF and can be changed at any time. At power-up and after reset, the C/T operates in counter mode.

COUNTER MODE

In counter mode, the CPU can start and stop the C/T. This mode allows the C/T to function as a system stopwatch or a real-time single interrupt generator. In this mode, the C/T counts down from the pre-load value using the programmed counter clock source. When a read at the start counter command register (address 0xE) is performed, the counter is initialized to the pre-load value and begins a countdown sequence. When the counter counts from 0x0001 to 0x0000 (terminal count), the C/T-ready bit in the interrupt status register (ISR Bit-3) is set.

Users can program the counter to generate an interrupt request for this condition on the -INT output by unmasking the bit-3 in the Interrupt Mask Register (IMR, address 0x5). After 0x0000 the count becomes 0xFFFF, and the counter continues counting down from there. If the CPU changes the pre-load value, the counter will not recognize the new value until it receives the next start counter command (and is reinitialized). When a read at the stop counter command register (address 0xF) is performed, the counter stops the countdown sequence and clears ISR Bit-3. The count value should only be read while the counter is stopped because only one of the count registers (either CUR, at address 0x6 or CLR, at address 0x7) can be read at a time. If the counter is running, a decrement of CLR that requires a borrow from the CUR could take place between the two register reads. Figure 2 shows the C/T output in the counter mode. OP3 can be programmed to show the C/T output.

In addition to the watch dog timer described above, the C/T can be used for receive timeout function (see description under CRA, CRB in the registers section also). The C/T is more accurate and the timeout period is programmable unlike the watchdog timer. However, only one channel can use the C/T for receive timeout at any given time. The C/T timeout mode uses the received data stream to start the counter. Each time a character is shifted from the receive shift register to the receive FIFO, the C/T is reloaded with the programmed value in CTPU and CTPL and it restarts on the next C/T clock. If a new character is not received before the C/T reaches terminal count (= 0x0000), a counter ready interrupt (ISR bit-3) is generated. The user can appropriately program the CTPU and CTPL for the desired timeout period. Typically this is slightly more than one character time. Note that if C/T is used for receiver timeout, a counter ready interrupt is generated whereas if the watchdog timer is used, a receiver ready interrupt is generated.

TIMER MODE

In the timer mode, the C/T runs continuously once the start command is issued (by reading the start C/T

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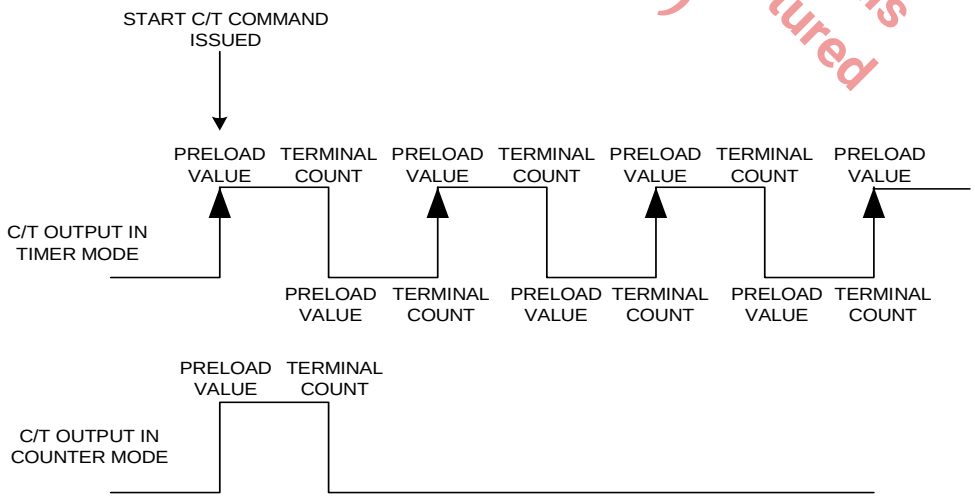

Figure 2: C/T output in Timer and Counter modes.

command register) and the CPU cannot stop it. When the stop command is issued (by reading the stop C/T command register), the CPU only resets the C/T interrupt. This mode allows the C/T to be used as a programmable clock source for channels A and B (see CSRA, CSRB register), and/or a periodic interrupt generator. In this mode, the C/T generates a square-wave output (see Figure 2) derived from the programmed timer input clock source. The square wave generated by the timer has a period of *2 X (pre-load value) X (period of clock source)* and is available as a clock source for both channels A and B. Since the timer cannot be stopped, the values in the registers (CUR:CLR) should not be read. See description of ACR register to see how to choose clock source for the C/T.

When the start counter command register (STCR, address 0xE) is read, the C/T terminates the current countdown sequence and sets its output to a '1' (OP3 can be programmed to show this output). The C/T is then initialized to the pre-load value, and begins a new countdown sequence. When the terminal count is reached (0x0000), the C/T sets its output to a '0'. Then, it gets re-initialized to the pre-load value and repeats the countdown sequence. See Figure 2 for the resulting waveform.

The timer sets the C/T-ready bit in the interrupt status register (ISR Bit-3) every other time it reaches the terminal count (at every rising edge of the output). Users can program the timer to generate an interrupt request for this condition (every second countdown cycle) on the -INT output. If the CPU changes the pre-load value, the timer will not recognize the new value until either

(a) it reaches the next terminal count and is reinitialized automatically, or

(b) it is forced to re-initialize by a start command.

When a read at the stop counter command address is performed, the timer clears ISR Bit-3 but does not stop. Because in timer mode the C/T runs continuously, it should be completely configured (pre-load value loaded and start counter command issued) before programming the timer output to appear on OP3.

OTHER PROGRAMMING REMARKS

The contents of internal registers should not be changed during receiver/transmitter operation as certain changes can produce undesired results. For example, changing the number of bits per character while the transmitter is active will result in transmitting an incorrect character. The contents of the clock-select register (CSR) and ACR Bit-7 should only be changed after the receiver(s) and transmitter(s) have been issued software RX and TX reset commands. Similarly, changes to the auxiliary control register (ACR Bits 4-6) should only be made while the counter/timer (C/T) is not used.

The mode registers of each channel MR0, MR1 and MR2 are accessed via an auxiliary pointer. The pointer is set to mode register one (MR1) by RESET. It can be set to MR0 or MR1 by issuing a “reset pointer” command (0xB0 or 0x10 respectively) via the channel's command register. Any read or write of the mode register switches the pointer to next mode register. All accesses subsequent to reading/writing MR1 will address MR2 unless the pointer is reset to MR0 or MR1 as described above. The mode, command, clock-select, and status registers are duplicated for each channel to allow independent operation and control (except that both channels are restricted to baud rates that are in the same set).

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INTERNAL REGISTER DESCRIPTIONS

A3	A2	A1	A0	READ Operation	WRITE Operation
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock-Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Receiver Buffer A (RXA)	Transmitter Buffer A (TXA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper Register (CUR)	C/T Preload value Upper Register (CTPU)
0	1	1	1	Counter/Timer Lower Register (CLR)	C/T Preload value Lower Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock-Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Receiver Buffer B (RXB)	Transmitter Buffer B (TXB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port Register (IPR)	Output Port Configuration Register (OPCR)
1	1	1	0	Start C/T Command (STCR)	Set Output Port Register (SOPR)
1	1	1	1	Stop C/T Command (SPCR)	Reset Output Port Register (ROPR)

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A3	A2	A1	A0	Register [Default]	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	0	MRA0[00]	Watch dog timer	RX trigger level [1]	TX trigger level [1]	TX trigger level [0]	Not used	Baud rate ext. 2	Factory test mode	Baud rate ext. 1
1	0	0	0	MRB0[00]	Watch dog timer	RX trigger level [1]	TX trigger level [1]	TX trigger level [0]	Not used	Not used	Not used	Not used
0 1	0 0	0 0	0 0	MRA1[00] MRB1[00]	RX RTS control	RX trigger level [0]	Error mode	Parity mode	Parity mode	Parity type	Word length	Word length
0 1	0 0	0 0	0 0	MRA2[00] MRB2[00]	Loopback mode select	Loopback mode select	TX RTS control	Auto CTS control	Stop bit length	Stop bit length	Stop bit length	Stop bit length
0 1	0 0	0 0	1 1	SRA[00] SRB[00]	Received break	Framing error	Parity error	Overrun error	Tx empty	Tx ready	Rx FIFO full	Rx ready
0 1	0 0	0 0	1 1	CSRA[00] CSRB[00]	RX clock	RX clock	RX clock	RX clock	TX clock	TX clock	TX clock	TX clock
0 1	0 0	1 1	0 0	CRA[00] CRB[00]	Misc. command	Misc. command	Misc. command	Misc. command	TX disable	TX enable	RX disable	RX enable
0 1	0 0	1 1	1 1	RXA[XX] RXB[XX]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0 1	0 0	1 1	1 1	TXA[XX] TXB[XX]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	1	0	0	IPCR[00]	Delta IP3	Delta IP2	Delta IP1	Delta IP0	IP3 input	IP2 input	IP1 input	IP0 input
0	1	0	0	ACR[00]	Baud rate set select	C/T mode	C/T mode	C/T mode	Delta IP3 int.	Delta IP2 int.	Delta IP1 int.	Delta IP0 int.
0	1	0	1	ISR[00]	Input port change	Delta break B	RxB ready	TxB ready	C/T ready	Delta break A	RxA ready	TxA ready
0	1	0	1	IMR[00]	Input port change	Delta break B	RxB ready	TxB ready	C/T ready	Delta break A	RxA ready	TxA ready
0	1	1	0	CTPU[00] CUR[00]	Bit-15	Bit-14	Bit-13	Bit-12	Bit-11	Bit-10	Bit-9	Bit-8
0	1	1	1	CTPL[00] CLR[00]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	0	0	IVR[0F]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	0	1	IPR[XX]	Not Used	Not Used	IP5	IP4	IP3	IP2	IP1	IP0
1	1	0	1	OPCR[00]	OP7	OP6	OP5	OP4	OP3	OP3	OP2	OP2
1	1	1	0	STCR[XX]	X	X	X	X	X	X	X	X
1	1	1	0	SOPR[00]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	1	1	SPCR[XX]	X	X	X	X	X	X	X	X
1	1	1	1	ROPR[00]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

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MODE REGISTER 0 (MR0A, MR0B)

This register is accessed only when command is applied via CRA, CRB register (upper nibble = 0xB). After reading or writing to MR0A (or MR0B) register, the mode register pointer will point to MR1A (or MR1B) register.

MR0A Bit-0:
Extended baud rate table selection for both channels.
0 = Normal baud rate tables
1 = Extended baud rate tables 1

MR0A Bit-1: Special Function.
0 = Normal
1 = Factory test mode

MR0A Bit-2:
Extended baud rate table selection for both channels.
0 = Normal baud rate tables
1 = Extend baud rate tables 2

MR0A Bit-3, MR0B Bits 3-0:
Not Used. Any write to this bit is ignored.

MR0A, MR0B Bits 5-4:
Transmit trigger level select.

Bit-5	Bit-4	XR68C92
0	0	8 FIFO locations empty (default)
0	1	4 FIFO locations empty
1	0	6 FIFO locations empty
1	1	1 FIFO location empty

Bit-5	Bit-4	XR68C192
0	0	16 FIFO locations empty (default)
0	1	6 FIFO locations empty
1	0	12 FIFO locations empty
1	1	1 FIFO location empty

MR0A, MR0B Bit-6:
Receive trigger level select. This bit is associated with MR1 Bit-6.

MR0 Bit-6	MR1 Bit-6	XR68C92
0	0	1 byte in FIFO (default)
0	1	3 bytes in FIFO
1	0	6 bytes in FIFO
1	1	8 bytes in FIFO

MR0 Bit-6	MR1 Bit-6	XR68C192
0	0	1 byte in FIFO (default)
0	1	6 bytes in FIFO
1	0	12 bytes in FIFO
1	1	16 bytes in FIFO

MR0A, MR0B Bit-7:
Receive time-out (watch dog timer).
0 = Disabled (default)
1 = Enabled
See description under 'Watchdog Timer'.

MODE REGISTER 1 (MR1A, MR1B)

MR1A, MR1B are accessed after reset or by command applied via CRA, CRB register (upper nibble = 0x1). After reading or writing to MR1A (or MR1B) register, the mode register pointer will point to MR2A (or MR2B) register.

MR1A, MR1B Bits 1-0:
Character Length
0 0 = 5 (default) 1 0 = 7
0 1 = 6 1 1 = 8

MR1A, MR1B Bit-2:
In non-Multidrop mode, this bit selects the parity.
0 = Even Parity (default)
1 = Odd Parity

In Multidrop mode, this bit is the Address/Data flag.
0 = Data (default)
1 = Address

MR1A, MR1B Bit 4-3: Parity mode.
00 = With parity (default) 10 = No parity
01 = Force parity 11 = Multidrop mode

MR1A, MR1B Bit-5: Data error mode.
0 = Single Character mode (default)
1 = Block (FIFO) mode

MR1A, MR1B Bit-6.
Receive trigger levels. See description under MR0 bit-6.

MR1A, MR1B Bit-7: Receive RTS flow control.
0 = No RX RTS control function (default)
1 = Auto RX RTS control function
The output OP0 (OP1) serves as the -RTS signal for channel A (channel B). Note that MR2 A/B bit-5 also controls OP0 (OP1). Only one of MR1 bit-7 or MR2 bit-5 should be set to '1'.

MODE REGISTER 2 (MR2A, MR2B)

This register is accessed after any read or write operation to MR1A (or MR1B) register is performed. Any read or write to MR2A (or MR2B) does not change the mode register pointer. User should use one of the

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two reset MR pointer command (see Command Register) to reset the pointer to MR0 or MR1.

MR2A, MR2B Bits 3-0: Stop bit length.

0000 = 0.563 (default)	1000 = 1.563
0001 = 0.625	1001 = 1.625
0010 = 0.688	1010 = 1.688
0011 = 0.750	1011 = 1.750
0100 = 0.813	1100 = 1.813
0101 = 0.875	1101 = 1.875
0110 = 0.938	1110 = 1.938
0111 = 1.000	1111 = 2.000

MR2A, MR2B Bit-4: Auto CTS Flow control.
0 = No Auto CTS flow control (default)
1 = Auto CTS flow control enabled

MR2A, MR2B Bit-5: Auto Transmit RTS control.
0 = No Auto TX RTS control (default)
1 = Auto Transmit RTS function enabled
The output OP0 (OP1) serves as the -RTS signal for channel A (channel B). Note that only one of MR1 bit-7 or MR2 bit-5 should be set to '1'.

MR2A, MR2B Bit 7-6: Loopback mode select.
0 0 = No loopback (default)
0 1 = Automatic Echo
1 0 = Local Loopback
1 1 = Remote Loopback

STATUS REGISTER (SRA, SRB)

SRA, SRB Bit-0: Receive Ready.
This bit indicates that one or more character(s) has been received and is waiting in the FIFO for the CPU to read them. It is set when the first character is transferred from the receive shift register to the empty FIFO, and cleared when the CPU reads the receiver buffer and there are no more characters in the FIFO after the read.

SRA, SRB Bit-1: Receive FIFO Full.
This bit is set when a character is transferred from the receive shift register to the receiver FIFO and the transfer fills the FIFO. All eight (or 16 in XR88C192) FIFO locations are occupied. It is cleared when the CPU reads the receiver buffer, unless another character is in the receive shift register waiting for an empty FIFO location.

SRA, SRB Bit-2: Transmit Ready.
This bit (when set) indicates that the transmit FIFO is not full. Transmitter ready bit is set when the transmit FIFO has at least one empty location. This bit is cleared when the transmit FIFO is full.

SRA, SRB Bit-3: Transmit Empty.
This bit will be set when the channel's transmitter is empty. It indicates that both the transmit FIFO and the transmit shift register are empty. It is set after transmission of the last stop bit of the last character in the TX FIFO. It is cleared when the CPU loads a character into the transmit FIFO or when the transmitter is disabled.

SRA, SRB Bit-4: Overrun Error.
This bit is set when one or more characters in the received data stream have been lost. It is set on receipt of a valid start bit when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error, and framing error status, if any) is overwritten. A reset error status command clears this bit.

SRA, SRB Bit-5: Parity Error.
This bit is set when the “with parity” or “force parity” mode is programmed by MR1A (or MR1B) and an incoming character is received with incorrect parity. In the Multidrop mode, the parity error bit position stores the received address/data tag. This bit is valid only when the RxRDY bit is set (SRA, SRB bit-0 = 1).

SRA, SRB Bit-6: Framing Error.
This bit is set when a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position. At least one bit in the received character (data or parity) must have been a “1” to signal a framing error. After a framing error, the receiver does not wait for the line to return to the marking state (high). If the line remains low for 1/2 a bit time after the stop bit sample (that is, the nominal end of the first stop bit), the receiver treats it as the beginning of a new start bit.This bit is valid only when the RxRDY bit is set (SRA, SRB Bit-0 = 1).

SRA, SRB Bit-7: Received Break.
This bit indicates a character with all data bits being zero has been received without a stop bit. This bit is valid only when the RxRDY bit is set (SRA, SRB Bit-0 = 1). Only a single FIFO position is occupied when a break is received; for longer break signals, additional entries to the FIFO are inhibited until the channel A/B receiver serial data input line returns to the marking state. The break-detect circuitry can detect a break that starts in the middle of a received character however, the break condition must persist completely through the end of the current character and the next character time to be recognized as a break signal.

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Baud Rate Table for a 3.6864MHz clock. Data rates would double for a 7.3728MHz clock.

	MR0A Bits 2,0=0		MR0A Bit-0=1 Bit-2=0 (extended table 1)		MR0A Bit-0=0 Bit-2=1 (extended table 2)	
CSRA, CSRB Bits 7:4 or Bits 3:0	SET-1 ACR Bit-7=0	SET-2 ACR Bit-7=1	SET-1 ACR Bit-7=0	SET-2 ACR Bit-7=1	SET-1 ACR Bit-7=0	SET-2 ACR Bit-7=1
0000 (default)	50	75	300	450	4800	7200
0001	110	110	110	110	880	880
0010	134.5	134.5	134.5	134.5	1076	1076
0011	200	150	1200	900	19.2k	14.4k
0100	300	300	1800	1800	28.8k	28.8k
0101	600	600	3600	3600	57.6k	57.6k
0110	1200	1200	7200	7200	115.2k	115.2k
0111	1050	2000	1050	2000	1050	2000
1000	2400	2400	14.4k	14.4k	57.6k	57.6k
1001	4800	4800	28.8k	28.8k	4800	4800
1010	7200	1800	7200	1800	57.6k	14.4k
1011	9600	9600	57.6k	57.6k	9600	9600
1100	38.4k	19.2k	230.4k	115.2k	38.4k	19.2k
1101	Timer	Timer	Timer	Timer	Timer	Timer
1110*	IP3-16X (CSRA 3:0), IP4-16X (CSRA 7:4), IP5-16X (CSRB 3:0), IP6-16X (CSRB 7:4)					
1111*	IP3-1X (CSRA 3:0), IP4-1X (CSRA 7:4), IP5-1X (CSRB 3:0), IP6-1X (CSRB 7:4)					

* Baud Rate is independent of MR0 bit-0 & bit-2 and ACR bit-7 settings.

The product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered. (obs)

CLOCK SELECT REGISTER (CSRA, CSRB)

Transmit / Receive baud rates for channels A, B can be selected via this register.

CSRA, CSRB Bits 3-0.
Transmit clock select(see baud rate table).

CSRA, CSRB Bits 7-4.
Receive clock select (see baud rate table).

COMMAND REGISTER (CRA, CRB)

CRA, CRB register is used to supply commands to A, B channels respectively. Multiple commands can be specified in a single write to CRA, CRB as long as commands are non-conflicting.

CRA, CRB Bits 1-0: Receiver Commands.
0 0 = No Action, Stays in Present Mode (default)
0 1 = Receiver Enabled
1 0 = Receiver Disabled
1 1 = Don't Use

CRA, CRB Bits 3-2: Transmitter Commands.
0 0 = No Action, Stays in Present Mode (default)
0 1 = Transmitter Enabled
1 0 = Transmitter Disabled
1 1 = Don't Use

CRA, CRB Bits 7-4: Miscellaneous Commands.

0 0 0 0 = No Command (default).
0 0 0 1 = Reset MR Pointer to MR1.
0 0 1 0 = Reset Receiver. Receiver is disabled and FIFO is flushed.
0 0 1 1 = Reset Transmitter. Transmitter is disabled and FIFO is flushed.
0 1 0 0 = Reset Error Status. Clears channel A/B, break, parity, and over-run error bits in the status register.
0 1 0 1 = Reset Channel's Break-Change Interrupt. Clears channel A/B break detect change bit in the interrupt status register (ISR bit-2 for channel A and ISR bit-6 for channel B).

0 1 1 0 = Start Break. Forces the transmitter output to go low and stay low. If transmitter is empty the start of the break condition will be delayed up to two bit times. If transmitter is active, all the characters in the FIFO are transmitted before break signal is sent. Transmitter must to be enabled for this command to work.

0 1 1 1 = Stop Break. Transmit output will go high within two bit times.

1 0 0 0 = Set -RTS output to low (assertion).

1 0 0 1 = Reset -RTS output to high (negation).

1 01 0 = Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the receive FIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR Bit-3 is reset. (See also Watchdog timer description)

1 0 1 1 = Set MR pointer to MR0.

1 1 0 0 = Disable Timeout Mode. This command returns control of the C/T to the regular Start/Stop counter commands. It does not stop the counter or clear any pending interrupts. After disabling the timeout mode, a “Stop Counter” command should be issued to force a reset of the ISR Bit-3.

1 1 0 1 = Not used.

1 1 1 0 = Enable Power Down Mode. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a XTAL1. While in the power down mode, do not issue any commands to the CRA or CRB except the disable power down mode command. The contents of all registers will be saved while in this mode. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. *This command is in CRA only.*

1 1 1 1 = Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR A/B. For maximum power reduction all input pins should be at GND or VCC. *This command is in CRA only.*

RECEIVE BUFFER (RXA, RXB)

The receive buffer consists of a 8-characters deep FIFO in XR68C92 and 16-characters deep FIFO in XR68C192. The received characters are transferred from the shift register one at a time to the FIFO and are stored there until read by the CPU or flushed by a reset receiver command.

TRANSMIT BUFFER (TXA, TXB)

The transmit buffer consists of a 8-characters deep FIFO in XR68C92 and 16-characters deep FIFO in XR68C192. Once loaded in the FIFO, the characters are transferred to the transmit shift register one at a time and transmitted unless the transmitter is disabled.

INPUT PORT CHANGE REGISTER (IPCR)

This is a read-only register which gives the state and the change-of-state information of the multi-purpose inputs IP0, IP1, IP2 and IP3.

IPCR Bits 3-0: Levels of IP3 - IP0.
These show the current state of IP3, IP2, IP1 and IP0 respectively.
0 = Low
1 = High

IPCR Bits 7-4: Transitions of IP3 - IP0.
These indicate if there has been a change of state in IP3, IP2, IP1 and IP0 respectively. They are cleared when the register is read by the CPU.
0 = No
1 = Yes

AUXILIARY CONTROL REGISTER (ACR)

ACR Bits 3-0:
This field selects which bits of the input port change register (IPCR) cause the interrupt status register (ISR) bit-7 to be set. For example, if bit-0 = 1, then a change of state in IP0 will set ISR bit-7. If bit-0 and bit-2 are both '1', then whenever IP0 or IP2 changes state, ISR bit-7 will be set.

0 = Disabled (default)
1 = Enabled

ACR Bits 6-4:
Counter/Timer Mode and Clock Source. These bits should not be altered while the C/T is in use. Prior to changing these bits, the C/T must be stopped if in counter mode. If the C/T is in timer mode, its output

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must be disabled and its interrupt must be masked. The following table shows how to select the clock source for the C/T when used in counter mode or timer mode:

ACR Bit-7: Baud rate table Select.
This bit is used to select between two sets of baud rate tables. See Baudrate table on Page 18. It should be changed only after both channels have been reset and disabled.
0 = Set 1
1 = Set 2

ACR Bits 6:4	C/T Mode	Clock Source
0 0 0	Counter	External (IP2)
0 0 1	Counter	TXAClk1-Transmit A 1X clock
0 1 0	Counter	TXBClk1-Transmit B 1X clock
0 1 1	Counter	Crystal or External Clock (XTAL1/Clk) Divided by 16
1 0 0	Timer	External (IP2)
1 0 1	Timer	External (IP2) Divided by 16
1 1 0	Timer	Crystal or External Clock (XTAL1/Clk)
1 1 1	Timer	Crystal or External Clock (XTAL1/Clk) Divided by 16

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INTERRUPT STATUS REGISTER (ISR)

This register provides the status of all potential interrupt sources. The contents of this register are logically “AND”-ed with the contents of the interrupt mask register, and the results are “OR”-ed. The resulting signal is inverted to produce the -INT output. *All active interrupt sources are visible by reading the ISR, regardless of the contents of the interrupt mask register.* Reading the ISR has no effect on any interrupt source. Each active interrupt source must be cleared in a source-specific fashion to clear the ISR. All interrupt sources are cleared when the XR68C92/192 is reset.

ISR Bit-0: Transmit ready A.
This bit is set when channel A's transmit buffer (FIFO) is filled below the programmed transmit trigger level (see MR0A bits 5-4). For example, if a TX trigger level of '4' is chosen, this bit will be set whenever the TX FIFO has four or more empty locations. This bit can be cleared by loading the TX FIFO above the trigger level.

ISR Bit-1: Receive ready A .
This bit is set when channel A's receive buffer (FIFO) is filled above the programmed receive trigger level condition (see MR0A bit-6 and MR1A bit-6). For example, if a RX trigger level of '6' is chosen, this bit will be set whenever the RX FIFO contains six or more bytes. This bit can be cleared by reading the data out of the FIFO till it falls below the trigger level.

ISR Bit-2: Channel A change in break.
This bit is set when channel A receiver detects the beginning or the end of a break condition. It is reset when the CPU issues a channel A reset break change interrupt command (CRA bits 7-4 = 0x5).

ISR Bit-3: Counter/Timer (C/T) ready.
In counter mode, this bit is set when the C/T reaches terminal count. In timer mode, this bit is set each time the C/T output switches from low to high (rising edge - see Figure 2). In either mode, this bit is cleared by a stop counter command.

ISR Bit-4: Transmit ready B.
This bit is set when channel B's transmit buffer (FIFO) is filled below the programmed transmit trigger level (see MR0B bits 5-4). For example, if a TX trigger level of '4' is chosen, this bit will be set whenever the TX FIFO has four or more empty locations. This bit can be cleared by loading the TX FIFO above the trigger level.

ISR Bit-5: Receive ready B.
This bit is set when channel B's receive buffer (FIFO) is filled above the programmed receive trigger level condition (see MR0B bit-6 and MR1B bit-6). For example, if a RX trigger level of '6' is chosen, this bit will be set whenever the RX FIFO contains six or more bytes. This bit can be cleared by reading the data out of the FIFO till it falls below the trigger level.

ISR Bit-6. Channel B change in break.
This bit is set when channel B receiver detects the beginning or the end of a break condition. It is reset when the CPU issues a channel B reset break change interrupt command (CRB bits 7-4 = 0x5).

ISR Bit-7. Input port change status.
This bit is set when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs, and that event has been enabled to cause an interrupt by programming ACR Bits 3-0. This bit is cleared when the CPU reads the input port change register.

INTERRUPT MASK REGISTER (IMR)

This register selects which bits in the interrupt status register can cause an interrupt output. If a bit in the interrupt status register is a “1” and the corresponding bit in this register is also a “1”, the -INT output will be asserted. If the corresponding bit in this register is a zero, the state of the bit in the interrupt status register has no effect on the -INT output. Note that the interrupt mask register does not have any effect on the programmable interrupt outputs OP7 through OP3 or the value read from the interrupt status register.
0 = Interrupt output (-INT) disabled (default)
1 = Enable interrupt output for the event controlled by the corresponding bit in ISR.

COUNTER / TIMER REGISTERS

The Preload value Upper (***CTPU***) and Lower (***CTPL***) registers hold the most-significant byte and the least-significant byte, respectively, of the value to be used by the C/T (in both counter and timer modes). The C/T Upper (***CUR***) and Lower Registers (***CLR***) give the current value of the C/T, at the time they are read. In the counter mode, the CUR and CLR should only be read when the counter is stopped. Upon receiving a start command after a stop command, the counter starts a fresh cycle and begins counting down from the original (preload) value written to CTPU and CTPL. Also changing the value of these registers does not take effect till the current cycle is stopped and a subsequent start command is issued.

In the timer mode, the CUR and CLR registers cannot be read by the CPU. A stop command will not stop the timer, but will only clear the counter ready status bit in ISR (bit-3). Changing the value of the CTPU and CTPL registers when the timer is running will change the waveform after the current half-period of the square wave. For more details, see the Counter/Timer section.

GENERAL PURPOSE REGISTER (GPR)

This is a general purpose scratchpad register which can be used to store and retrieve one byte of user infomation.

INPUT PORT REGISTER - Read Only

The current state of the multi-purpose inputs (IP0-IP6) can be read via this register.

IPR Bit 0-5:
0 = Inputs are in low state.
1 = Inputs are in high state.

IPR Bit 6-7:
Not used and set to “0”.

OUTPUT PORT CONFIGURATION REGISTER (OPCR) - Write Only

This register selects following options for the multi-purpose outputs OP2 to OP7. Alternate functions of OP1 and OP0 are controlled by the mode registers, not the OPCR. MR1A Bit-7 and MR2A Bit-5 control OP0. MR1B Bit-7 and MR2B Bit-5 control OP1. For more details on these, see 'Multi-purpose Outputs' on page 8.

OP2 Output Select

Bit-1	Bit-0	
0	0	Controlled by SOPR and ROPR (default)
0	1	TxAClk16-Transmit A 16X clock
1	0	TxAClk1-Transmit A 1X clock
1	1	RxAClk1- Receive A 1X clock

OP3 Output Select

Bit-3	Bit-2	
0	0	Controlled by SOPR and ROPR (default)
0	1	C/T Output
1	0	TxBClk1-Transmit B 1X clock
1	1	RxBClk1- Receive B 1X clock

If OP3 is to be used for the timer output (a square wave of the programmed frequency), program the counter/timer for timer mode (ACR Bit-6 = 1), initialize the counter/timer pre-load registers (CTPU and CTPL), and read the 'Start C/T Command Register' (STCR) before setting OPCR Bits 3-2 = 01. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. The output becomes high again when the counter is stopped by a stop counter command.

OP4 output select (Bit 4):
0 = Controlled by SOPR and ROPR (default)
1 = -RxARDY which is the complement of ISR bit-1

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OP5 output select (Bit 5):
0 = Controlled by SOPR and ROPR (default)
1 = -RxBRDY which is the complement of ISR bit-5

OP6 output select (Bit 6):
0 = Controlled by SOPR and ROPR (default)
1 = -TxARDY which is the complement of ISR bit-0

OP7 output select (Bit 7):
0 = Controlled by SOPR and ROPR (default)
1 = -TxBRDY which is the complement of ISR bit-4

START COUNTER/TIMER REGISTER (STCR) - Read Only

Reading from this register will start the C/T. Data values returned should be ignored.

STOP COUNTER/TIMER REGISTER (SPCR) - Read Only

Reading from this register will stop the C/T. Data values returned should be ignored.

SET OUTPUT PORT REGISTER (SOPR) - Write Only

Output ports (OP0-OP7), when used as general purpose outputs, can be asserted (set to low) by writing a "1" to the corresponding bit in this register. Once an output is asserted, it can be negated only by issuing a command through the Reset Output Port Register (see below).

However, note that SOPR and ROPR cannot be used to assert and negate outputs that are programmed for alternate functions (see description under OPCR). For example, if OP0 is programmed to output -RTSA (see 'Configuring Multi-purpose Outputs), it cannot be controlled by SOPR or ROPR. In that case, commands from the Command Register should be issued to assert (CRA bits 7:4 = 0x8) and negate (CRA bits 7:4 = 0x9) OP0.

SOPR Bit 0-7:
0 = No change (same state).
1 = Assert the corresponding output (Set it low).

RESET OUTPUT PORT REGISTER (ROPR) - Write Only

Each output port bit can be changed to high state by writing a "1" to each individual bit.

ROPR Bit 0-7:
0 = No change (same state).
1 = Negate the corresponding output (Set it high).

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PROGRAMMING EXAMPLES

The following examples show how to initialize the XR68C92/192 for various operating conditions:

A) The first example will initialize channel A of an XR68C92 device for regular RX/TX. The operating parameters will be 9600 baud, 8 word length, no parity and 1 stop bit.

Operation	Register	Value	Remarks
Write	CRA	0x20	; reset RX (receiver)
Write	CRA	0x30	; reset TX (transmitter)
Write	CRA	0x40	; reset error status
Write	CRA	0xB0	; reset MR pointer to MR0
Write	MR0A	0x00	; use normal baud rate table. Now MR pointer points to MR1
Write	MR1A	0x13	; select word length & parity. Now MR pointer points to MR2
Write	MR2A	0x07	; normal mode (not loopback) & 1 stop bit
Write	CSRA	0xBB	; 9600 baud for RX & TX - clock source is XTAL1
Write	CRA	0x05	; enable RX & TX
Read	SRA		; should get a value 0x0C

B) This example will show how to use hardware flow control for both RX (RTS via OP0) and TX (CTS via IP0):

Write	CRA	0x10	; reset MR pointer to MR1
Write	MR1A	0x93	; select auto RTS control. The -RTS signal is sent via output OP0
Write	MR2A	0x17	; select auto CTS control. The input IP0 serves as the -CTS signal

C) This example will configure clock sources for TX and RX of both channels and C/T. Specifically, XTAL1 will be used as channel A's TX clock; IP4 as channel A's 16X RX clock; IP5 as channel B's 1X TX clock and XTAL1 as channel B's RX clock. Also, the C/T will be initialized in the timer mode and IP2 will be used as its clock source. Some of these will be programmed to appear at the multi-purpose output pins:

Write	ACR	0x40	; C/T initialized in timer mode & IP2 chosen as its clock source
			; also, bit-7 = 0, therefore baud rate Set1 has been selected
Write	CTPU	0x00	; It is essential to program CTPU & CTPL before programming OP3
Write	CTPL	0x05	; as C/T output (see below)
Write	CSRA	0xEB	; channel A RX clock source: IP4-16X, TX clock source: XTAL1 (if MR0A
			; bits 2 and 0 = 0, the TX baud rate is 9600)
Write	CSRB	0xBF	; channel B RX clock source: XTAL1 (9600 baud), TX clock source: IP5-1X
Read	STCR		; Start the C/T
Write	OPCR	0x06	; C/T output appears at OP3 and channel A's TX 1X clock (this is XTAL1
			; clock divided by 16) at OP2.

D) The next example will show how to configure and run channel B's transmitter in a multi-drop application. Note that all other relevant parameters should be configured already, like baud rate etc.

Write	CRB	0x10	; reset MR pointer to MR1
Write	MR1B	0x1B	; word length = 8 and use A/D tag in the place of parity
Write	CRB	0x04	; Enable transmitter of channel B
Write	TXB	address	; Send the address first (A/D tag = 1)
Write	CRB	0x10	; reset MR pointer to MR1
Write	MR1B	0x13	; change A/D tag = 0
Write	TXB	data	; You can load the data (A/D tag = 0) immediately after the address. There is no
			; need to wait till the transmitter is empty. Load all the data. Check to see if the
Read	SRB		; transmitter is empty & ready. You need to do this before you can load the next
			; address. Repeat the last 5 steps to load different addresses and their data.

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS FOR XR68C92 AND XR68C192

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

Symbol	Parameter	Limits 3.3 Min	Limits 3.3 Max	Limits 5.0 Min	Limits 5.0 Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock input high level (Devices with top marking of "CC" and older)	2.4	VCC	3.0	VCC	V	
V_{IHCK}	Clock input high level (Devices with top marking of "D2" and newer)	2.4	5.5	3.0	5.5	V	
V_{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input high level (Devices with top marking of "CC" and older)	2.0	VCC	2.2	VCC	V	
V_{IH}	Input high level (Devices with top marking of "D2" and newer)	2.0	5.5	2.2	5.5	V	
V_{OL}	Output low level on all outputs				0.4	V	I_{OL}= 8 mA
V_{OL}	Output low level on all outputs		0.4			V	I_{OL}= 5 mA
V_{OH}	Output high level			2.4		V	I_{OH}= -8 mA
V_{OH}	Output high level	2.4				V	I_{OH}= -1 mA
I_{IL}	Input leakage		±10		±10	µA	
I_{CL}	Clock leakage		±10		±10	µA	
I_{CC}	Avg power supply current		1.0*		1.5*	mA	
I_{PD}	Avg power-down supply current (68C92)		100*		150*	µA	
I_{PD}	Avg power-down supply current (68C192)		200*		300*	µA	
C_P	Input capacitance		5		5	pF	

*All inputs tied to VCC/GND.

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{1w},T_{2w}	Clock pulse duration	17		17		ns	
T_{3w}	Oscillator/Clock frequency		8		24	MHz	
T_{AS}	Address Valid to -CS Low	0		0		ns	
T_{AH}	-CS High to Address Invalid	0		0		ns	
T_{RWS}	R/-W Setup Time to -CS Low	0		0		ns	
T_{RWH}	R/-W Hold Time from -CS High	0		0		ns	
T_{DD}	-CS/-IACK Low to Data Valid (Read)		51		32	ns	
T_{DS}	Data Valid to -CS High (Write)	20		10		ns	
T_{DH}	-CS High to Data Invalid (Write)	1		1		ns	
T_{DF}	-CS/-IACK High to Data Hi-Z (Read)		30		20	ns	
T_{CSL}	-CS Low Pulse Width	100		70		ns	
T_{CSH}	-CS High Pulse Width	100		70		ns	
T_{AKL}	-CS/-IACK Low to -DACK Low		70		42	ns	
T_{AKH}	-CS/-IACK High to -DACK High		45		27	ns	
T_{AKT}	-CS/-IACK High to -DACK Hi-Z		70		43	ns	
T_{9s}	Port input setup time	0		0		ns	
T_{9h}	Port input hold time	0		0		ns	
T_{10d}	Delay from R/-W to output		110		110	ns	
T_{11d}	Delay to reset interrupt from -CS		100		100	ns	
T_R	Reset pulse width	2		2		clks*	
N	Baud rate divisor	1	2^{16}-1	1	2^{16}-1	N/A	

* number of input clock (crystal or external clock) periods

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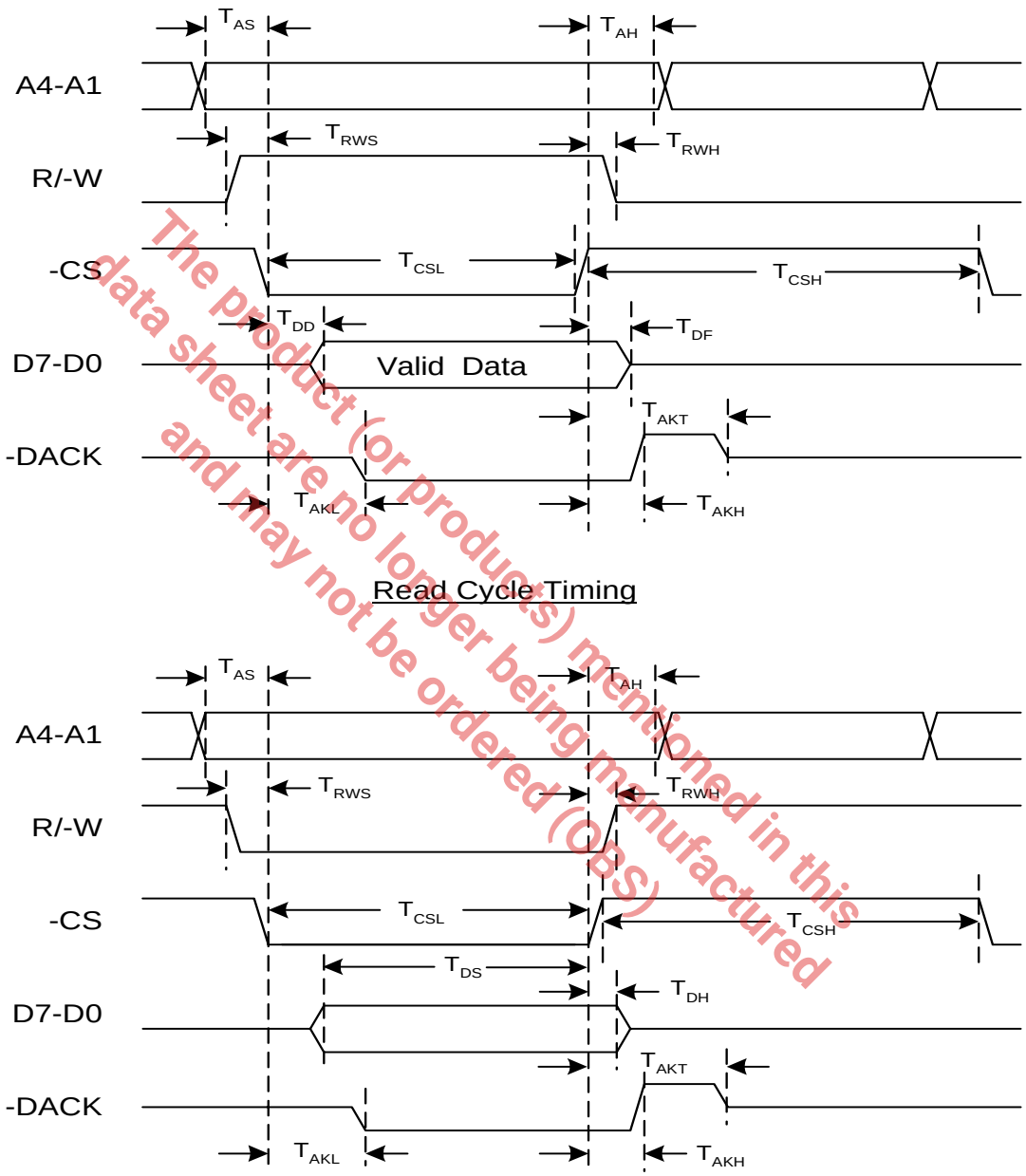

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Figure 3: Bus Timing (Read/Write cycle)

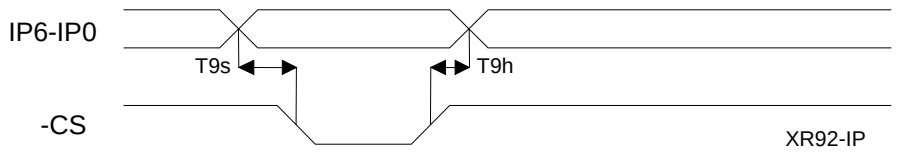

Figure 4: Input Port Timing

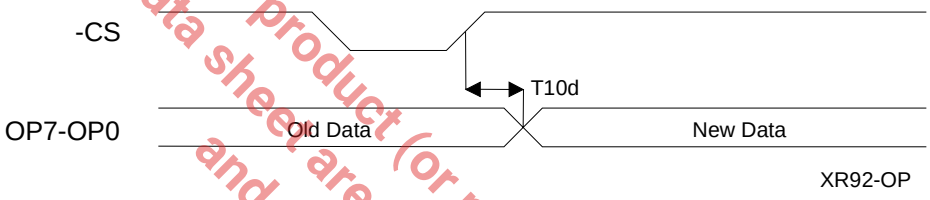

Figure 5: Output Port Timing

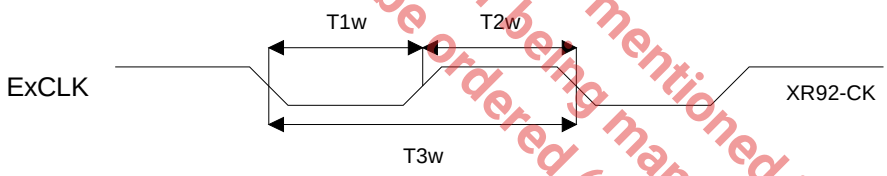

Figure 6: External clock Timing

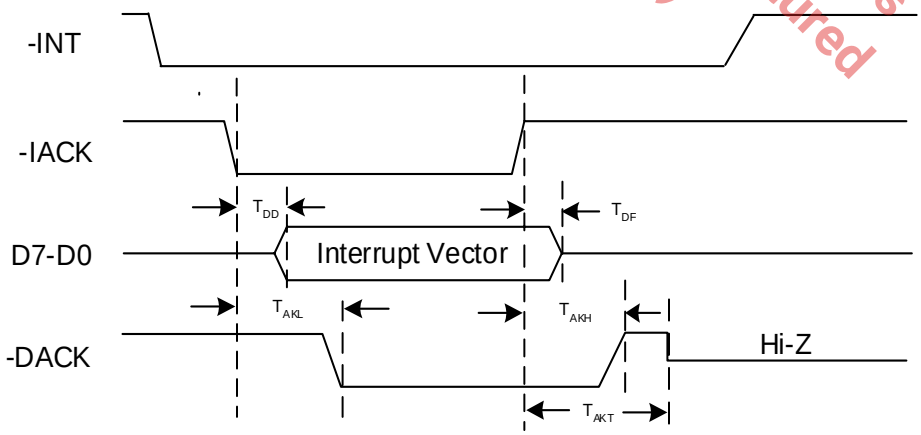

Figure 7: Interrupt Timing

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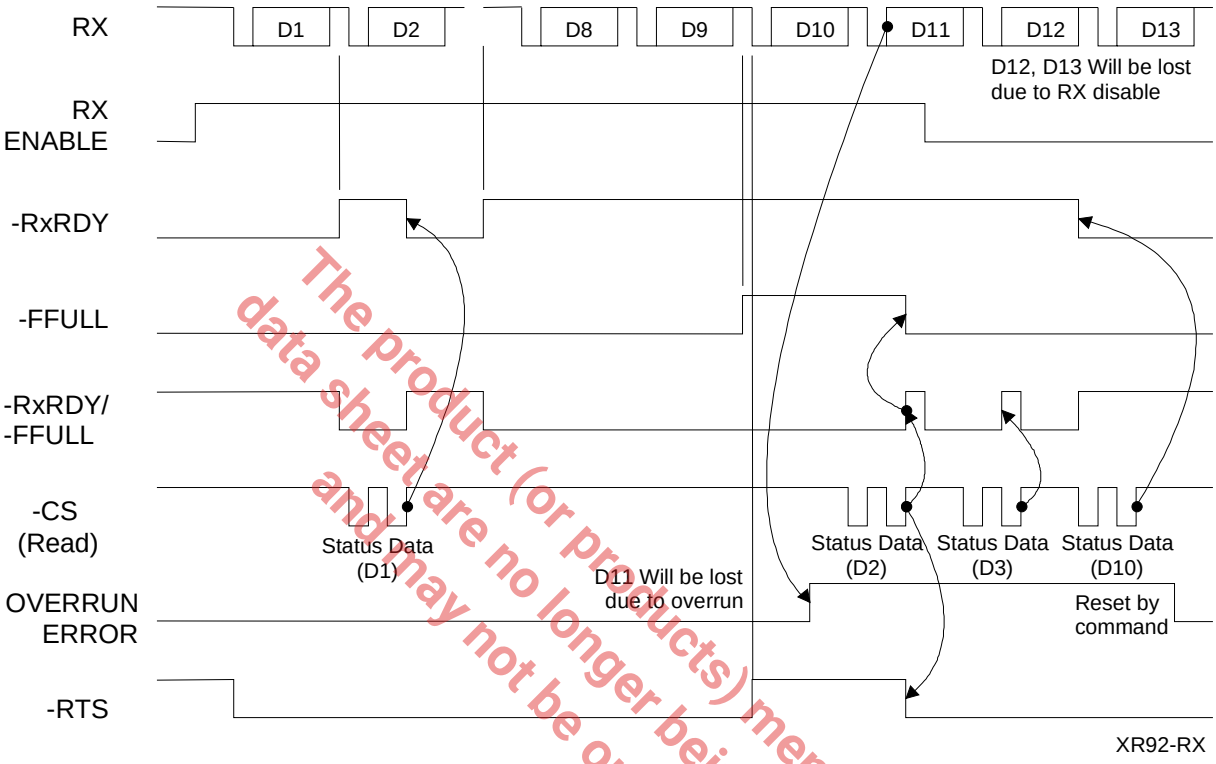

Figure 8: Receive Timing

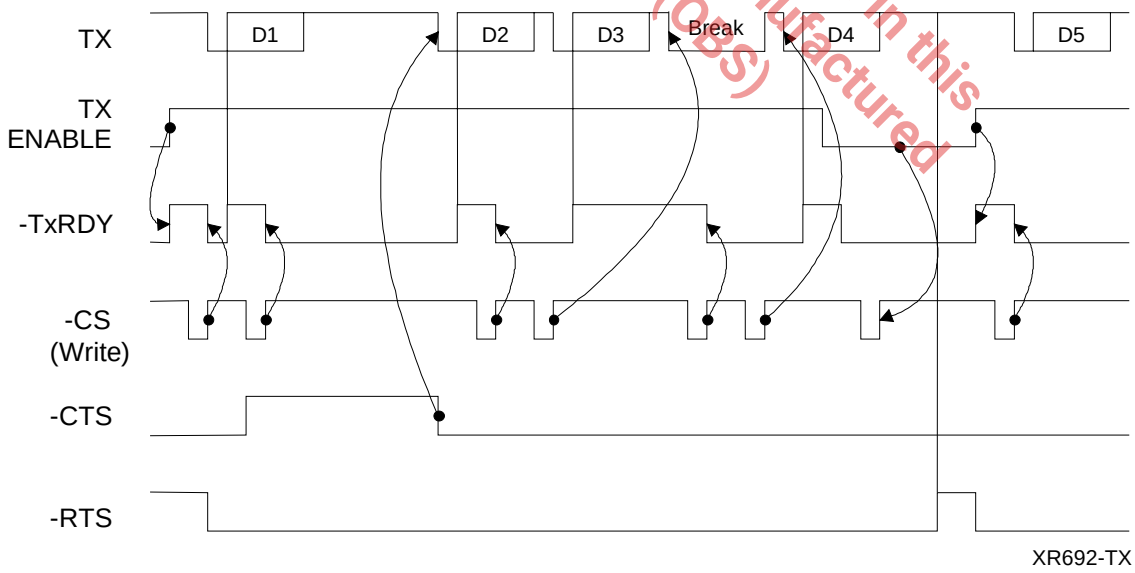

Figure 9: Transmit Timing

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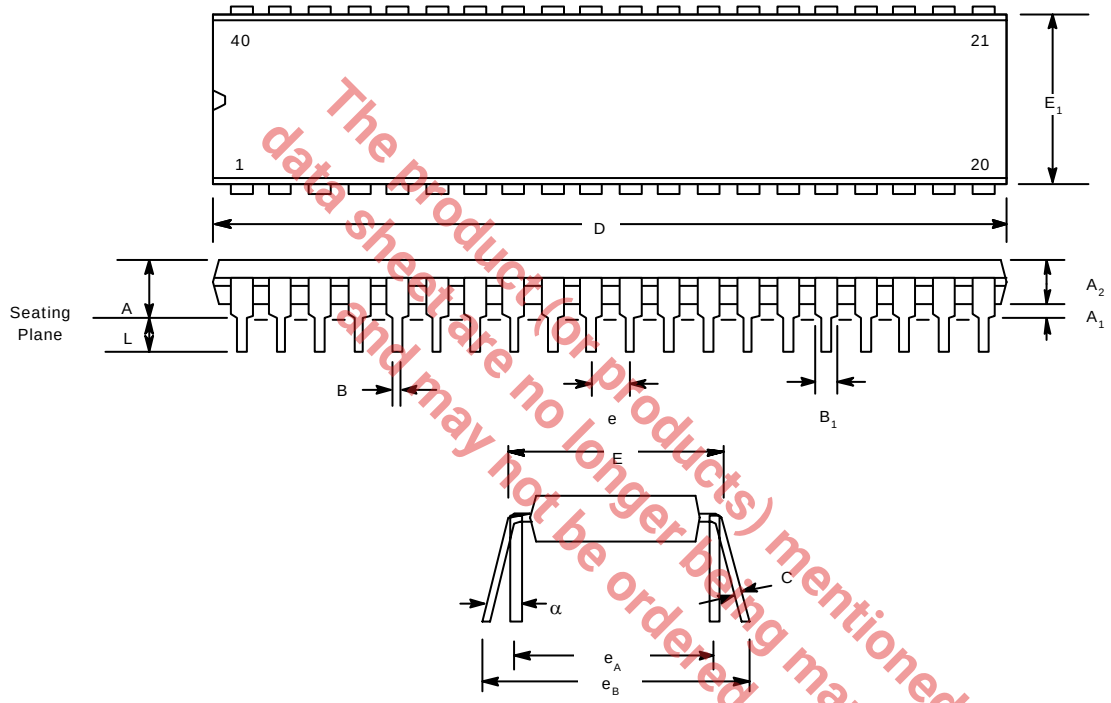
PACKAGE OUTLINE DRAWING

40 LEAD PLASTIC DUAL-IN-LINE
(PDIP)



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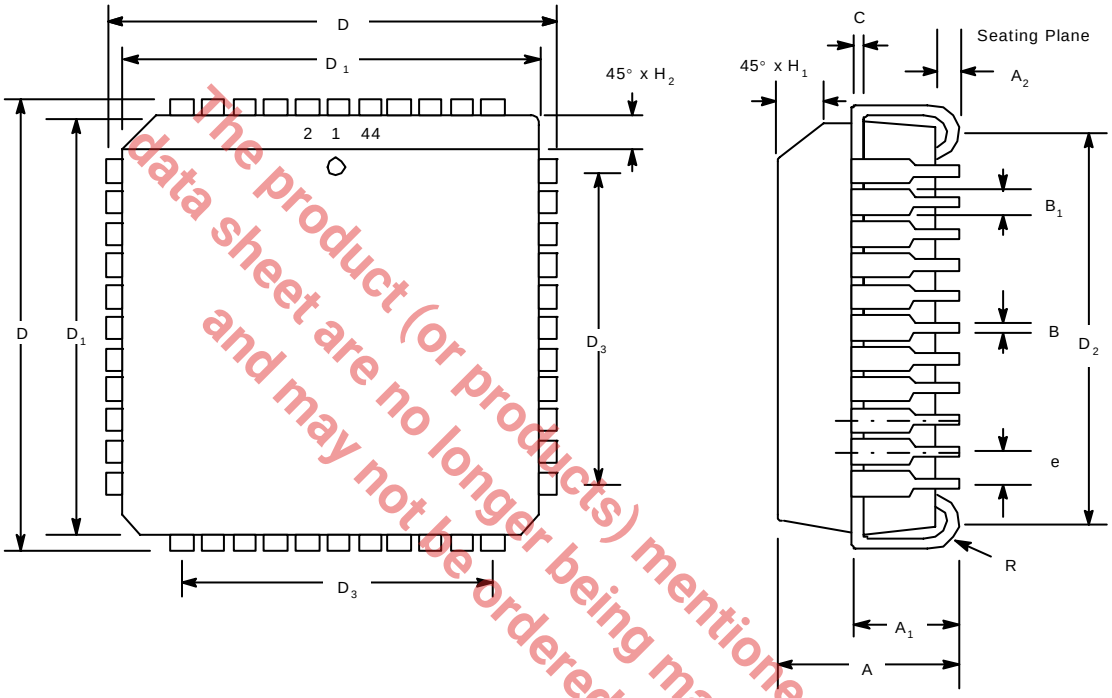
Note: The control dimension is the inch column				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.250	4.06	6.35
A_1	0.015	0.070	0.38	1.78
A_2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.980	2.095	50.29	53.21
E	0.600	0.625	15.24	15.88
E_1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0^0	15^0	0^0	15^0

PACKAGE OUTLINE DRAWING

44LEAD PLASTIC LEADED CHIP CARRIER (PLCC)



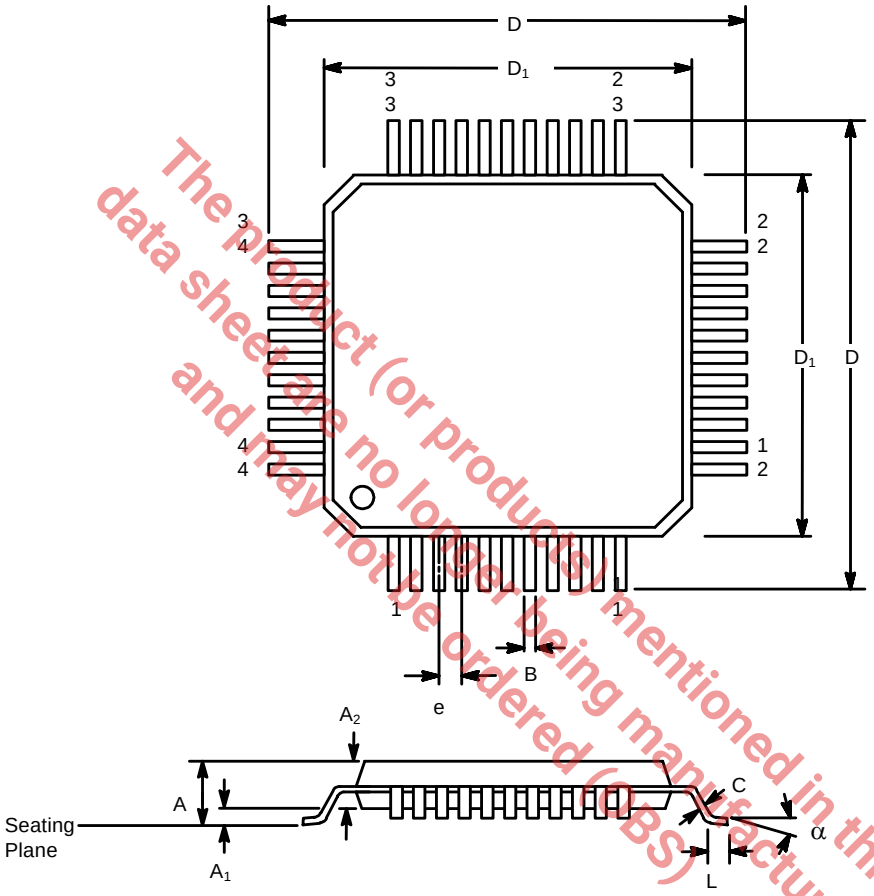
The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Note: The control dimension is the inch column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	-----	0.51	------
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ		12.70 typ	
e	0.50 BSC		1.27BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

PACKAGE OUTLINE DRAWING

44 LEAD LOW-PROFILE QUAD FLAT PACK (LQFP)



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Note: The control dimension is the inch column				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D_1	0.390	0.398	9.90	10.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0^0	7^0	0^0	7^0

EXPLANATION OF DATA SHEET REVISIONS:

FROM	TO	CHANGES	DATE
1.20	1.30	Added and updated Device Status to front page. Added 5V tolerant input descriptions. Clarified Programming example D. Clarified SRA, SRB Bit-2 description.	August 2003
1.30	1.31	Clarified that 5V tolerant inputs are only for devices with top marking of "D2" and newer. Devices with top marking of "CC" or newer do not have 5V tolerant inputs.	Sept 2003
1.31	1.32	Clarified that Extended Baud Rate Tables can only be selected via MR0A for both channels.	February 2005
1.32	1.33	Removed discontinued packages in Ordering Information. Updated the 1.4mm-thick Quad Flat Pack package description from "TQFP" to "LQFP" to be consistent with JEDEC and Industry norms.	August 2005

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