GENERAL DESCRIPTION

The XR16V654[1] (V654) is an enhanced quad Universal Asynchronous Receiver and Transmitter (UART) each with 64 bytes of transmit and receive FIFOs, programmable transmit and receive FIFO trigger levels, automatic hardware and software flow control, and data rates of up to 16 Mbps at 4X sampling rate. Each UART has a set of registers that provide the user with operating status and control, receiver error indications, and modem serial interface controls. An internal loopback capability allows onboard diagnostics. The V654 is available in a 48-pin QFN, 64-pin LQFP, 68-pin PLCC, 80-pin LQFP and 100-pin QFP packages. The 64-pin and 80-pin packages only offer the 16 mode interface, but the 48, 68 and 100 pin packages offer an additional 68 mode interface which allows easy integration with Motorola processors. The XR16V654IV (64-pin) offers three state interrupt output while the XR16V654DIV provides continuous interrupt output. The 100 pin package provides additional FIFO status outputs (TXRDY# and RXRDY# A-D), separate infrared transmit data outputs (IRTX A-D) and channel C external clock input (CHCCLK). The XR16V654 is compatible with the industry standard ST16C554 and ST16C654/654D.

NOTE: 1 Covered by U.S. Patent #5,649,122.

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FEATURES

- Pin-to-pin compatible with ST16C454, ST16C554, TI's TL16C754B and Philip's SC16C654B
- Intel or Motorola Data Bus Interface select
- Four independent UART channels
  - Register Set Compatible to 16C550
  - Data rates of up to 16 Mbps
  - 64 Byte Transmit FIFO
  - 64 Byte Receive FIFO with error tags
  - 4 Selectable TX and RX FIFO Trigger Levels
  - Automatic Hardware (RTS/CTS) Flow Control
  - Automatic Software (Xon/Xoff) Flow Control
  - Progammable Xon/Xoff characters
  - Wireless Infrared (IrDA 1.0) Encoder/Decoder
  - Full modem interface
- 2.25V to 3.6V supply operation
- Sleep Mode with automatic wake-up
- Crystal oscillator or external clock input

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FIGURE 1. XR16V654 BLOCK DIAGRAM

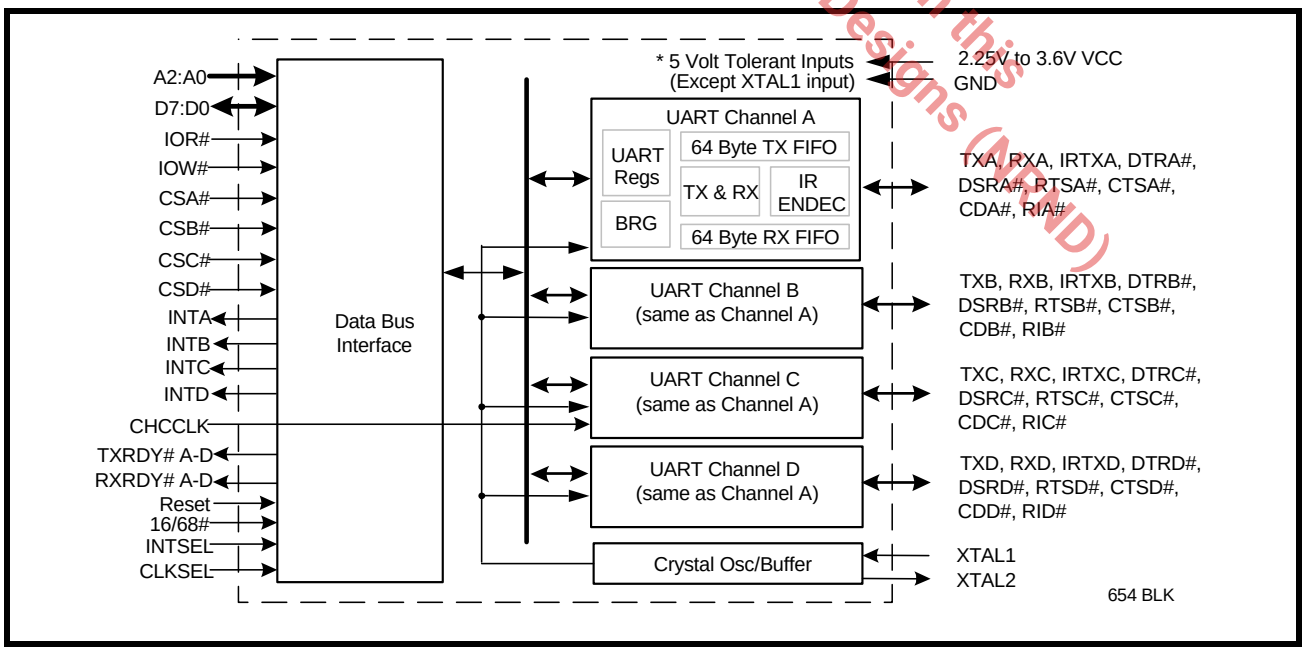

FIGURE 2. PIN OUT ASSIGNMENT FOR 100-PIN QFP PACKAGES IN 16 AND 68 MODE

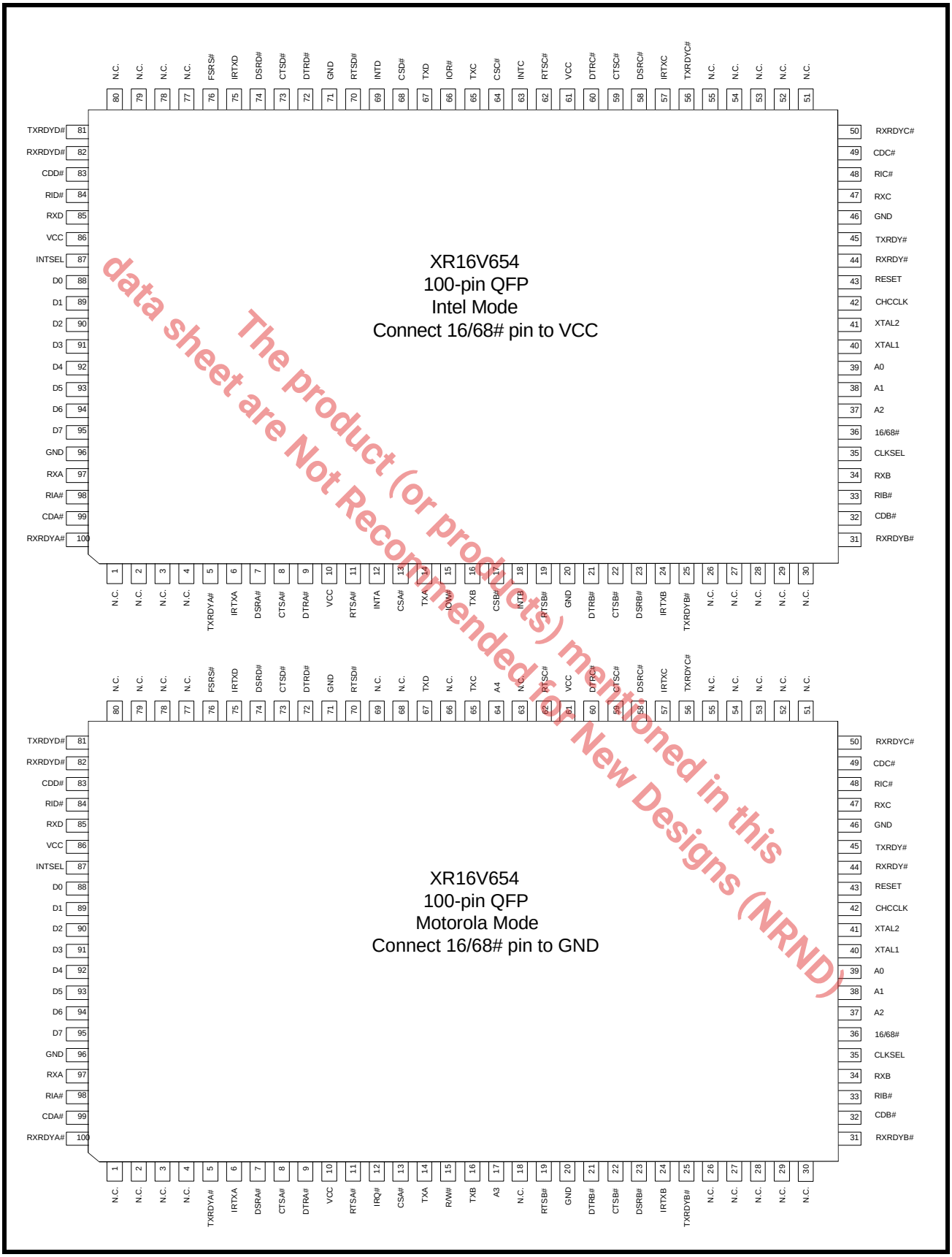

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FIGURE 3. PIN OUT ASSIGNMENT FOR 68-PIN PLCC PACKAGES IN 16 AND 68 MODE AND 64-PIN LQFP PACKAGES

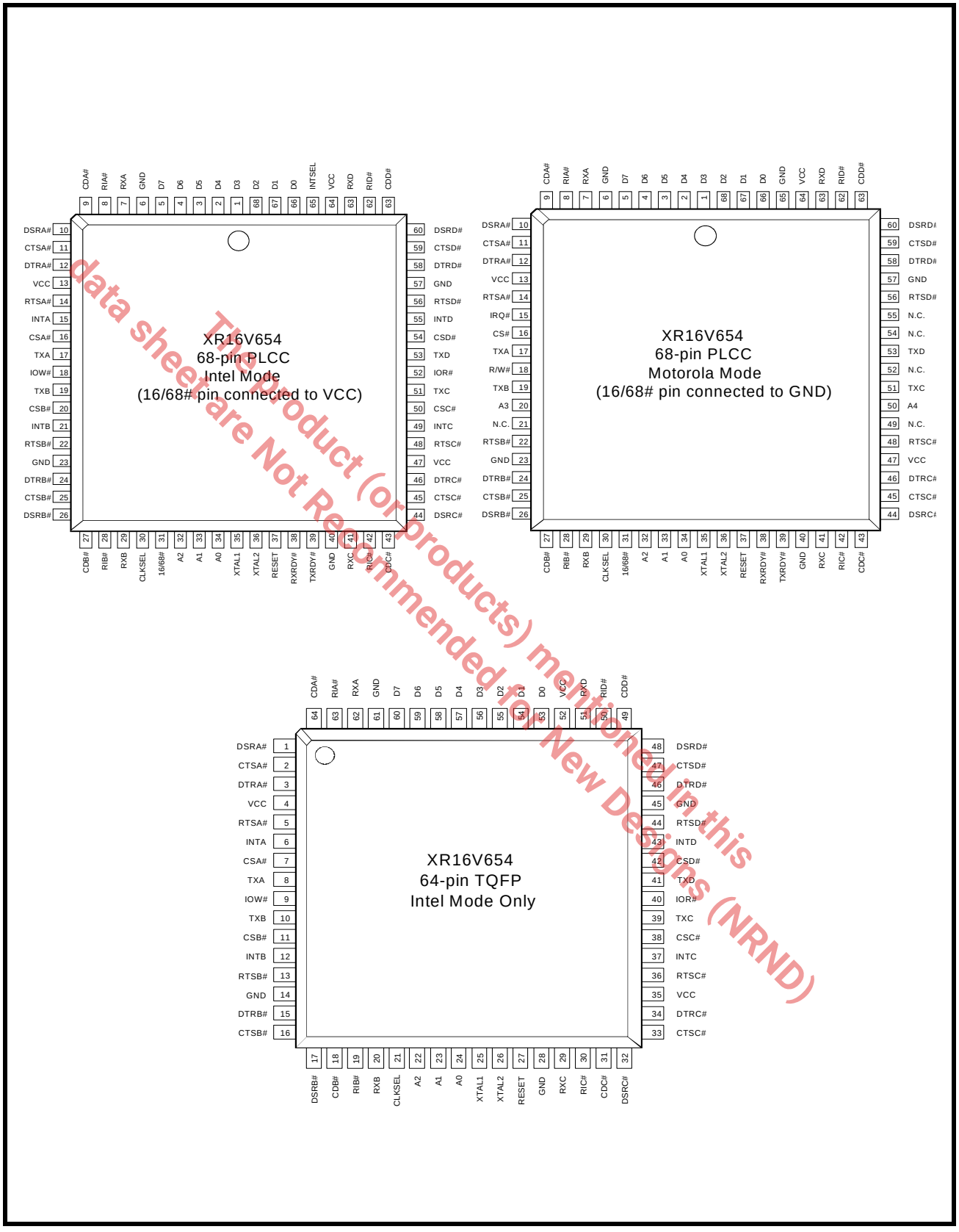

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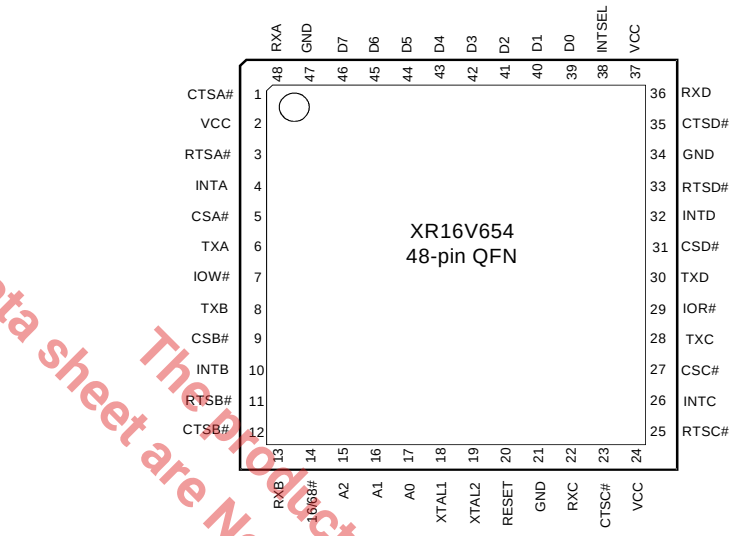
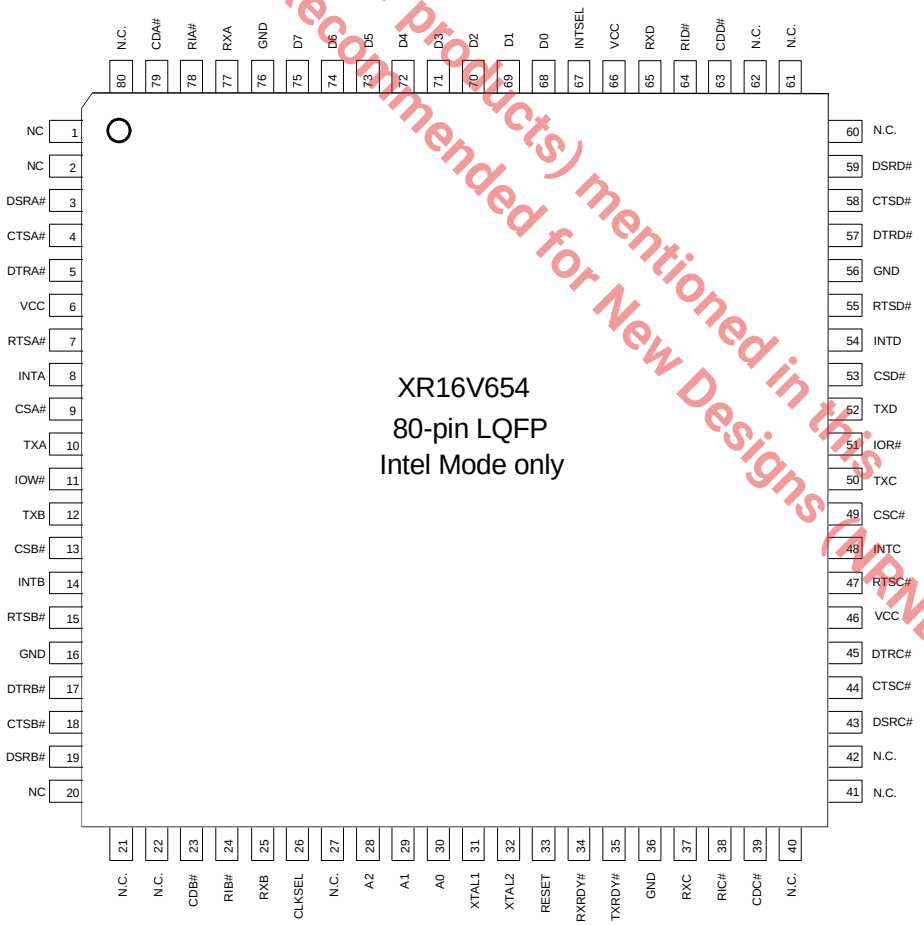
FIGURE 4. PIN OUT ASSIGNMENT FOR 48-PIN QFN PACKAGE AND 80-PIN LQFP PACKAGE





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ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16V654IJ	68-Lead PLCC	-40°C to +85°C	Active
XR16V654IV	64-Lead LQFP	-40°C to +85°C	Active
XR16V654DIV	64-Lead LQFP	-40°C to +85°C	Active
XR16V654IQ	100-Lead QFP	-40°C to +85°C	Active
XR16V654IL	48-pin QFN	-40°C to +85°C	Active
XR16V654IV80	80-Lead LQFP	-40°C to +85°C	Active

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PIN DESCRIPTIONS

Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN#	80-LQFP PIN #	100-QFP PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE							
A2 A1 A0	15 16 17	22 23 24	32 33 34	28 29 30	37 38 39	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A-D during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	46 45 44 43 42 41 40 39	60 59 58 57 56 55 54 53	5 4 3 2 1 68 67 66	75 74 73 72 71 70 69 68	95 94 93 92 91 90 89 88	I/O	Data bus lines [7:0] (bidirectional).
IOR# (VCC)	29	40	52	51	66	I	When 16/68# pin is HIGH, the Intel bus interface is selected and this input becomes read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When 16/68# pin is LOW, the Motorola bus interface is selected and this input is not used and should be connected to VCC.

Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN#	80-LQFP PIN #	100-QFP PIN #	TYPE	DESCRIPTION
IOW# (R/W#)	7	9	18	11	15	I	When 16/68# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is LOW, the Motorola bus interface is selected and this input becomes read (logic 1) and write (logic 0) signal.
CSA# (CS#)	5	7	16	9	13	I	When 16/68# pin is HIGH, this input is chip select A (active low) to enable channel A in the device. When 16/68# pin is LOW, this input becomes the chip select (active low) for the Motorola bus interface.
CSB# (A3)	9	11	20	13	17	I	When 16/68# pin is HIGH, this input is chip select B (active low) to enable channel B in the device. When 16/68# pin is LOW, this input becomes address line A3 which is used for channel selection in the Motorola bus interface.
CSC# (A4)	27	38	50	49	64	I	When 16/68# pin is HIGH, this input is chip select C (active low) to enable channel C in the device. When 16/68# pin is LOW, this input becomes address line A4 which is used for channel selection in the Motorola bus interface.
CSD# (VCC)	31	42	54	53	68	I	When 16/68# pin is HIGH, this input is chip select D (active low) to enable channel D in the device. When 16/68# pin is LOW, this input is not used and should be connected VCC.
INTA (IRQ#)	4	6	15	8	12	O (OD)	When 16/68# pin is HIGH for Intel bus interface, this ouput becomes channel A interrupt output. The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode when MCR[3] is set to a logic 1. INTA is set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3]. When 16/68# pin is LOW for Motorola bus interface, this output becomes device interrupt output (active low, open drain). An external pull-up resistor is required for proper operation.

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Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN#	80-LQFP PIN #	100-QFP PIN #	TYPE	DESCRIPTION
INTB INTC INTD (N.C.)	10 26 32	12 37 43	21 49 55	14 48 54	18 63 69	O	When 16/68# pin is HIGH for Intel bus interface, these ouputs become the interrupt outputs for channels B, C, and D. The output state is defined by the user through the software setting of MCR[3]. The interrupt outputs are set to the active mode when MCR[3] is set to a logic 1 and are set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3]. When 16/68# pin is LOW for Motorola bus interface, these outputs are unused and will stay at logic zero level. Leave these outputs unconnected.
INTSEL	38	-	65	67	87	I	Interrupt Select (active high, input with internal pull-down). When 16/68# pin is HIGH for Intel bus interface, this pin can be used in conjunction with MCR bit-3 to enable or disable the INT A-D pins or override MCR bit-3 and enable the interrupt outputs. Interrupt outputs are enabled continuously when this pin is HIGH. MCR bit-3 enables and disables the interrupt output pins. In this mode, MCR bit-3 is set to a logic 1 to enable the continuous output. See MCR bit-3 description for full detail. This pin must be LOW in the Motorola bus interface mode. For the 64 pin packages, this pin is bonded to VCC internally in the XR16V654D so the INT outputs operate in the continuous interrupt mode. This pin is bonded to GND internally in the XR16V654 and therefore requires setting MCR bit-3 for enabling the interrupt output pins.
TXRDYA# TXRDYB# TXRDYC# TXRDYD#	- - - -	- - - -	- - - -	- - - -	5 25 56 81	O	UART channels A-D Transmitter Ready (active low). The outputs provide the TX FIFO/THR status for transmit channels A-D. See Table 5. If these outputs are unused, leave them unconnected.
RXRDYA# RXRDYB# RXRDYC# RXRDYD#	- - - -	- - - -	- - - -	- - - -	100 31 50 82	O	UART channels A-D Receiver Ready (active low). This output provides the RX FIFO/RHR status for receive channels A-D. See Table 5. If these outputs are unused, leave them unconnected.
TXRDY#	-	-	39	35	45	O	Transmitter Ready (active low). This output is a logically ANDed status of TXRDY# A-D. See Table 5. If this output is unused, leave it unconnected.
RXRDY#	-	-	38	34	44	O	Receiver Ready (active low). This output is a logically ANDed status of RXRDY# A-D. See Table 5. If this output is unused, leave it unconnected.

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Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN#	80-LQFP PIN #	100-QFP PIN #	TYPE	DESCRIPTION
FSRS#	-	-	-	-	76	I	FIFO Status Register Select (active low input with internal pull-up). The content of the FSTAT register is placed on the data bus when this pin becomes active. However it should be noted, D0-D3 contain the inverted logic states of TXRDY# A-D pins, and D4-D7 the logic states (un-inverted) of RXRDY# A-D pins. A valid address is not required when reading this status register.
MODEM OR SERIAL I/O INTERFACE							
TXA TXB TXC TXD	6 8 28 30	8 10 39 41	17 19 51 53	10 12 50 52	14 16 65 67	O	UART channels A-D Transmit Data and infrared transmit data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be a logic 1 during reset, or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infra-red mode, the inactive state (no data) for the Infrared encoder/decoder interface is a logic 0.
IRTXA IRTXB IRTXC IRTXD	- - - -	- - - -	- - - -	- - - -	6 24 57 75	O	UART channel A-D Infrared Transmit Data. The inactive state (no data) for the Infrared encoder/decoder interface is LOW. Regardless of the logic state of MCR bit-6, this pin will be operating in the Infrared mode.
RXA RXB RXC RXD	48 13 22 36	62 20 29 51	7 29 41 63	77 25 37 65	97 34 47 85	I	UART channel A-D Receive Data or infra-red receive data. Normal receive data input must idle HIGH.
RTSA# RTSB# RTSC# RTSD#	3 11 25 33	5 13 36 44	14 22 48 56	7 15 47 55	11 19 62 70	O	UART channels A-D Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], and IER[6]. Also see **Figure 12**. If these outputs are not used, leave them unconnected.
CTSA# CTSB# CTSC# CTSD#	1 12 23 35	2 16 33 47	11 25 45 59	4 18 44 58	8 22 59 73	I	UART channels A-D Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. Also see **Figure 12**. These inputs should be connected to VCC when not used.
DTRA# DTRB# DTRC# DTRD#	- - - -	3 15 34 46	12 24 46 58	5 17 45 57	9 21 60 72	O	UART channels A-D Data-Terminal-Ready (active low) or general purpose output. If these outputs are not used, leave them unconnected.

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Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN#	80-LQFP PIN #	100-QFP PIN #	TYPE	DESCRIPTION
DSRA# DSRB# DSRC# DSRD#	- - - -	1 17 32 48	10 26 44 60	3 19 43 59	7 23 58 74	I	UART channels A-D Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDA# CDB# CDC# CDD#	- - - -	64 18 31 49	9 27 43 61	79 23 39 63	99 32 49 83	I	UART channels A-D Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIA# RIB# RIC# RID#	- - - -	63 19 30 50	8 28 42 62	78 24 38 64	98 33 48 84	I	UART channels A-D Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
ANCILLARY SIGNALS							
XTAL1	18	25	35	31	40	I	Crystal or external clock input. Caution: this input is not 5V tolerant.
XTAL2	19	26	36	32	41	O	Crystal or buffered clock output.
16/68#	14	-	31	-	36	I	Intel or Motorola Bus Select (input with internal pull-up). When 16/68# pin is HIGH, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When 16/68# pin is LOW, 68 or Motorola mode, the device will operate in the Motorola bus type of interface. Motorola bus interface is not available on the 64 pin package.
CLKSEL	-	21	30	26	35	I	Baud-Rate-Generator Input Clock Prescaler Select for channels A-D. This input is only sampled during power up or a reset. Connect to VCC for divide by 1 (default) and GND for divide by 4. MCR[7] can override the state of this pin following a reset or initialization. See MCR bit-7 and **Figure 7** in the Baud Rate Generator section.
CHCCLK	-	-	-	-	42	I	This input provides the clock for UART channel C. An external 16X baud clock or the crystal oscillator's output, XTAL2, must be connected to this pin for normal operation. This input may also be used with MIDI (Musical Instrument Digital Interface) applications when an external MIDI clock is provided. This pin is only available in the 100-pin QFP package.

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Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN#	80-LQFP PIN #	100-QFP PIN #	TYPE	DESCRIPTION
RESET (RESET#)	20	27	37	33	43	I	When 16/68# pin is HIGH for Intel bus interface, this input becomes the Reset pin (active high). In this case, a 40 ns minimum HIGH pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (Table 17). When 16/68# pin is at LOW for Motorola bus interface, this input becomes Reset# pin (active low). This pin functions similarly, but instead of a HIGH pulse, a 40 ns minimum LOW pulse will reset the internal registers and outputs. Motorola bus interface is not available on the 64 pin package.
VCC	2, 24, 37	4, 35, 52	13, 47, 64	6, 46, 66	10, 61, 86	Pwr	2.25V to 3.6V power supply. All inputs, except XTAL1, are 5V tolerant.
GND	21, 47	14, 28, 45, 61	6, 23, 40, 57	16, 36, 56, 76	20, 46, 71, 96	Pwr	Power supply common, ground.
GND	Center Pad	N/A	N/A	N/A	N/A	Pwr	The center pad on the backside of the QFN package is metallic and should be connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.
N.C.	-	-	-		1, 2, 20, 21, 22, 27, 40, 41, 42, 60, 61, 62, 80		No Connection. These pins are not used in either the Intel or Motorola bus modes.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

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1.0 PRODUCT DESCRIPTION

The XR16V654 (V654) integrates the functions of 4 enhanced 16C550 Universal Asynchrounous Receiver and Transmitter (UART). Each UART is independently controlled and has its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 64 bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, infrared encoder and decoder (IrDA ver 1.0), programmable fractional baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 16 Mbps. The XR16V654 can operate from 2.25 to 3.6 volts. The V654 is fabricated with an advanced CMOS process.

Enhanced FIFO

The V654 QUART provides a solution that supports 64 bytes of transmit and receive FIFO memory, instead of 16 bytes in the ST16C554, or one byte in the ST16C454. The V654 is designed to work with high performance data communication systems, that require fast data processing time. Increased performance is realized in the V654 by the larger transmit and receive FIFOs, FIFO trigger level control and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C554 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 64 byte FIFO in the V654, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

Data Rate

The V654 is capable of operation up to 16 Mbps at 3.3V with 4Xinternal sampling clock rate. The device can operate at 3.3V with a crystal oscillator of up to 24 MHz crystal on pins XTAL1 and XTAL2, or external clock source of 64 MHz on XTAL1 pin. With a typical crystal of 14.7456 MHz and through a software option, the user can set the prescaler bit and sampling rate for data rates of up to 3.68 Mbps.

Enhanced Features

The rich feature set of the V654 is available through the internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. MCR bit-5 provides a facility for turning off (Xon) software flow control with any incoming (RX) character. In the 16 mode INTSEL and MCR bit-3 can be configured to provide a software controlled or continuous interrupt capability. For backward compatibility to the ST16C654, the 64-pin LQFP does not have the INTSEL pin. Instead, two different LQFP packages are offered. The XR16V654DIV operates in the continuous interrupt enable mode by internally bonding INTSEL to VCC. The XR16V654IV operates in conjunction with MCR bit-3 by internally bonding INTSEL to GND.

The XR16V654 offers a clock prescaler select pin to allow system/board designers to preset the default baud rate table on power up. The CLKSEL pin selects the div-by-1 or div-by-4 prescaler for the baud rate generator. It can then be overridden following initialization by MCR bit-7.

The 100 pin packages offer several other enhanced features. These features include a CHCCLK clock input, FSTAT register and separate IrDA TX outputs. The CHCCLK must be connected to the XTAL2 pin for normal operation or to external MIDI (Music Instrument Digital Interface) oscillator for MIDI applications. A separate register (FSTAT) is provided for monitoring the real time status of the FIFO signals TXRDY# and RXRDY# for each of the four UART channels (A-D). This reduces polling time involved in accessing individual channels. The 100 pin QFP package also offers four separate IrDA (Infrared Data Association Standard) TX outputs for Infrared applications. These outputs are provided in addition to the standard asynchronous modem data outputs.

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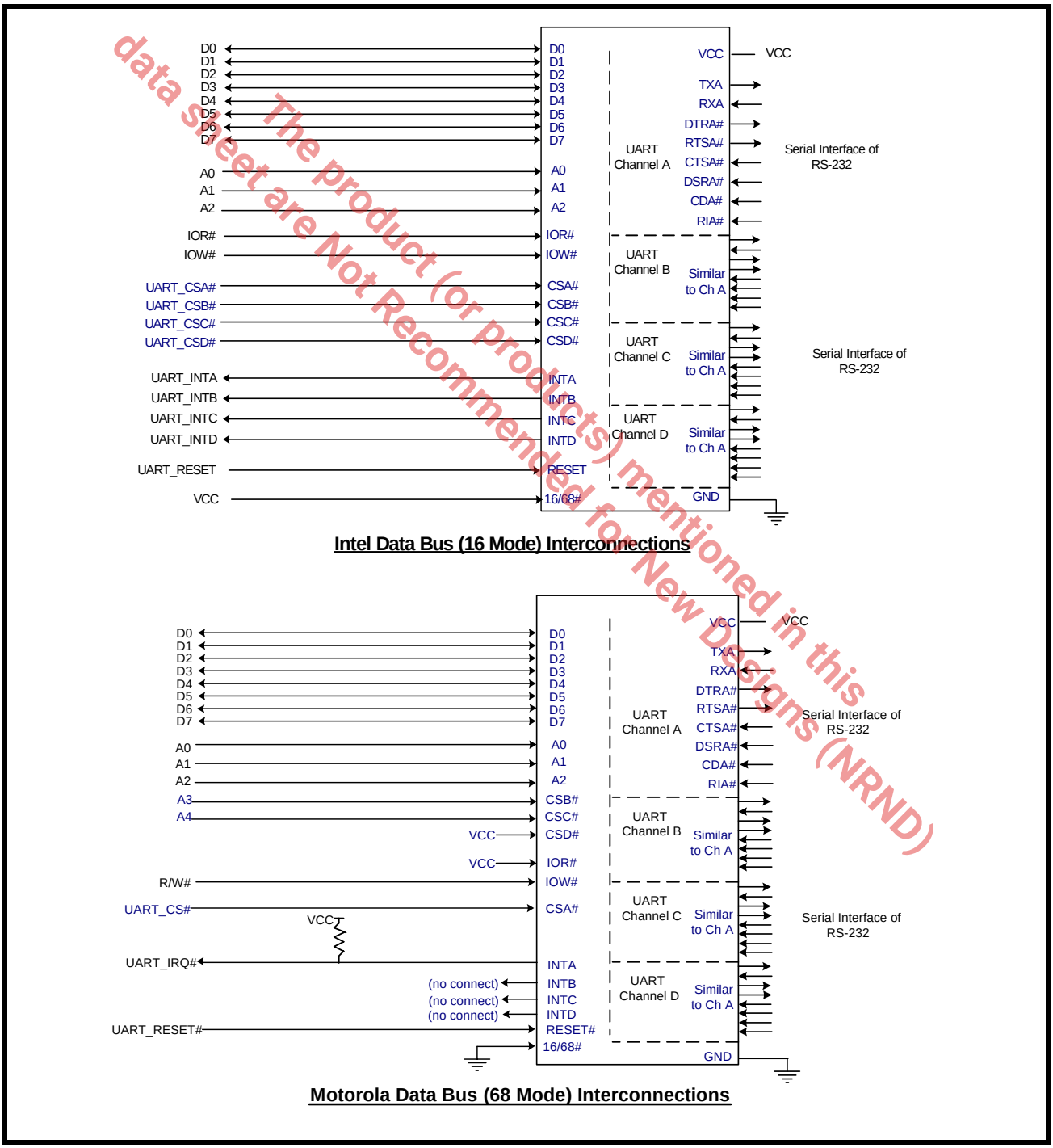
2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The V654 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required for a data bus transaction. Each bus cycle is asynchronous using CS# A-D, IOR# and IOW# or CS#, R/W#, A4 and A3 inputs. All four UART channels share the same data bus for host operations. A typical data bus interconnection for Intel and Motorola mode is shown in **Figure 5**.

FIGURE 5. XR16V654 TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS



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2.2 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 17). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device. Following a power-on reset or an external reset, the V654 is software compatible with previous generation of UARTs, 16C454 and 16C554.

2.3 Channel Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. During Intel Bus Mode (16/68# pin is connected to VCC), a logic 0 on chip select pins, CSA#, CSB#, CSC# or CSD# allows the user to select UART channel A, B, C or D to configure, send transmit data and/or unload receive data to/from the UART. Selecting all four UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from all four uarts simultaneously. Individual channel select functions are shown in **Table 1**.

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TABLE 1: CHANNEL A-D SELECT IN 16 MODE

CSA#	CSB#	CSC#	CSD#	FUNCTION
1	1	1	1	UART de-selected
0	1	1	1	Channel A selected
1	0	1	1	Channel B selected
1	1	0	1	Channel C selected
1	1	1	0	Channel D selected
0	0	0	0	Channels A-D selected

During Motorola Bus Mode (16/68# pin is connected to GND), the package interface pins are configured for connection with Motorola, and other popular microprocessor bus types. In this mode the V654 decodes two additional addresses, A3 and A4, to select one of the four UART ports. The A3 and A4 address decode function is used only when in the Motorola Bus Mode. **See Table 2.**

TABLE 2: CHANNEL A-D SELECT IN 68 MODE

CS#	A4	A3	FUNCTION
1	X	X	UART de-selected
0	0	0	Channel A selected
0	0	1	Channel B selected
0	1	0	Channel C selected
0	1	1	Channel D selected

2.4 Channels A-D Internal Registers

Each UART channel in the V654 has a set of enhanced registers for controlling, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM/DLD), and a user accessible scratchpad register (SPR).

Beyond the general 16C550 features and capabilities, the V654 offers enhanced feature registers (EFR, Xon/Xoff 1, Xon/Xoff 2, FSTAT) that provide automatic RTS and CTS hardware flow control and automatic Xon/Xoff software flow control. All the register functions are discussed in full detail later in **"Section 3.0, UART INTERNAL REGISTERS" on page 26**.

2.5 INT Ouputs for Channels A-D

The interrupt outputs change according to the operating mode and enhanced features setup. **Table 3 and 4** summarize the operating behavior for the transmitter and receiver. Also see **Figure 21** through **26**.

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TABLE 3: INT PIN OPERATION FOR TRANSMITTER FOR CHANNELS A-D

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
INT Pin	LOW = a byte in THR HIGH = THR empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty

TABLE 4: INT PIN OPERATION FOR RECEIVER FOR CHANNELS A-D

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
INT Pin	LOW = no data HIGH = 1 byte	LOW = FIFO below trigger level HIGH = FIFO above trigger level	LOW = FIFO below trigger level HIGH = FIFO above trigger level

2.6 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document does not mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A-D and TXRDY# A-D output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3 = 1). When the transmit and receive FIFOs are enabled and the DMA mode is disabled (FCR bit-3 = 0), the V654 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by

loading or unloading the FIFO in a block sequence determined by the programmed trigger level. The following table show their behavior. Also see Figure 21 through 26.

TABLE 5: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE FOR CHANNELS A-D

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR BIT-3 = 0 (DMA MODE DISABLED)	FCR BIT-3 = 1 (DMA MODE ENABLED)
RXRDY#	LOW = 1 byte HIGH = no data	LOW = at least 1 byte in FIFO HIGH = FIFO empty	HIGH to LOW transition when FIFO reaches the trigger level, or timeout occurs LOW to HIGH transition when FIFO empties
TXRDY#	LOW = THR empty HIGH = byte in THR	LOW = FIFO empty HIGH = at least 1 byte in FIFO	LOW = FIFO has at least 1 empty location HIGH = FIFO is full

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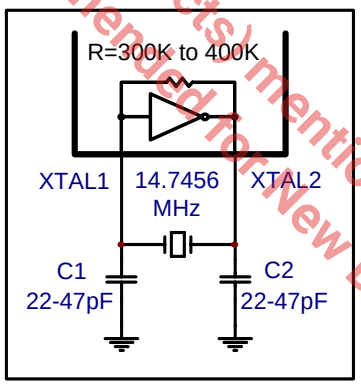
2.7 Crystal Oscillator or External Clock Input

The V654 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Caution: the XTAL1 input is not 5V tolerant. For programming details, see **"Section 2.8, Programmable Baud Rate Generator with Fractional Divisor" on page 15**.

FIGURE 6. TYPICAL CRYSTAL CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins. Typical oscillator connections are shown in Figure 6. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.8 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (216 - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X or 8X or 4X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to

the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon reset. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the divisor. Only the four lower bits of the DLD are implemented and they are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. **Table 6** shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in **Table 6**. At 8X sampling rate, these data rates would double. And at 4X sampling rate, they would quadruple. Also, when using 8X sampling mode, please note that the bit-time will have a jitter (+/- 1/16) whenever the DLD is non-zero and is an odd number. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal)=(XTAL1 clock frequency / prescaler) /(serial data rate x 16), with 16X mode, **DLD[5:4]='00'**
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 8), with 8X mode, **DLD[5:4] = '01'**
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 4), with 4X mode, **DLD[5:4] = '10'**

The closest divisor that is obtainable in the V654 can be calculated using the following formula:

ROUND((Required Divisor - TRUNC(Required Divisor))*16)/16 + TRUNC(Required Divisor), where

DLM = TRUNC(Required Divisor) >> 8
DLL = TRUNC(Required Divisor) & 0xFF
DLD = ROUND((Required Divisor-TRUNC(Required Divisor))*16)

In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value 'A' by 'B' number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 7. BAUD RATE GENERATOR

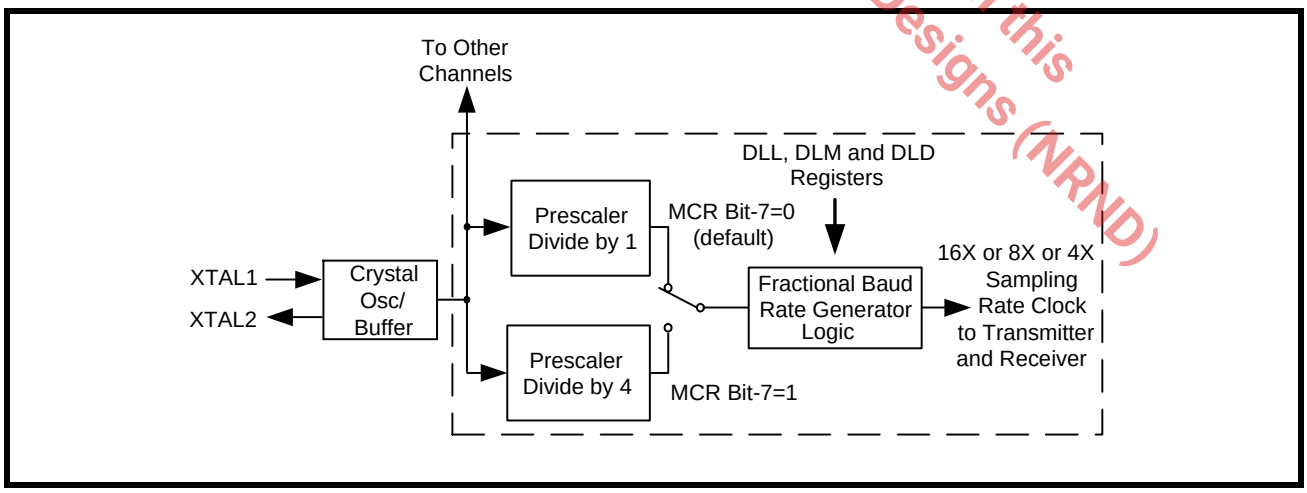


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TABLE 6: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	DIVISOR FOR 16x Clock (Decimal)	DIVISOR OBTAINABLE IN V654	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DLD PROGRAM VALUE (HEX)	DATA ERROR RATE (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0
300000	5	5	0	5	0	0
400000	3.75	3 12/16	0	3	C	0
460800	3.2552	3 4/16	0	3	4	0.16
500000	3	3	0	3	0	0
750000	2	2	0	2	0	0
921600	1.6276	1 10/16	0	1	A	0.16
1000000	1.5	1 8/16	0	1	8	0

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2.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X/4X internal clock. A bit time is 16/8/4 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

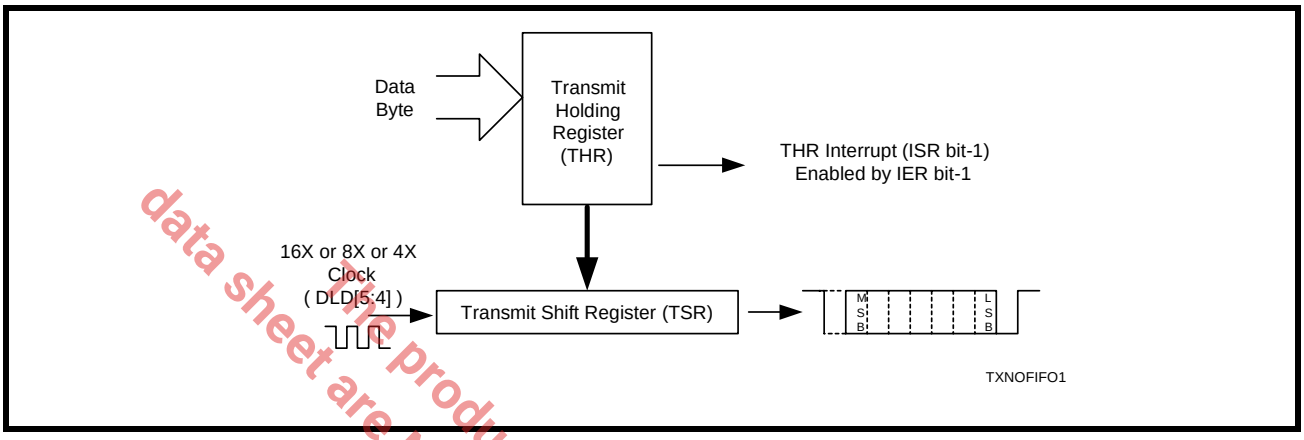
2.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 8. TRANSMITTER OPERATION IN NON-FIFO MODE



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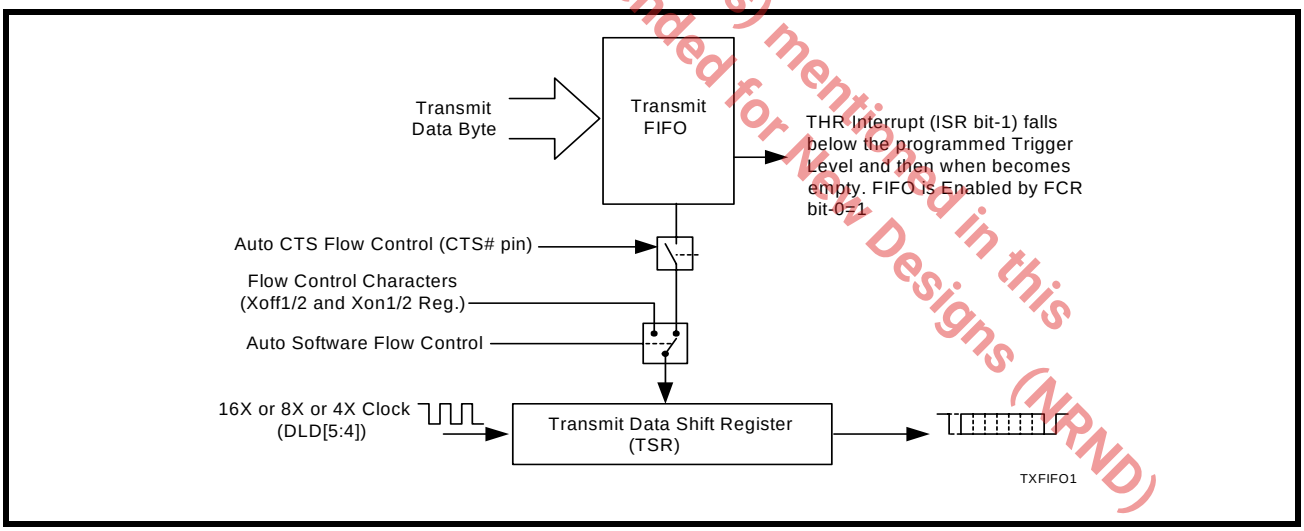
2.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the FIFO becomes empty. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 9. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X/4X clock (DLD[5:4]) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X/4X clock rate. After 8 clocks (or 4 if 8X or 2 if 4X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0. See **Figure 10** and **Figure 11** below.

2.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

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FIGURE 10. RECEIVER OPERATION IN NON-FIFO MODE

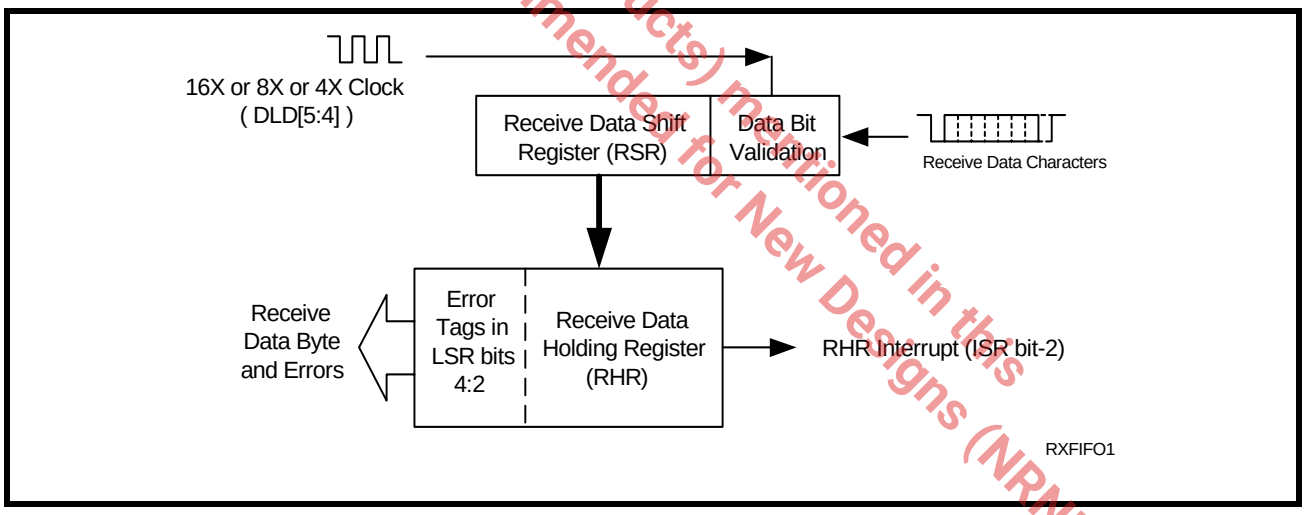
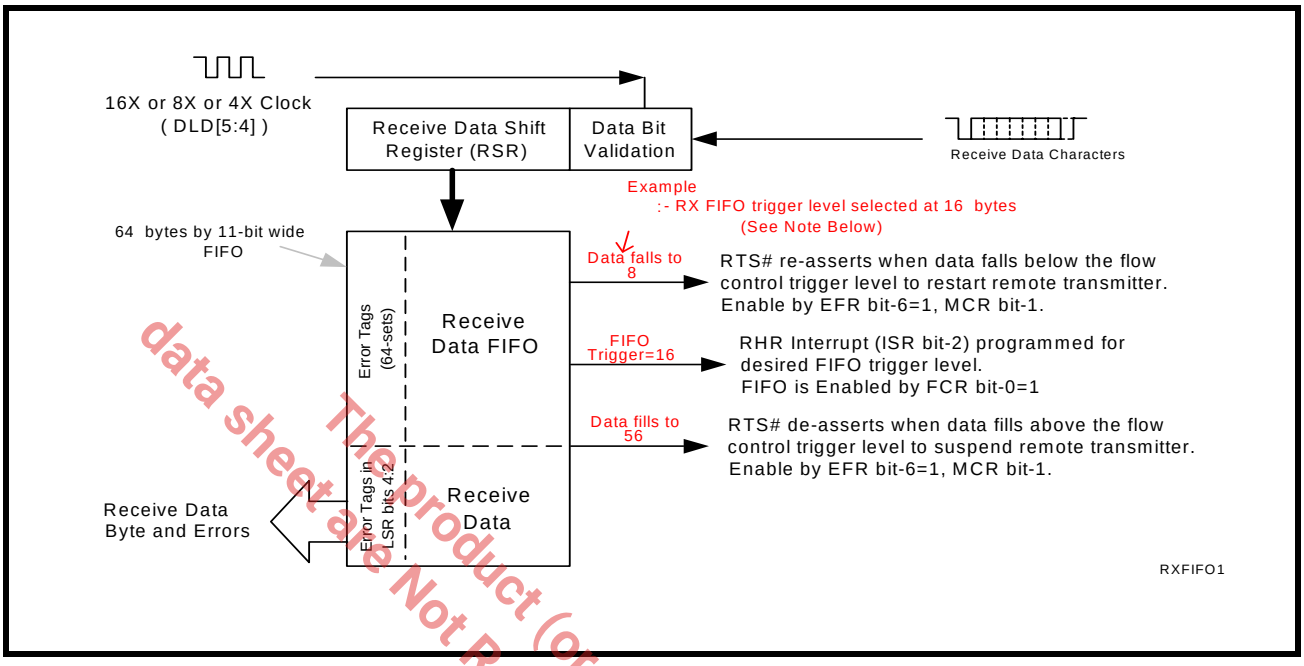


FIGURE 11. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.11 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 12):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.12 Auto RTS Hysteresis

The V654 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the XR16C850, ST16C650A and ST16C550 family of UARTs. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the selected RX trigger level. The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches one trigger level above the selected trigger level in the trigger table (Table 12). The RTS# pin will return LOW after the RX FIFO is unloaded to one level below the selected trigger level. Under the above described conditions, the V654 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On).

TABLE 7: AUTO RTS (HARDWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	RTS# DE-ASSERTED (HIGH) (CHARACTERS IN RX FIFO)	RTS# ASSERTED (LOW) (CHARACTERS IN RX FIFO)
8	8	16	0
16	16	56	8
56	56	60	16
60	60	60	56

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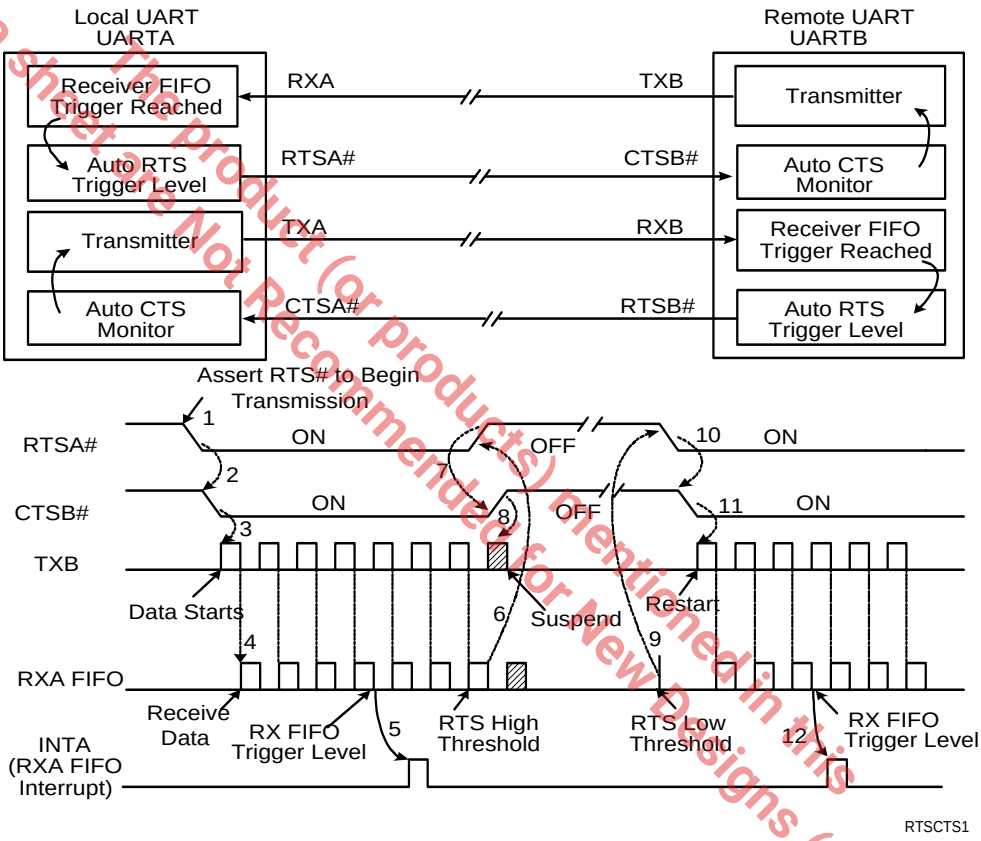
2.13 Auto CTS Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 12**):

- Enable auto CTS flow control using EFR bit-7.

If needed, the CTS interrupt can be enabled through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 12. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

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2.14 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 16), the V654 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the V654 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the V654 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the V654 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 16) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the V654 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the V654 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The V654 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the V654 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level. Table 8 below explains this.

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TABLE 8: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
56	56	56*	16
60	60	60*	56

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2* characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.

2.15 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The V654 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

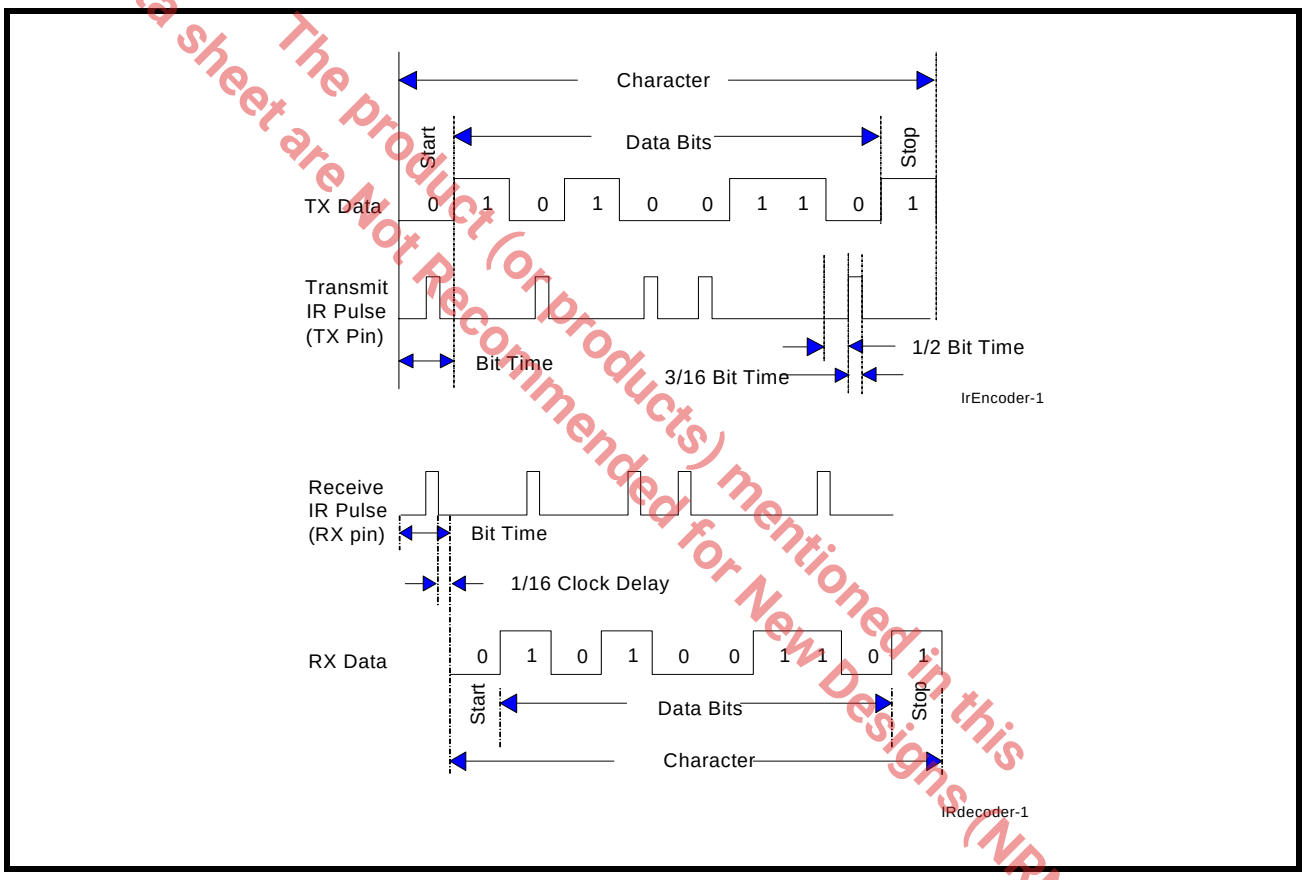
2.16 Infrared Mode

The V654 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 13** below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see **Figure 13**.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream.

FIGURE 13. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



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2.17 Sleep Mode with Auto Wake-Up

The V654 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the V654 to enter sleep mode:

- no interrupts pending for all four channels of the V654 (ISR bit-0 = 1)
- sleep mode of all channels are enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idling HIGH

The V654 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The V654 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the V654 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the V654 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The V654 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, CSC#, CSD# and modem input lines remain steady when the V654 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 42. If the input lines are floating or are toggling while the V654 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX A-D pins are idling HIGH or “marking” condition during sleep mode. This may not occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on each of the RX A-D inputs.

2.18 Internal Loopback

The V654 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. **Figure 14** shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held HIGH or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

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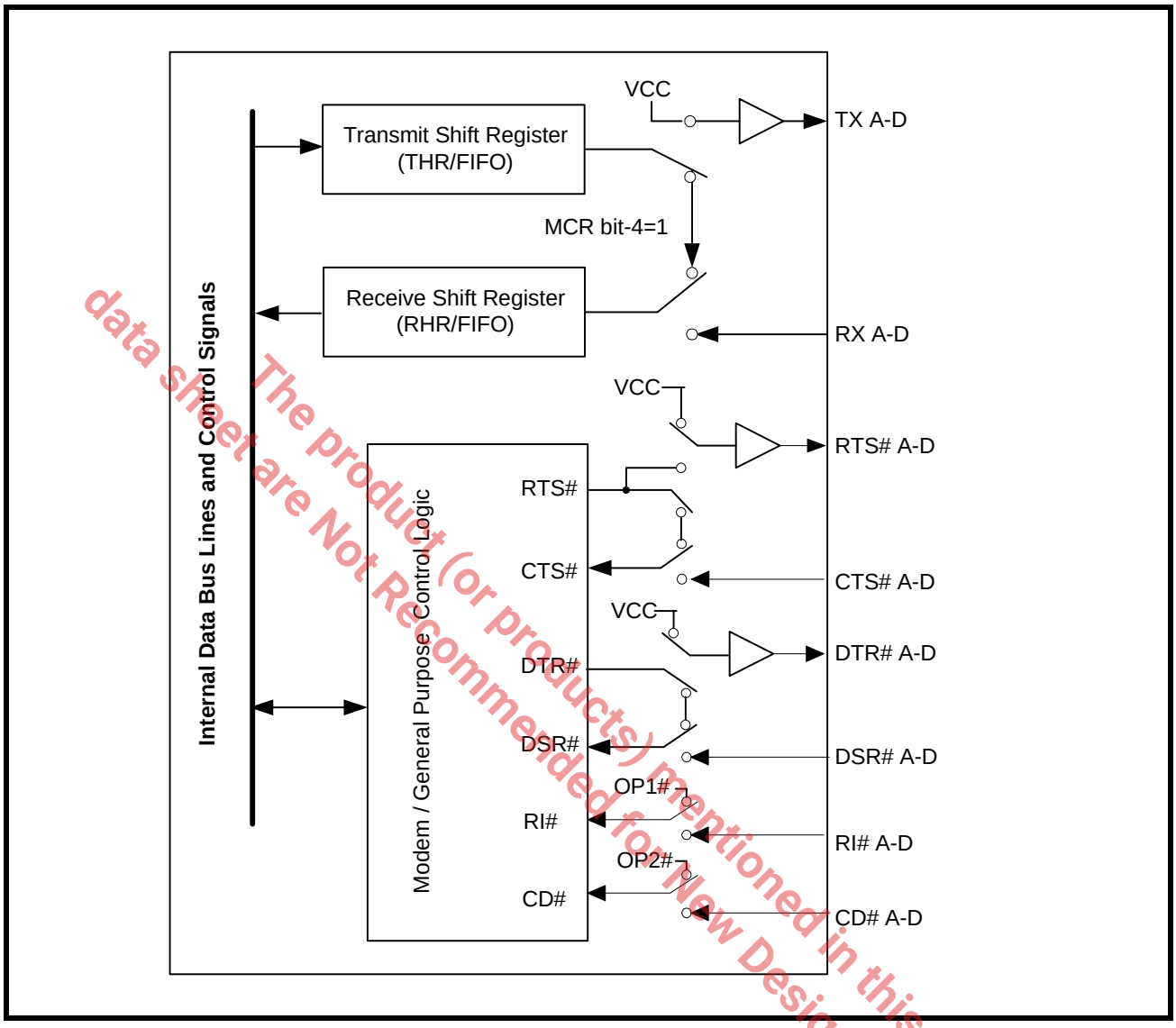
FIGURE 14. INTERNAL LOOP BACK IN CHANNEL A AND B



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3.0 UART INTERNAL REGISTERS

Each UART channel in the V654 has its own set of configuration registers selected by address lines A0, A1 and A2 with a specific channel selected (See Table 1 and Table 2). The complete register set is shown on Table 9 and Table 10.

.

TABLE 9: UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor MSB	Read/Write	
0 1 0	DLD - Divisor Fractional	Read/Write	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register	Read-only	
1 1 0	MSR - Modem Status Register	Read-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Reg	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	
X X X	FSTAT - FIFO Status Register	Read-only	FSRS# pin is LOW

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The product(s) mentioned in this

TABLE 10: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS# Int. Enable	0/ RTS# Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR[7] = 0
0 1 0	FCR	WR	RX FIFO Trigger	RX FIFO Trigger	0/ TX FIFO Trigger	0/ TX FIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Mode ENable	0/ XonAny	Internal Lopback Enable	INT Out-put Enable (OP2#)	Rsvd (OP1#)	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run Error	RX Data Ready	LCR[7] = 0
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR≠0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 1 0	DLD	RD/WR	Rsvd	Rsvd	4X Mode	8X Mode	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR≠0xBF EFR[4] = 1

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The product (or Products) mentioned in this

TABLE 10: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Enhanced Registers											
0 1 0	EFR	RD/WR	Auto CTS# Enable	Auto RTS# Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5], DLD	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	LCR=0xBF
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
X X X	FSTAT	RD	RX-RDYD#	RX-RDYC#	RX-RDYB#	RX-RDYA#	TX-RDYD#	TX-RDYC#	TX-RDYB#	TX-RDYA#	FSRS# pin is a logic 0. No address lines required.

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4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

SEE"RECEIVER" ON PAGE 19.

4.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 17.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16V654 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

Logic 0 = Disable the receive data ready interrupt (default).

Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

Logic 0 = Disable Transmit Ready interrupt (default).

Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when an overrun occurs. LSR bits 2-4 generate an interrupt when the character in the RHR has an error.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR[4] = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR[4]=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt. (default)
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

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IER[6]: RTS# Output Interrupt Enable (requires EFR[4]=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from LOW to HIGH (if enabled by EFR bit-6).

IER[7]: CTS# Input Interrupt Enable (requires EFR[4]=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from LOW to HIGH (if enabled by EFR bit-7).

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 11, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

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4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.
- CTS# is when the remote transmitter toggles the input pin (from LOW to HIGH) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS flow control.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff interrupt is cleared by a read to the ISR register or when XON character(s) is received.
- Special character interrupt is cleared by a read to ISR register or after next character is received.
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register.

TABLE 11: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or Special character)
7	1	0	0	0	0	0	CTS#, RTS# change of state
-	0	0	0	0	0	1	None (default)

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ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 11).

ISR[4]: Interrupt Status (requires EFR bit-4 = 1)

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s) or a special character.

ISR[5]: Interrupt Status (requires EFR bit-4 = 1)

ISR bit-5 indicates that CTS# or RTS# has changed state from LOW to HIGH.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the -TXRDY and -RXRDY pins. See DMA operation section for details.

- Logic 0 = Normal Operation (default).
- Logic 1 = DMA Mode.

FCR[5:4]: Transmit FIFO Trigger Select (requires EFR bit-4 = 1)

(logic 0 = default, TX trigger level = 8)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 12 below shows the selections.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level = 8)

These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. Table 12 shows the complete selections.

TABLE 12: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION

FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL
		0	0		8
		0	1		16
		1	0		32
		1	1		56
0	0			8	
0	1			16	
1	0			56	
1	1			60	

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4.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See **Table 13** for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

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LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 13: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, HIGH
1	1	1	Forced parity to space, LOW

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LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a “space’, logic 0, state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a “space”, logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM/DLD) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

4.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output HIGH (default).
- Logic 1 = Force DTR# output LOW.

MCR[1]: RTS# Output

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# output HIGH (default).
- Logic 1 = Force RTS# output LOW.

MCR[2]: Reserved

OP1# is not available as an output pin on the V654. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem RI# interface signal.

MCR[3]: INT Output Enable

Enable or disable INT outputs to become active or in three-state. This function is associated with the INTSEL input, see below table for details. This bit is also used to control the OP2# signal during internal loopback mode. INTSEL pin must be LOW during 68 mode.

- Logic 0 = INT (A-D) outputs disabled (three state) in the 16 mode (default). During internal loopback mode, OP2# is HIGH.
- Logic 1 = INT (A-D) outputs enabled (active) in the 16 mode. During internal loopback mode, OP2# is LOW.

TABLE 14: INT OUTPUT MODES

INTSEL PIN	MCR BIT-3	INT A-D OUTPUTS IN 16 MODE
0	0	Three-State
0	1	Active
1	X	Active

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MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and Figure 14.

MCR[5]: Xon-Any Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Xon-Any function (for 16C550 compatibility, default).
- Logic 1 = Enable Xon-Any function. In this mode, any RX character received will resume transmit operation. The RX character will be loaded into the RX FIFO , unless the RX character is an Xon or Xoff character and the V654 is programmed to use the Xon/Xoff flow control.

MCR[6]: Infrared Encoder/Decoder Enable (requires EFR bit-4 = 1)

- Logic 0 = Enable the standard modem receive and transmit input/output interface. (Default)
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. The TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels conform to the IrDA infrared interface requirement. The RX FIFO may need to be flushed upon enable. While in this mode, the infrared TX output will be LOW during idle data conditions.

MCR[7]: Clock Prescaler Select (requires EFR bit-4 = 1)

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is enabled, LSR bit 1 will generate an interrupt immediately and LSR bits 2-4 will generate an interrupt when a character with an error is in the RHR.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was LOW for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, “mark” or HIGH.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

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4.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used for general purpose inputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from LOW to HIGH, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A HIGH on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a LOW will resume data transmission. Normally MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

Normally this bit is the complement of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.10 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

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4.11 Baud Rate Generator Registers (DLL and DLM) - Read/Write

These registers make-up the value of the baud rate divisor. The concatenation of the contents of DLM and DLL gives the 16-bit divisor value. Then the value is added to DLD[3:0]/16 to achieve the fractional baud rate divisor. DLD must be enabled via EFR bit-4 before it can be accessed. See **Table 15** below and **See "Section 2.8, Programmable Baud Rate Generator with Fractional Divisor" on page 15.**

DLD[5:4]: Sampling Rate Select

These bits select the data sampling rate. By default, the data sampling rate is 16X. The maximum data rate will double if the 8X mode is selected and will quadruple if the 4X mode is selected. See **Table 15** below.

TABLE 15: SAMPLING RATE SELECT

DLD[5]	DLD[4]	SAMPLING RATE
0	0	16X
0	1	8X
1	X	4X

DLD[7:6]: Reserved

4.12 Enhanced Feature Register (EFR) - Read/Write

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see **Table 16**). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[3:0]: Software Flow Control Select

Single character and dual sequential characters software flow control is supported. Combinations of software flow control can be selected by programming these bits.

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

TABLE 16: SOFTWARE FLOW CONTROL FUNCTIONS

EFR BIT-3 CONT-3	EFR BIT-2 CONT-2	EFR BIT-1 CONT-1	EFR BIT-0 CONT-0	TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	No transmit flow control, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

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The product (or products) mentioned in this

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7, and DLD are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the receive data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit of the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]= ‘10’) then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]= ‘01’) then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt, if enabled via IER bit-5.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS de-asserts HIGH at the next upper trigger level/hysteresis level. RTS# will return LOW when FIFO data falls below the next lower trigger level/hysteresis level. The RTS# output must be asserted (LOW) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled (default).
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled (default).
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts to logic 1. Data transmission resumes when CTS# returns to a logic 0.

4.13 Software Flow Control Registers (XOFF1, XOFF2, XON1, XON2) - Read/Write

These registers are used as the programmable software flow control characters xoff1, xoff2, xon1, and xon2. For more details, see Table 8.

4.14 FIFO Status Register (FSTAT) - Read/Write

This register is applicable only to the 100 pin QFP XR16V654. The FIFO Status Register provides a status indication for each of the transmit and receive FIFO. These status bits contain the inverted logic states of the TXRDY# A-D outputs and the (un-inverted) logic states of the RXRDY# A-D outputs. The contents of the FSTAT register are placed on the data bus when the FSRS# pin (pin 76) is a logic 0. Also see FSRS# pin description.

FSTAT[3:0]: TXRDY# A-D Status Bits

Please see Table 5 for the interpretation of the TXRDY# signals.

FSTAT[7:4]: RXRDY# A-D Status Bits

Please see Table 5 for the interpretation of the RXRDY# signals.

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The product (s) mentioned in this

TABLE 17: UART RESET CONDITIONS FOR CHANNELS A-D

REGISTERS	RESET STATE
DLM, DLL	DLM = 0x00 and DLL = 0x01. Only resets to these values during a power up. They do not reset when the Reset Pin is asserted.
DLD	Bits 7-0 = 0x00
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
EFR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
FSTAT	Bits 7-0 = 0xFF
I/O SIGNALS	**RESET STATE**
TX	HIGH
IRTX	LOW
RTS#	HIGH
DTR#	HIGH
RXRDY#	HIGH
TXRDY#	LOW
INT (16 Mode)	XR16V654 = Three-State Condition (INTSEL = LOW) XR16V654 = LOW (INTSEL = HIGH) XR16V654D = LOW
IRQ# (68 Mode)	Three-State Condition (INTSEL = LOW)

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The product (or products) mentioned in this

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	4 Volts
Voltage at Any Pin	GND-0.3 V to 4 V
Operating Temperature	-40° to +85°C
Storage Temperature	-65° to +150°C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (48-QFN)	theta-ja = 28°C/W, theta-jc = 10.5^{o}C/W
Thermal Resistance (64-LQFP)	theta-ja = 49°C/W, theta-jc = 10°C/W
Thermal Resistance (68-PLCC)	theta-ja = 39°C/W, theta-jc = 17°C/W
Thermal Resistance (80-LQFP)	theta-ja = 37°C/W, theta-jc = 7°C/W
Thermal Resistance (100-QFP)	theta-ja = 45°C/W, theta-jc = 12°C/W

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The product (or products) mentioned in this

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC IS 2.25 TO 3.6V

SYMBOL	PARAMETER	LIMITS 2.5V MIN	LIMITS 2.5V MAX	LIMITS 3.3V MIN	LIMITS 3.3V MAX	UNITS	CONDITIONS
V_{ILCK}	Clock Input Low Level	-0.3	0.4	-0.3	0.6	V	
V_{IHCK}	Clock Input High Level	2.0	VCC	2.4	VCC	V	
V_{IL}	Input Low Voltage	-0.3	0.5	-0.3	0.7	V	
V_{IH}	Input High Voltage	1.8	5.5	2.0	5.5	V	
V_{OL}	Output Low Voltage		0.4		0.4	V V	I_{OL} = 6 mA I_{OL} = 4 mA
V_{OH}	Output High Voltage	1.8		2.0		V V	I_{OH} = -4 mA I_{OH} = -2 mA
I_{IL}	Input Low Leakage Current		±15		±15	uA	
I_{IH}	Input High Leakage Current		±15		±15	uA	
C_{IN}	Input Pin Capacitance		5		5	pF	
I_{CC}	Power Supply Current		1.7		3	mA	Ext Clk = 2MHz
I_{SLEEP}	Sleep Current		350		450	uA	See Test 1

Test 1: The following inputs remain steady at VCC or GND state to minimize Sleep current: A0-A2, D0-D7, IOR#, IOW#, CSA#, CSB#, CSC#, and CSD#. Also, RXA, RXB, RXC, and RXD inputs must idle at HIGH while asleep.

AC ELECTRICAL CHARACTERISTICS

TA = -40° TO +85°C, VCC IS 2.25 TO 3.6V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 2.5V ± 10% MIN	LIMITS 2.5V ± 10% MAX	LIMITS 3.3V ± 10% MIN	LIMITS 3.3V ± 10% MAX	UNIT
XTAL1	UART Crystal Frequency		24		24	MHz
ECLK	External Clock Frequency		50		64	MHz
T_{ECLK}	External Clock Time Period	10		7		ns
T_{AS}	Address Setup Time (16 Mode)	0		0		ns
T_{AH}	Address Hold Time (16 Mode)	0		0		ns
T_{CS}	Chip Select Width (16 Mode)	50		40		ns
T_{RD}	IOR# Strobe Width (16 Mode)	50		40		ns
T_{DY}	Read Cycle Delay (16 Mode)	50		40		ns
T_{RDV}	Data Access Time (16 Mode)		45		35	ns
T_{DD}	Data Disable Time (16 Mode)		10		10	ns
T_{WR}	IOW# Strobe Width (16 Mode)	50		40		ns
T_{DY}	Write Cycle Delay (16 Mode)	50		40		ns
T_{DS}	Data Setup Time (16 Mode)	10		10		ns
T_{DH}	Data Hold Time (16 Mode)	5		5		ns
T_{ADS}	Address Setup (68 Mode)	0		0		ns
T_{ADH}	Address Hold (68 Mode)	0		0		ns
T_{RWS}	R/W# Setup to CS# (68 Mode)	0		0		ns
T_{RDA}	Data Access Time (68 mode)		45		35	ns
T_{RDH}	Data Disable Time (68 mode)		10		10	ns
T_{WDS}	Write Data Setup (68 mode)	10		15		ns
T_{WDH}	Write Data Hold (68 Mode)	5		5		ns
T_{RWH}	CS# De-asserted to R/W# De-asserted (68 Mode)	10		5		ns
T_{CSL}	CS# Strobe Width (68 Mode)	50		40		ns
T_{CSD}	CS# Cycle Delay (68 Mode)	50		40		ns
T_{WDO}	Delay From IOW# To Output		50		50	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		50		50	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		50		50	ns

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

AC ELECTRICAL CHARACTERISTICS

TA = -40° TO +85°C, VCC IS 2.25 TO 3.6V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 2.5V ± 10% MIN	LIMITS 2.5V ± 10% MAX	LIMITS 3.3V ± 10% MIN	LIMITS 3.3V ± 10% MAX	UNIT
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45		45	ns
T_{SI}	Delay From Start To Interrupt		45		45	ns
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		45		45	ns
T_{SSR}	Delay From Stop To Set RXRDY#		1		1	Bclk
T_{RR}	Delay From IOR# To Reset RXRDY#		45		45	ns
T_{WT}	Delay From IOW# To Set TXRDY#		45		45	ns
T_{SRT}	Delay From Center of Start To Reset TXRDY#		8		8	Bclk
T_{RST}	Reset Pulse Width	40		40		ns
Bclk	Baud Clock	16X or 8X or 4X of data rate				Hz

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The product (or products) mentioned in this

FIGURE 15. CLOCK TIMING

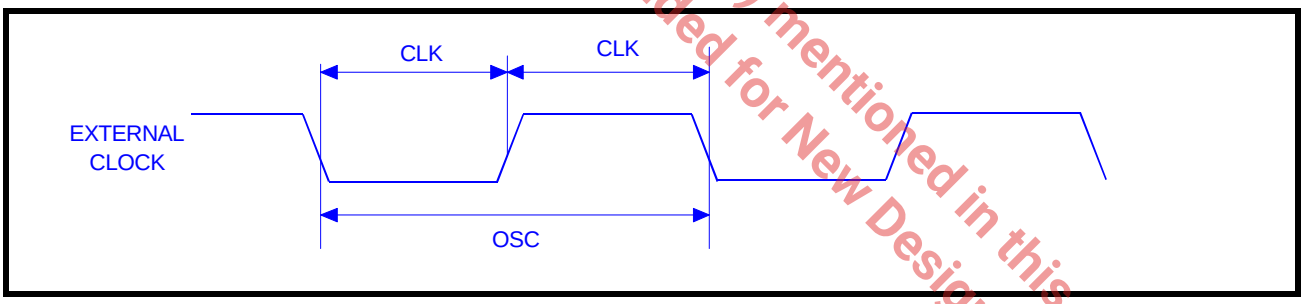

FIGURE 16. MODEM INPUT/OUTPUT TIMING FOR CHANNELS A-D

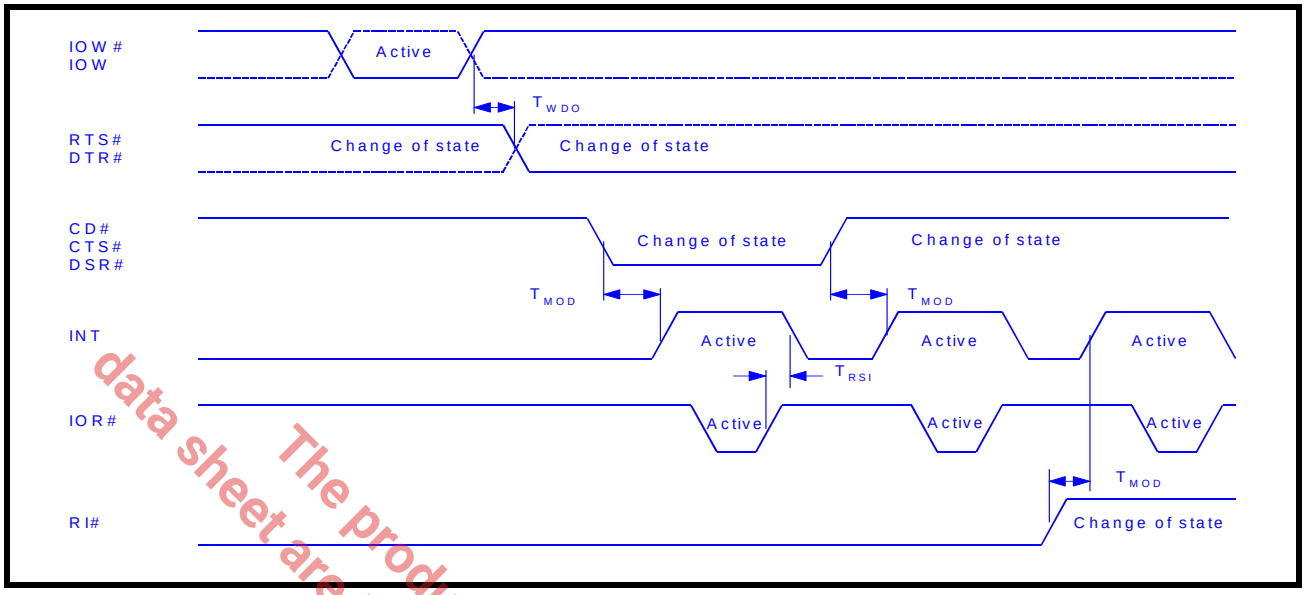

FIGURE 17. 16 MODE (INTEL) DATA BUS READ TIMING FOR CHANNELS A-D

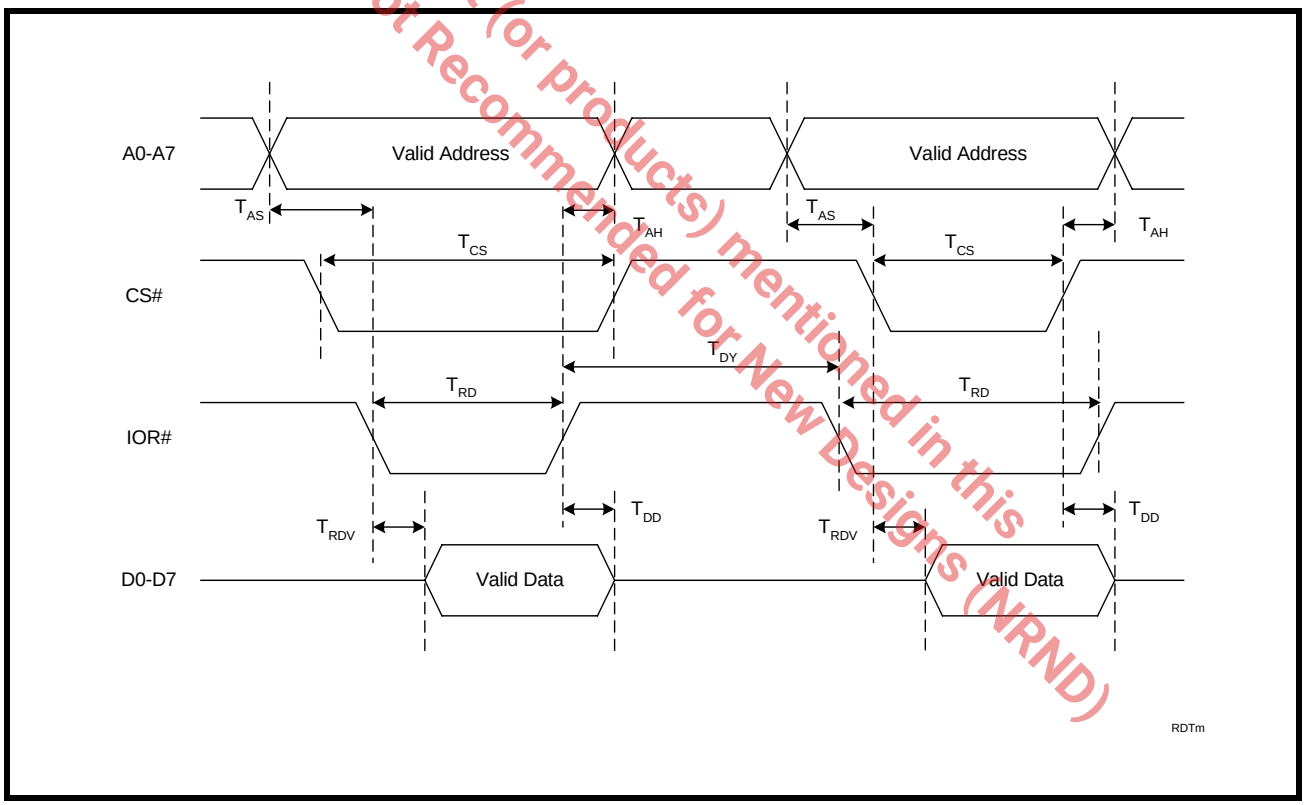

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FIGURE 18. 16 MODE (INTEL) DATA BUS WRITE TIMING FOR CHANNELS A-D

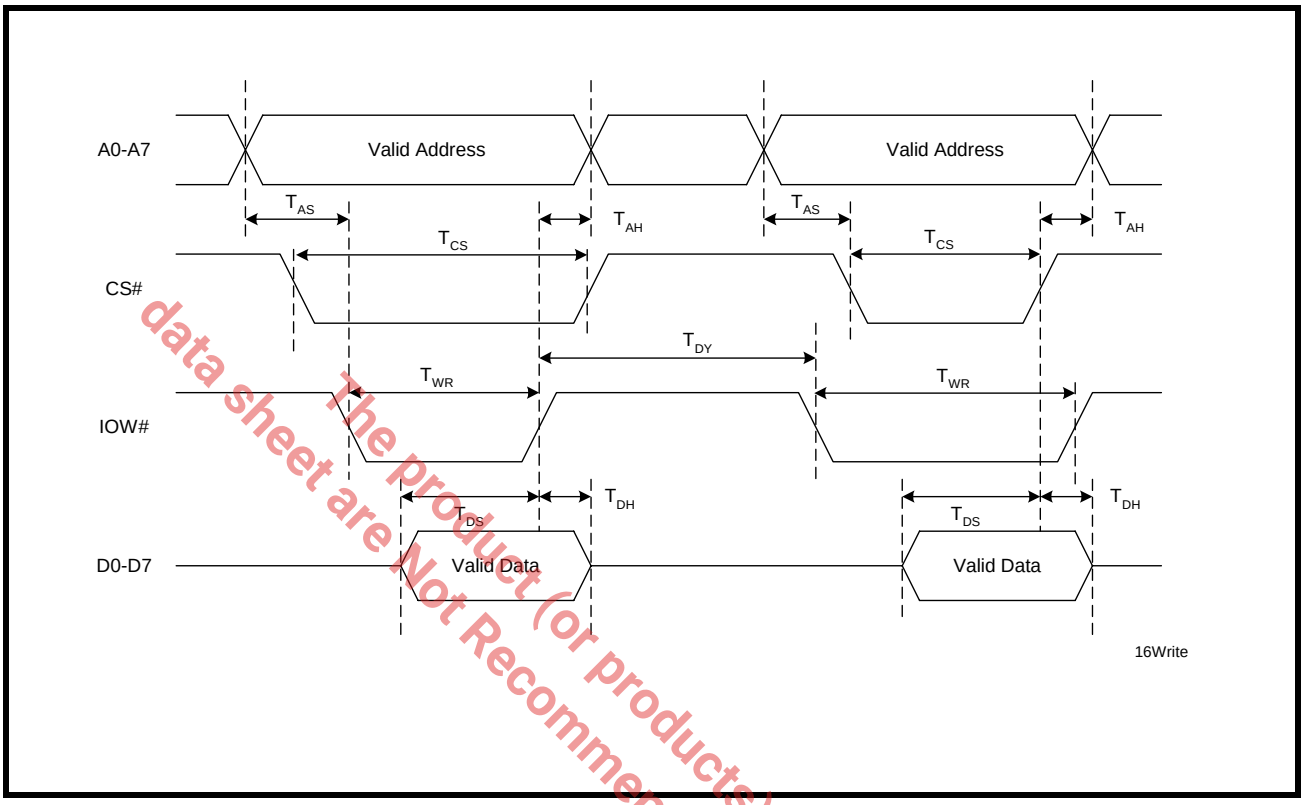
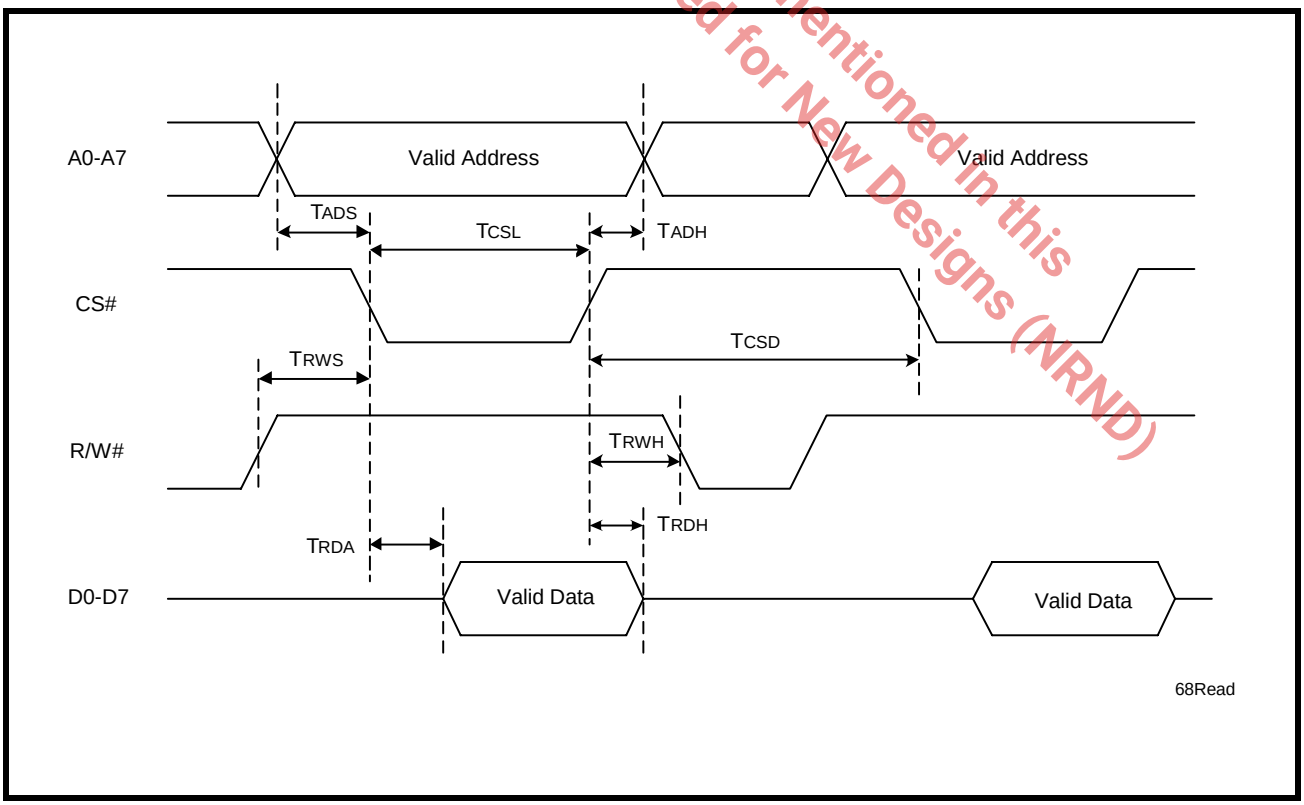


FIGURE 19. 68 MODE (MOTOROLA) DATA BUS READ TIMING FOR CHANNELS A-D



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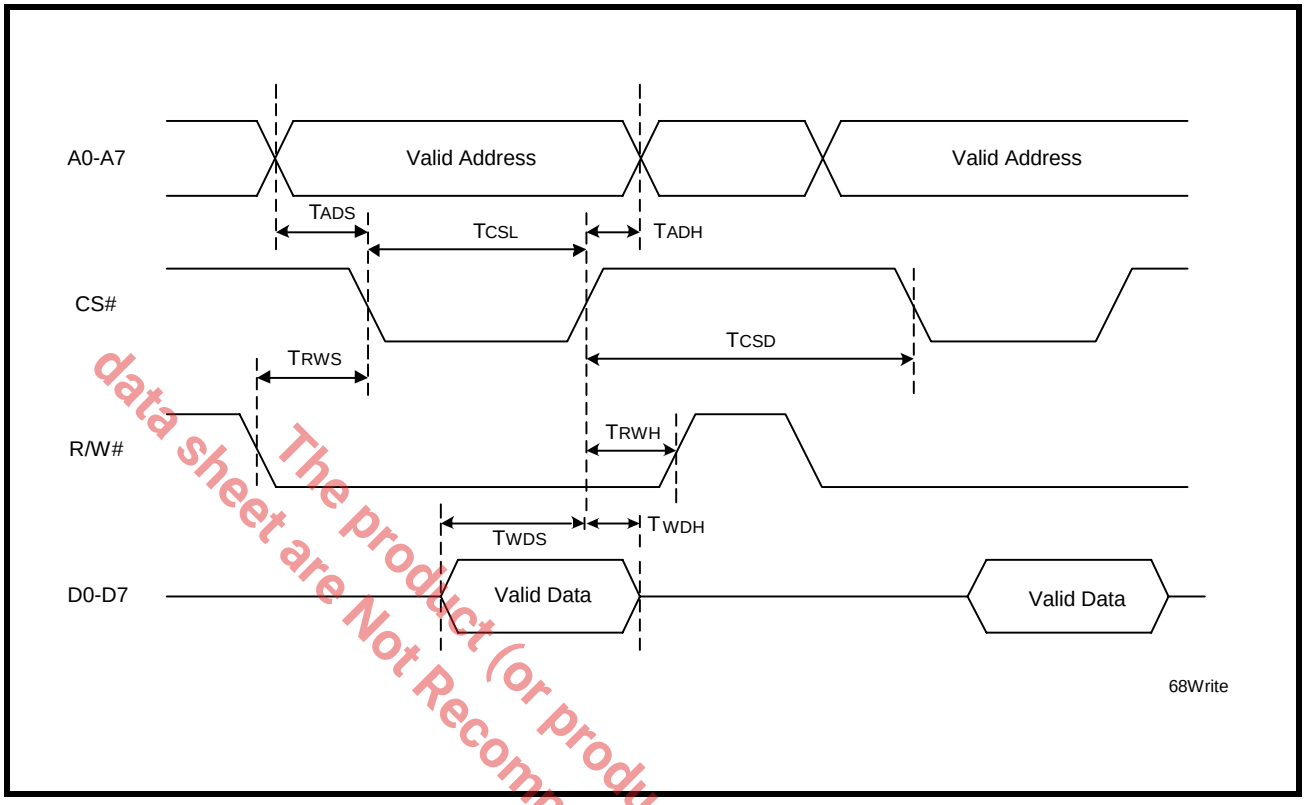
The product (or products) mentioned in this

FIGURE 20. 68 MODE (MOTOROLA) DATA BUS WRITE TIMING FOR CHANNELS A-D



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The product (or products) mentioned in this

FIGURE 21. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A-D

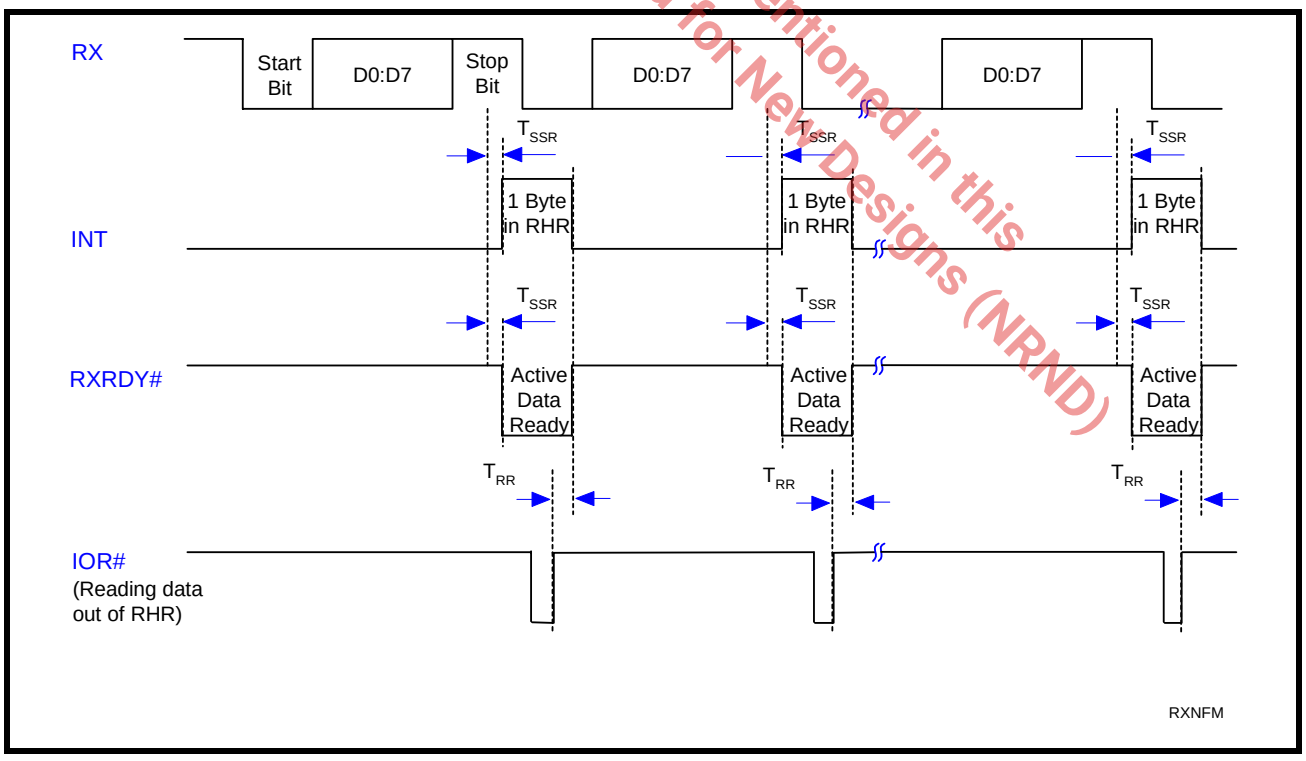


FIGURE 22. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A-D

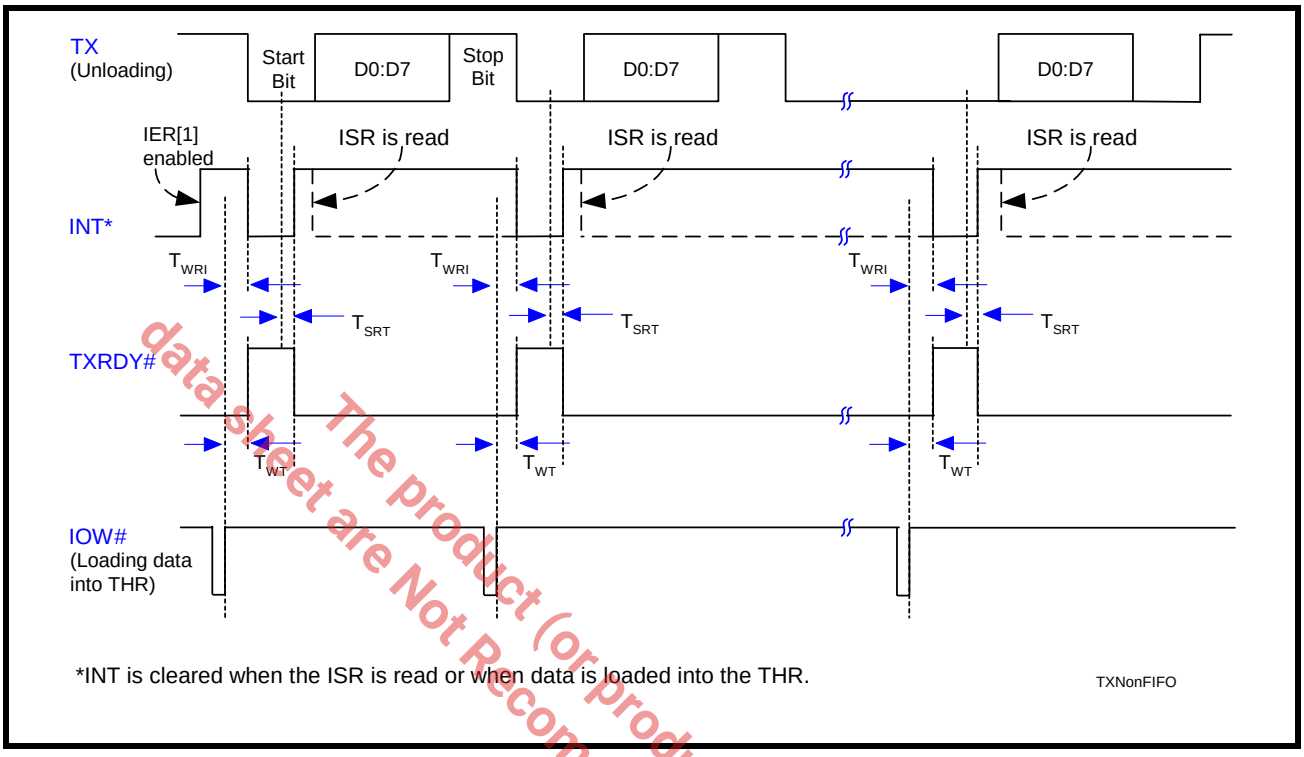
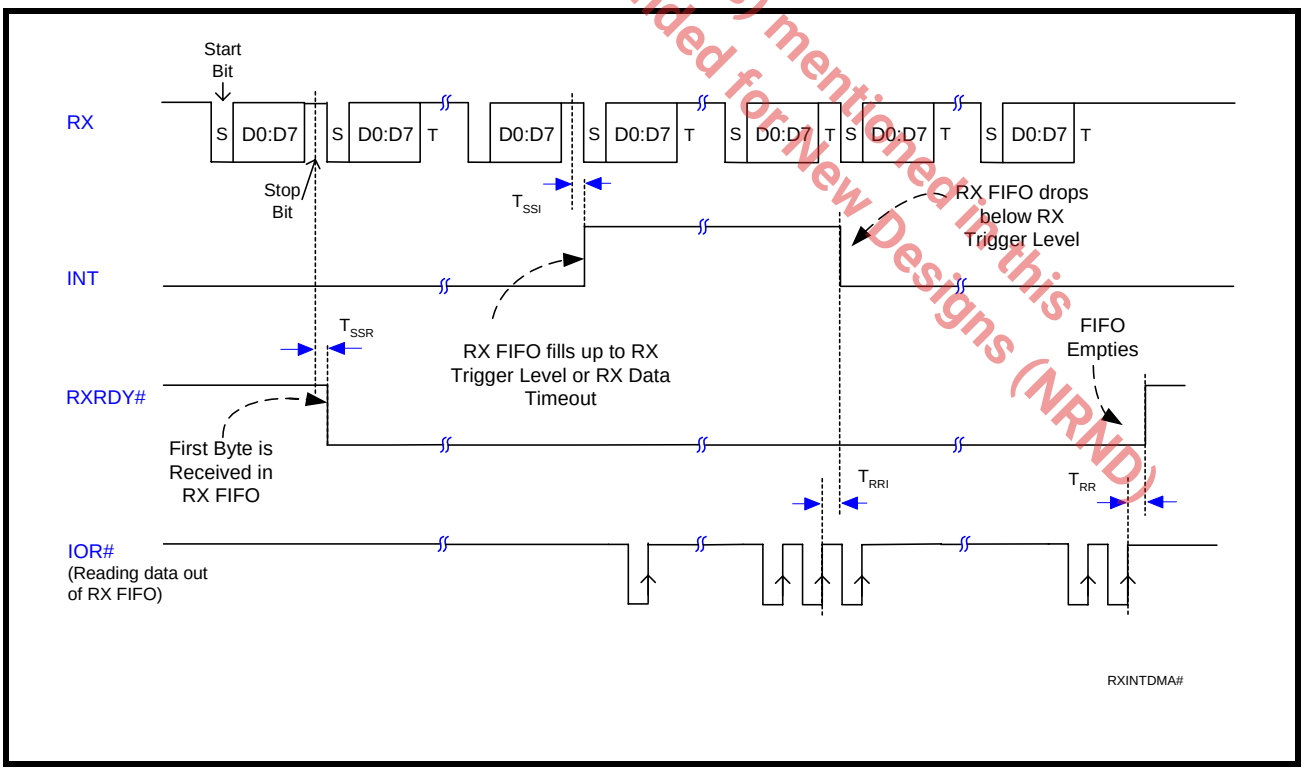


FIGURE 23. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED] FOR CHANNELS A-D



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The product (or products) mentioned in this

FIGURE 24. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED] FOR CHANNELS A-D

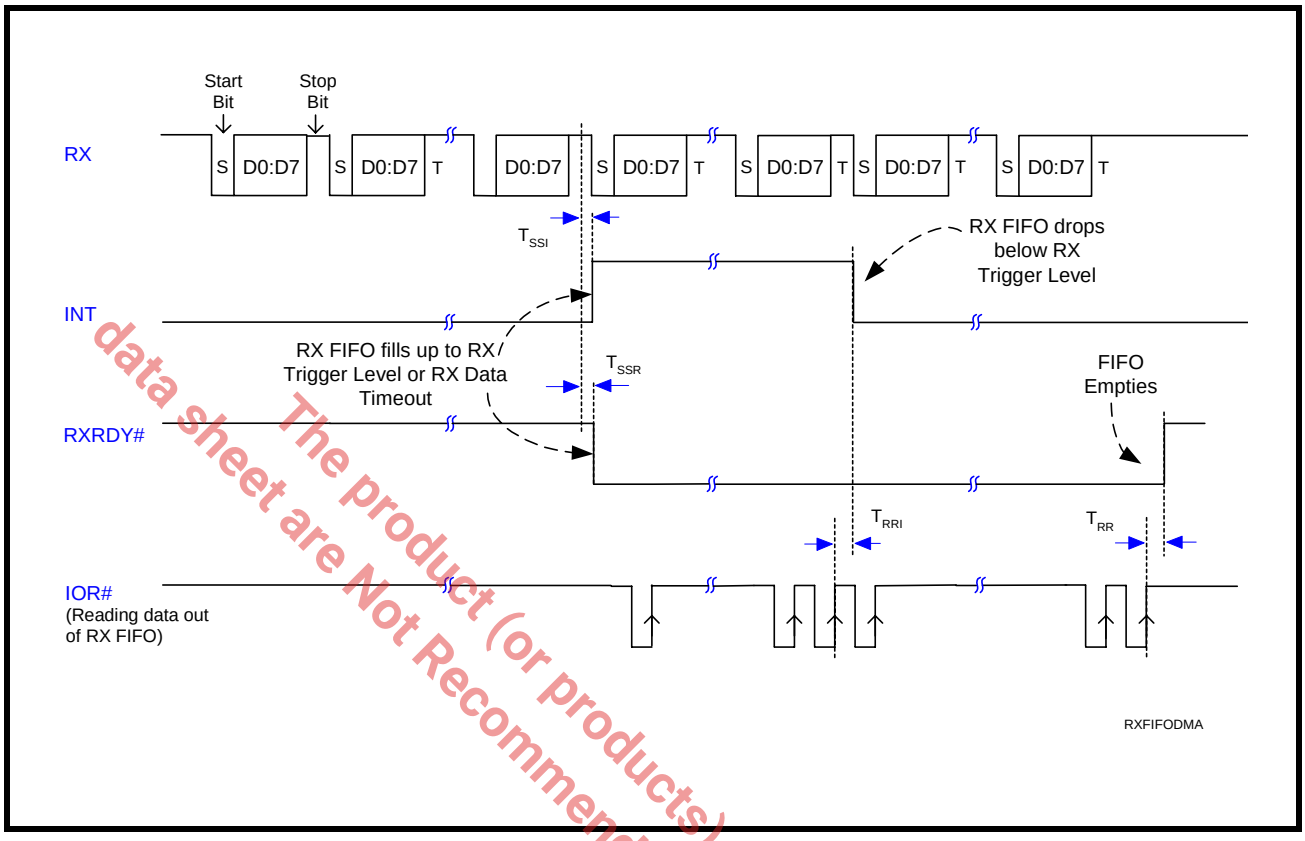
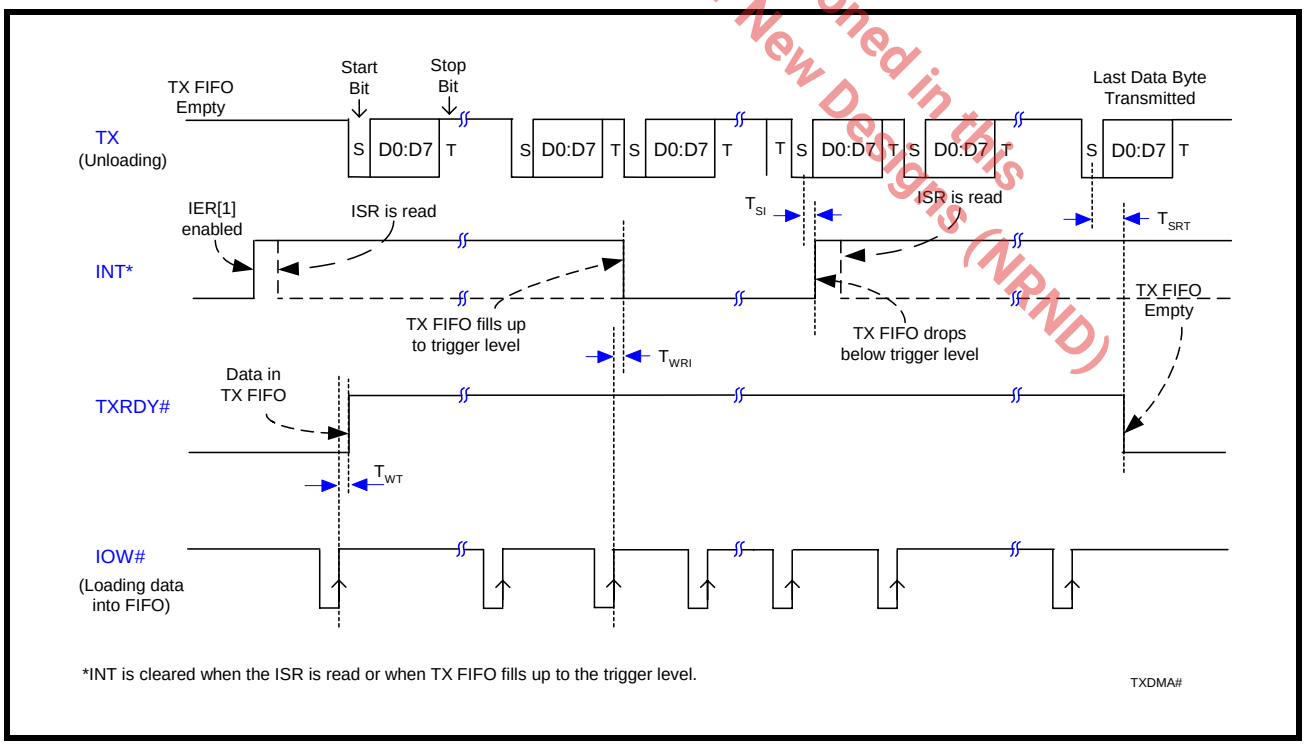
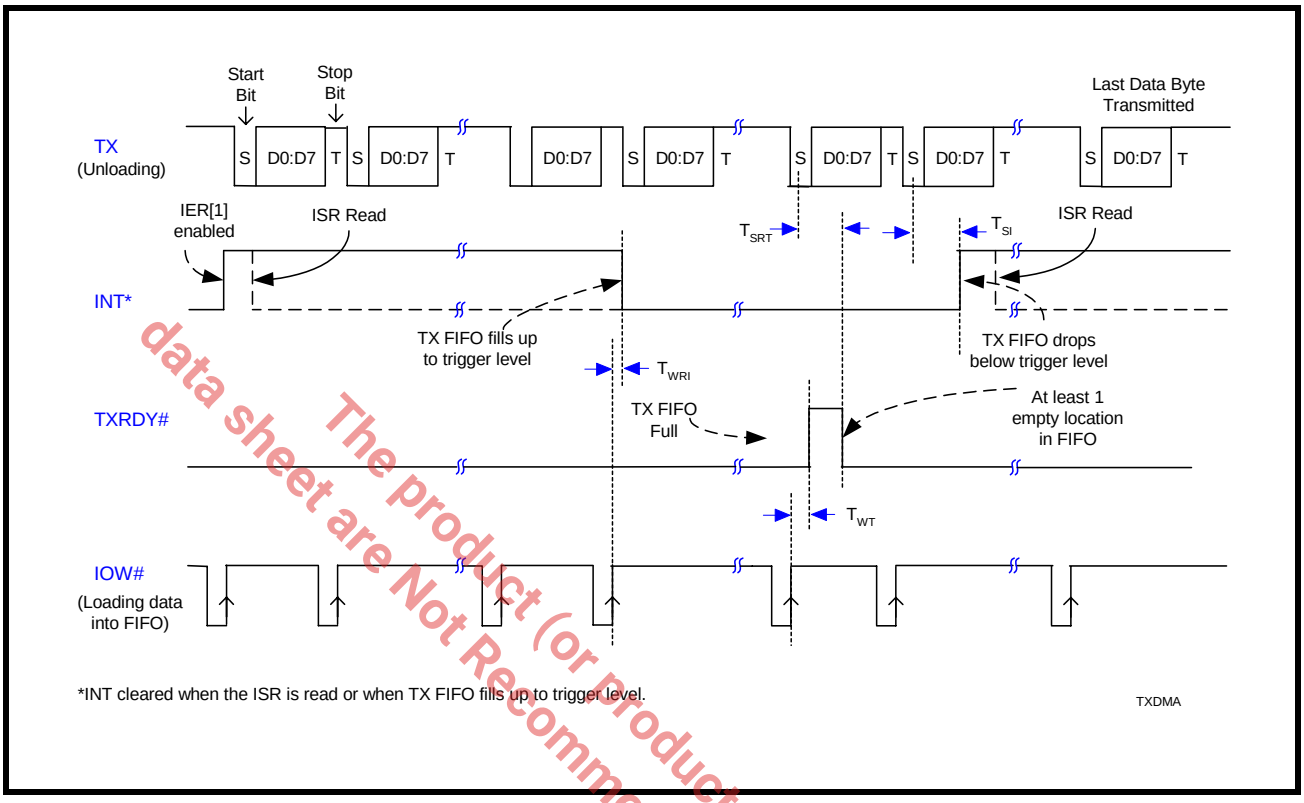


FIGURE 25. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED] FOR CHANNELS A-D



data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

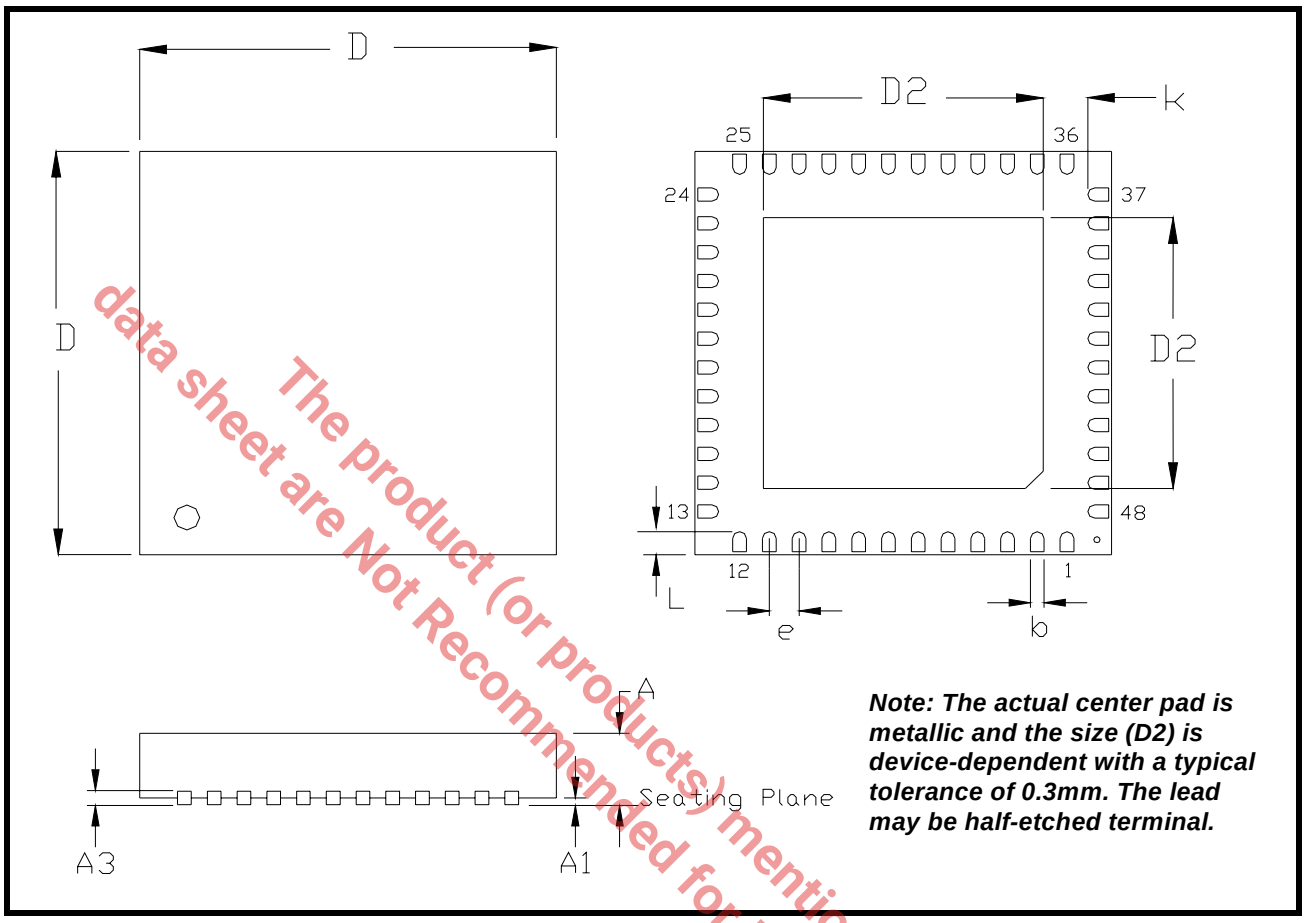
FIGURE 26. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED] FOR CHANNELS A-D



data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

PACKAGE DIMENSIONS

48 LEAD QUAD FLAT NO LEAD (7 x 7 x 0.9 mm, 0.50 mm pitch QFN)



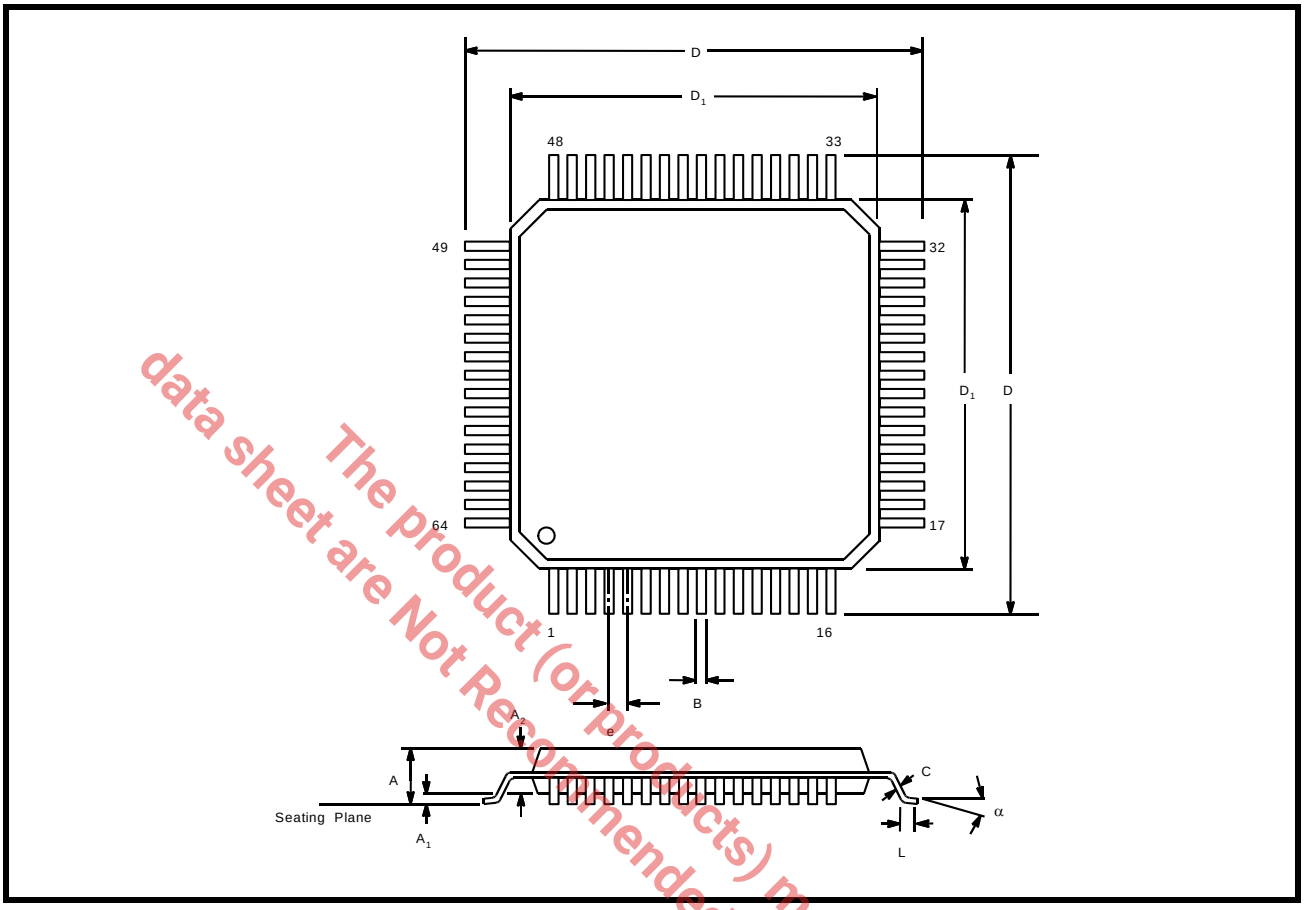
Note: The actual center pad is metallic and the size (D2) is device-dependent with a typical tolerance of 0.3mm. The lead may be half-etched terminal.

The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.006	0.010	0.15	0.25
D	0.270	0.281	6.85	7.15
D2	0.201	0.209	5.10	5.30
b	0.007	0.012	0.18	0.30
e	0.0197 BSC		0.50 BSC	
L	0.012	0.020	0.30	0.50
k	0.008	-	0.20	-

64 LEAD LOW-PROFILE QUAD FLAT PACK (10 x 10 x 1.4 mm LQFP)

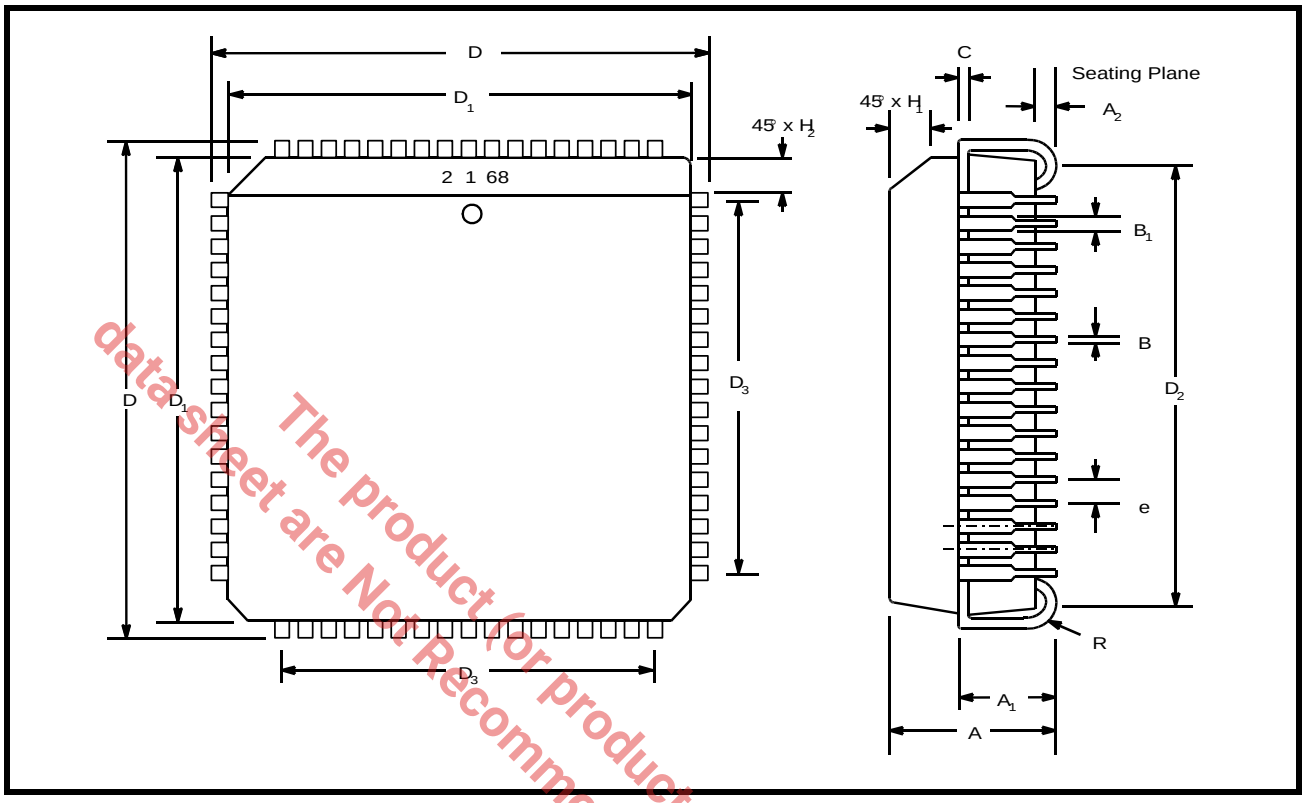


data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

68 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

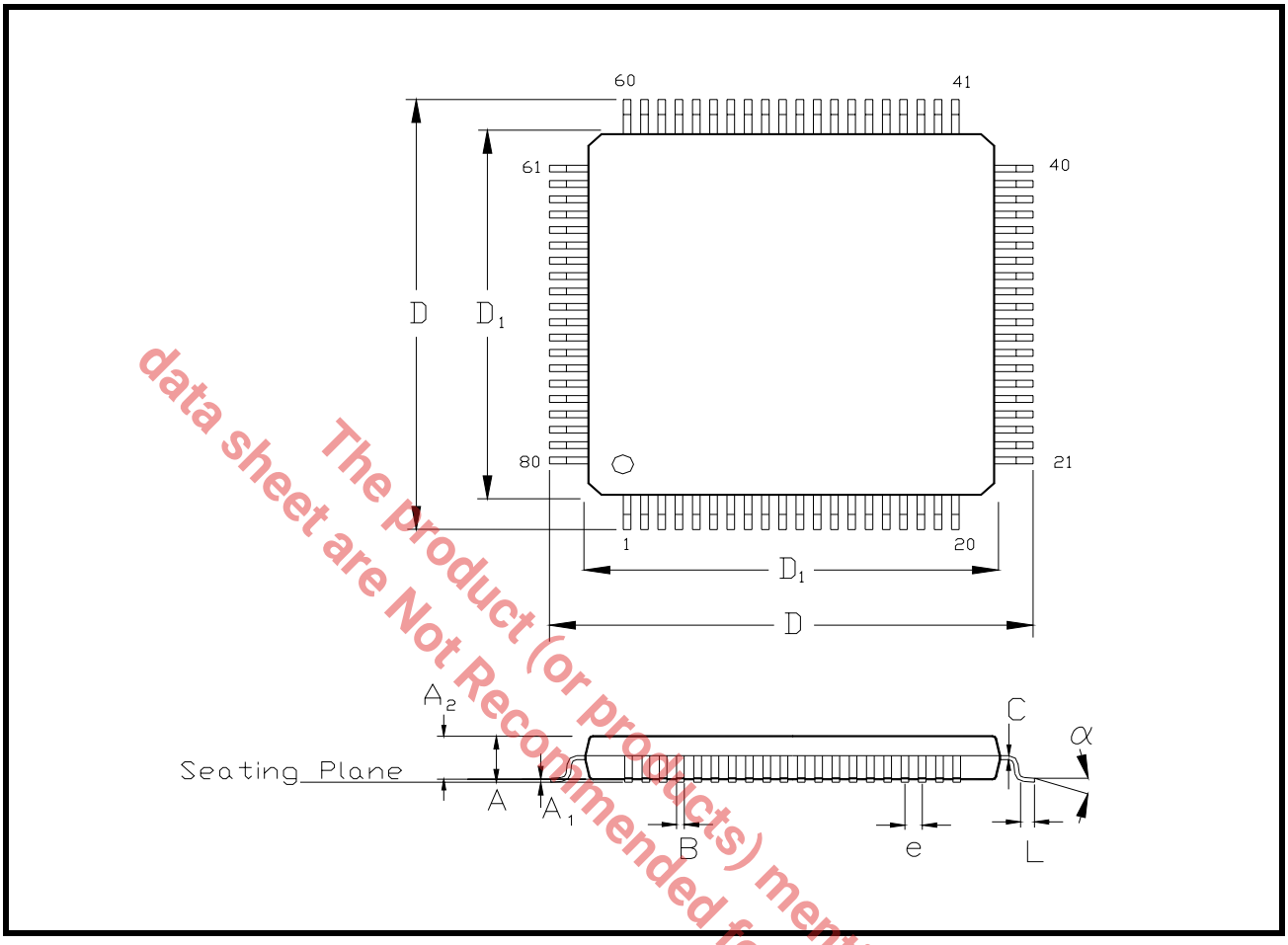


datasheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

Note: The control dimension is the inch column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.19	5.08
A_1	0.090	0.130	2.29	3.30
A_2	0.020	---.	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.985	0.995	25.02	25.27
D_1	0.950	0.958	24.13	24.33
D_2	0.890	0.930	22.61	23.62
D_3	0.800 typ.		20.32 typ.	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

80 LEAD PLASTIC QUAD FLAT PACK (12 mm x 12 mm LQFP, 1.4 mm Form)

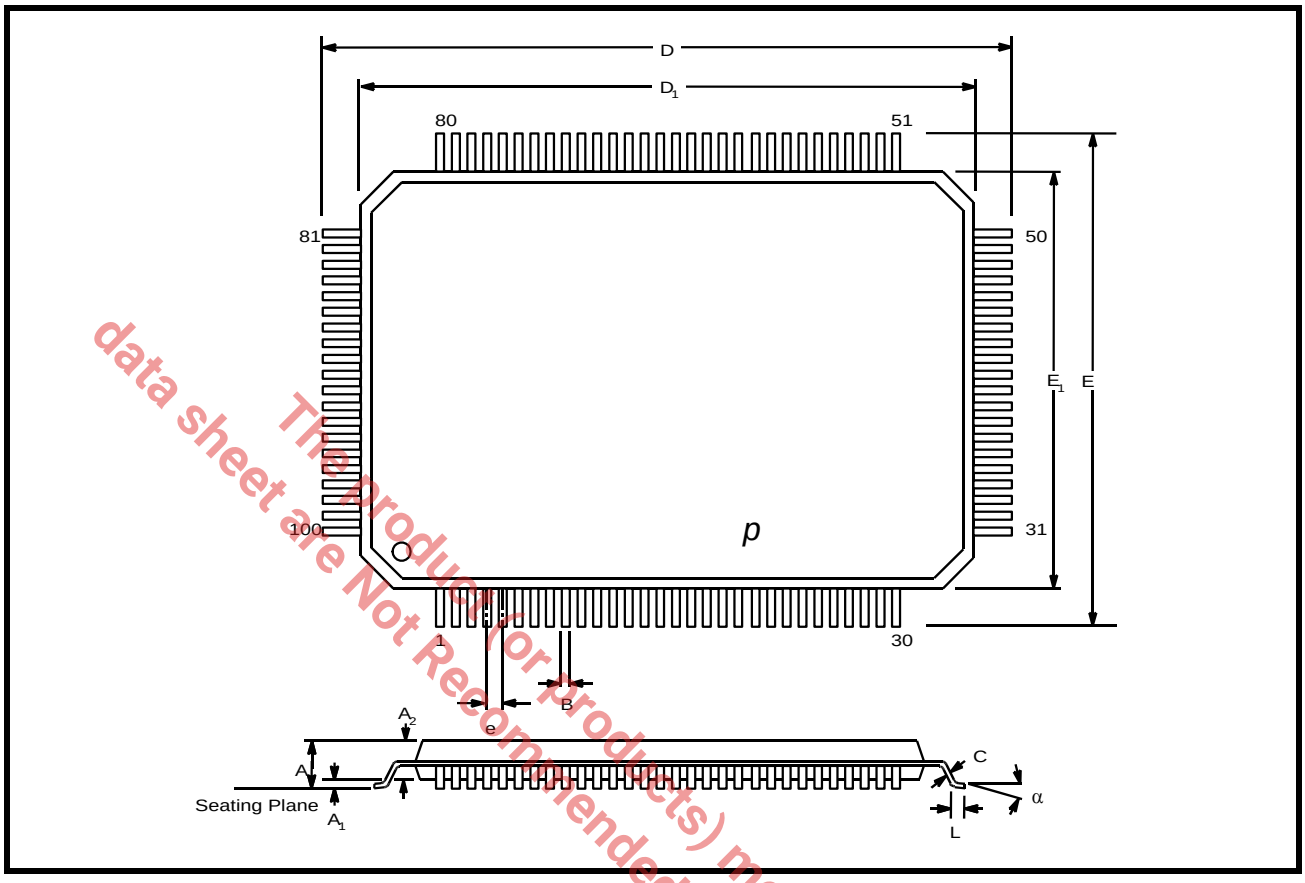


data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

Note: The control dimension is in the millimeter column

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.543	0.559	13.80	14.20
D1	0.465	0.480	11.80	12.20
e	0.0197 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

100 LEAD PLASTIC QUAD FLAT PACK (14 mm x 20 mm QFP, 1.95 mm Form)



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Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.102	0.134	2.60	3.40
A_1	0.002	0.014	0.05	0.35
A_2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
C	0.004	0.009	0.11	0.23
D	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10
E	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC	
L	0.029	0.040	0.73	1.03
α	0°	7°	0°	7°

REVISION HISTORY

DATE	REVISION	DESCRIPTION
April 2006	Rev A1.0.0	Advanced Datasheet.
May 2006	Rev P1.0.0	Preliminary Datasheet.
July 2006	Rev P1.0.1	Updated AC Electrical Characteristics.
October 2006	Rev P1.0.2	Updated DC Electrical Characteristics.
January 2007	Rev 1.0.0	Final Datasheet.
May 2007	Rev 1.0.1	Updated QFN package dimensions drawing to show minimum "k" parameter.
September 2007	Rev 1.0.2	Corrected RX and TX FIFO trigger levels.

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