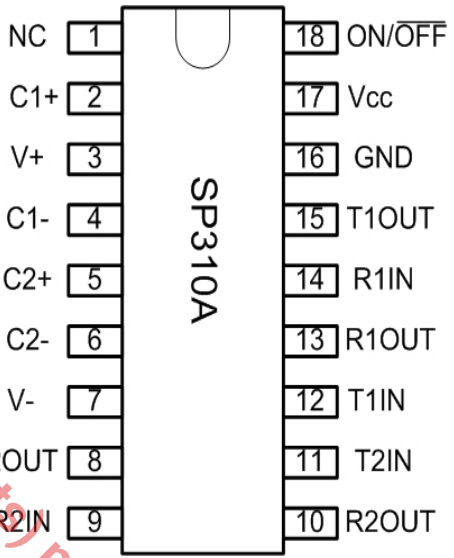
MAXLINEAR

SP233A

Enhanced RS-232 Line Drivers/Receivers

FEATURES

- Operates from a Single +5V Power Supply
- Meets all RS-232F and ITU V.28 Specifications
- Operates with 0.1µF Ceramic Capacitors
- No External Capacitors required (SP233A)
- Low Power Shutdown (SP310A, SP312A)
- High Data Rate - 120kbps under load
- Low power CMOS Operation
- +/-2kV Human Body Model ESD Protection
- Lead Free packaging available



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

DESCRIPTION

The SP233A / SP310A / SP312A devices are a family of line driver and receiver pairs that meets the specifications of RS-232 and V.28 serial protocols. The devices are pin-to-pin compatible with popular industry standard pinouts. The SP233A / SP310A / SP312A offer 120kbps data rate under load, small ceramic type 0.1µF charge pump capacitors and overall ruggedness for comercial applications. Features include Exar's BiCMOS design allowing for low power operation without sacrificing performance. These devices are available in plastic DIP and SOIC Wide packages operating over the commercial and industrial temperature ranges.

SELECTION TABLE

Model	Number of RS-232		No. of RX active in Shutdown	No. of External 0.1µF Capacitors	Shutdown	WakeUp	TTL Tri-State
	Drivers	Receivers					
SP233A	2	2	N/A	0	No	No	No
SP310A	2	2	0	4	Yes	No	Yes
SP312A	2	2	2	4	Yes	Yes	Yes

SP310A and SP312A are obsolete

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below are not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect reliability.

Supply Voltage (V_{CC}).....+ 6V
V+..... (Vcc-0.3V) to +11.0V
V- .....-11.0V
Input Voltages
Tin.....-0.3V to (Vcc + 0.3V)
Rin.....+/-30V
Output Voltages
Tout.....(V+, +0.3V) to (V-, -0.3V
Rout.....-0.3V to (Vcc + 0.3V)

Short Circuit duration
Tout.....Continuous
Package Power Dissipation:
Plastic DIP.....375mW
(derate 7mW/°C above +70°C)
Small Outline.....375mW
(derate 7mW/°C above +70°C)
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s)..... +300°C

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ELECTRICAL CHARACTERISTICS

Vcc=5V ±10%, 0.1µF charge pump capacitors, T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are Vcc=5V and T_A=25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TTL INPUT					
Logic Threshold LOW	TIN, $\overline{EN}$, $\overline{SD}$, $\overline{ON/OFF}$			0.8	Volts
Logic Threshold HIGH	TIN, $\overline{EN}$, $\overline{SD}$, $\overline{ON/OFF}$	2.0			Volts
Logic Pull-Up Current	TIN = 0V		15	200	µA
TTL OUTPUT					
Output Voltge LOW	I_{OUT} = 3.2mA: Vcc = +5V			0.4	Volts
Output Voltage HIGH	I_{OUT} = -1.0mA	3.5			Volts
Leakage Current; T_A=25°C	$\overline{EN}$ = Vcc, 0V ≤ V_{OUT} ≤ Vcc SP310A and SP312A only		0.05	+/-10	µA
RS-232 OUTPUT					
Output Voltage Swing	All Transmitter outputs loaded with 3k ohms to GND	+/-5.0	+/-9V		Volts
Output Resistance	Vcc = 0V, Vout = +/-2V	300			Ohms
Output Short Circuit Current	Infinite Duration		+/-18		mA
Maximum Data Rate	CL = 2500pF, RL = 3kΩ	120	240		kbps
RS-232 INPUT					
Voltage Range		-25		+25	Volts
Voltage Threshold LOW	Vcc = 5V, T_A=25°C	0.8	1.2		Volts
Voltage Threshold HIGH	Vcc = 5V, T_A=25°C		1.7	2.4	Volts
Hysteresis	Vcc = 5V, T_A=25°C	0.2	0.5	1.0	Volts
Resistance	T_A=25°C, -25V ≤ V_{IN} ≤ +25V	3	5	7	kΩ

ELECTRICAL CHARACTERISTICS

Vcc=5V ±10%, 0.1µF charge pump capacitors, TMIN to TMAX, unless otherwise noted, Typical values are Vcc=5V and TA=25°C

Parameter	TEST CONDITIONS	MIN	TYP	MAX	Unit
DYNAMIC CHARACTERISTICS					
Driver Propagation Delay	TTL to RS_232; CL = 50pF		1.5	3.0	µs
Receiver Propagation Delay	RS-232 to TTL,		0.1	1.0	µs
Instantaneous Slew Rate	CL = 10pF, RL = 3-7kΩ			30	V/ µs
Transition Region Slew Rate	CL = 2500pF, RL = 3kΩ; Measured from +3V to -3V or -3V to +3V		10		V/ µs
Output Enable Time	SP310A and SP312A only		400		ns
Output Disable Time	SP310A and SP312A only		250		ns
POWER REQUIREMENTS					
Vcc Power Supply Current	No Load, Vcc = 5V, TA=25°C		10	15	mA
Vcc Power Supply Current, Loaded	All Transmitters RL = 3kΩ, TA=25°C		25		mA
Shutdown Supply Current SP310A and SP312A only	Vcc = 5V, TA=25°C		1	10	µA

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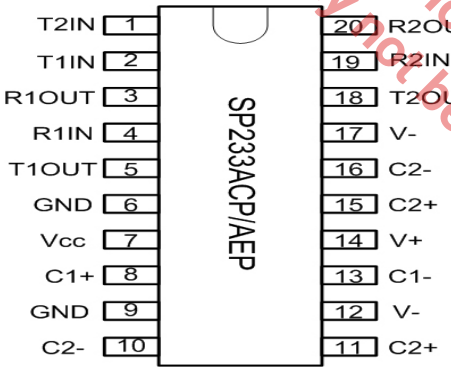
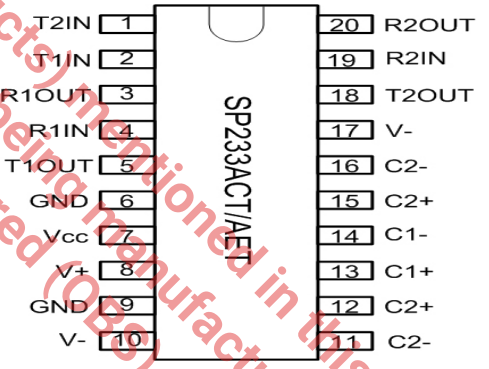
PIN ASSIGNMENTS

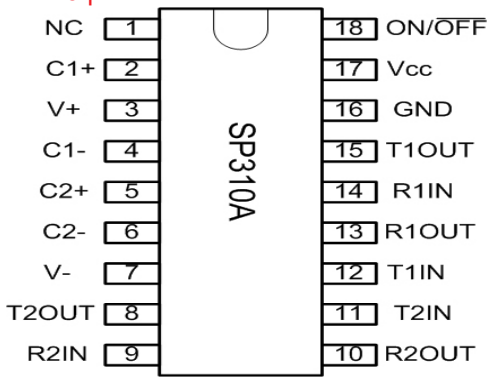


20 pin PDIP

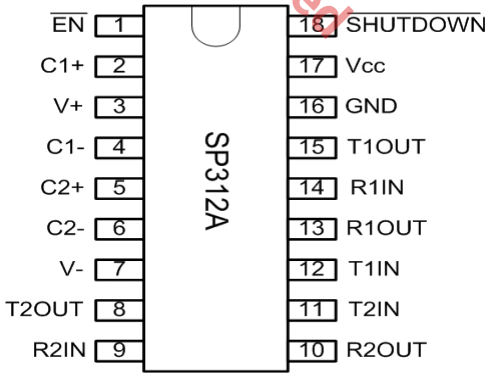
20 pin PDIP version is obsolete



20 pin WSOIC



18 pin WSOIC



18 pin WSOIC

SP310A and SP312A are obsolete

DETAILED DESCRIPTION

The SP233A, SP310A and SP312A devices are a family of line driver and receiver pairs that meet the EIA/TIA-232 and V.28 serial communication protocols. These devices are pin-to-pin compatible with popular industry standards. The SP233A, SP310A and SP312A devices offer a 120kbps data rate, 10V/µs slew rate and an on-board charge pump that operates from a single 5V supply using 0.1µF ceramic capacitors. The ESD tolerance has been improved on these devices to +/-2kV Human Body Model.

The SP233A device provides internal charge pump capacitors. The SP310A provides an ON/$\overline{OFF}$ input that simultaneously disables the internal charge pump circuit and puts all transmitter and receiver outputs into a high impedance state. The SP312A is identical to the SP310 but with seperate tri-state and shutdown inputs.

Theory Of Operation

The SP233A, SP310A and SP312A devices are made up of three basic circuit blocks: 1. Drivers, 2. Receivers, and 3. charge pump.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the driver output voltage swing is +/-9V. Even under worst case loading conditions of 3k ohms and 2500pF, the driver output is guaranteed to be +/-5.0V minimum, thus satisfying the RS-232 specification. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability.

The drivers can guarantee output data rates of 120kbps under worst case loading of 3k ohms and 2500pF.

The Slew rate of the driver output is internally limited to 30V/ µs in order to meet the EIA standards (EIA-232F). Additionally, the driver outputs LOW to HIGH transition meets the montonic output requirements of the standard.

Receivers

The receivers convert EIA/TIA-232 signal levels to TTL or CMOS logic output levels. Since the input is usually from a transmission line, where long cable length and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kohm pull-down resistor to ground will commit the output of the receiver to a HIGH state.

Charge pump

The charge pump is a patented design and uses a unique approach compared to older less efficiant designs. The charge pump requires 4 external capacitors and uses a four phase voltage shifting technique. The internal power supply consists of a dual charge pump that provides a driver output voltage swing of +/-9V. The internal oscillator controls the four phases of the voltage shifting. A description of each phase follows:

Phase 1

Vss charge store and double: The positive terminals of capacitors C1 and C2 are charged from Vcc with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1- is superimposed onto C2-. Since C2+ is still connected to Vcc the voltage potential across C2 is now 2 x Vcc.

Phase 2

Vss transfer and invert: Phase two connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground. This transfers the doubled and inverted (V-) voltage onto C4. Meanwhile, capacitor C1 is charged from Vcc to prepare it for its next phase.

Phase 3

Vdd charge store and double: Phase three is identical to the first phase. The positive terminals of C1 and C2 are charged from Vcc with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1- is superimposed onto C2-. Since C2+ is still connected to Vcc the voltage potential across capacitor C2 is now 2 x Vcc.

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Phase 4
Vdd transfer: The fourth phase connects the negative terminal of C2 to ground and the positive terminal of C2 to the Vdd storage capacitor. This transfers the doubled (V+) voltage onto C3. Meanwhile, capacitor C1 is charged from Vcc to prepare it for its next phase.

The clock rate for the charge pump typically operates at greater than 15kHz allowing the pump to run efficiently with small 0.1uF capacitors. Efficient operation depends on rapid charging and discharging of C1 and C2, therefore capacitors should be mounted as close as possible to the IC and have low ESR (equivalent series resistance). Inexpensive surface mount, ceramic capacitors are ideal for using on charge pump. If polarized capacitors are used the positive and negative terminals should be connected as shown in the typical operating circuit. A diagram of the individual phases are shown in Figure 1.

Shutdown ($\overline{SD}$) and Enable ($\overline{EN}$) features for the SP310A and SP312A
Both the SP310A and SP312A have a shutdown / standby mode to conserve power in battery-powered applications. To activate the shutdown mode, which stops the operation of the charge pump, a logic "0" is applied to the appropriate control line. For the SP310A, this control line is the ON/$\overline{OFF}$ (pin 18) input. Activating the shutdown mode puts the SP310A transmitter and receiver ouptuts into a high impedance condition. For the SP312A, this control line is the $\overline{SHUTDOWN}$ (pin18) input; this also puts the transmitter outputs in a tri-state mode. The receiver outputs can be tri-stated seperately during normal operation or shutdown by applying a logic "1" on the $\overline{EN}$ line (pin 1).

Wake-Up Feature for the SP312A
The SP312A has a wake-up feature that keeps the receivers active when the device is placed into shutdown. Table 1 defines the truth table for the Wake-Up function. When only the receivers are activated, the SP312A typically draws less than 5uA supply current. In the case of when a modem is interfaced to a computer in power down mode, the Ring Indicator (RI) signal from the modem would be used to "wake-up" the computer, allowing it to accept data transmission.

After the ring indicator has propagated through the SP312A receiver, it can be used to trigger the power management circuitry of the computer to power up the microprocessor, and bring the $\overline{SD}$ pin of the SP312A to a logic high, taking it out of the shutdown mode. The receiver propagation delay is typically 1us. The enable time for V+ and V- is typically 2ms. After V+ and V- have settled to their final values, a signal can be sent back to the modem on the data terminal ready (DTR) pin signifying that the computer is ready to accept the transmit data.

$\overline{SD}$	$\overline{EN}$	Power Up/Down	Receiver outputs
0	0	Down	Enabled
0	1	Down	Tri-state
1	0	Up	Enabled
1	1	Up	Tri-state

Table 1. Wake-up Function truth table

Pin Strapping for the SP233ACT/ACP
The SP233A packaged in a 20 pin SOICW package (SP233ACT) has a slightly different pinout than the SP233A in PDIP packaging (SP233ACP). To operate properly, the following pairs of pins must be externally wired together as noted in table 2:

Pins Wired Together	SOICW	PDIP
Two V- pins	10 & 17	12 & 17
Two C2+ pins	12 & 15	11 & 15
Two C- pins	11 & 16	10 & 16
	No Connections for Pins 8, 13 and 14	
	Connect Pins 6 and 9 to GND	

Table 2. Pin Strapping table for SP233A

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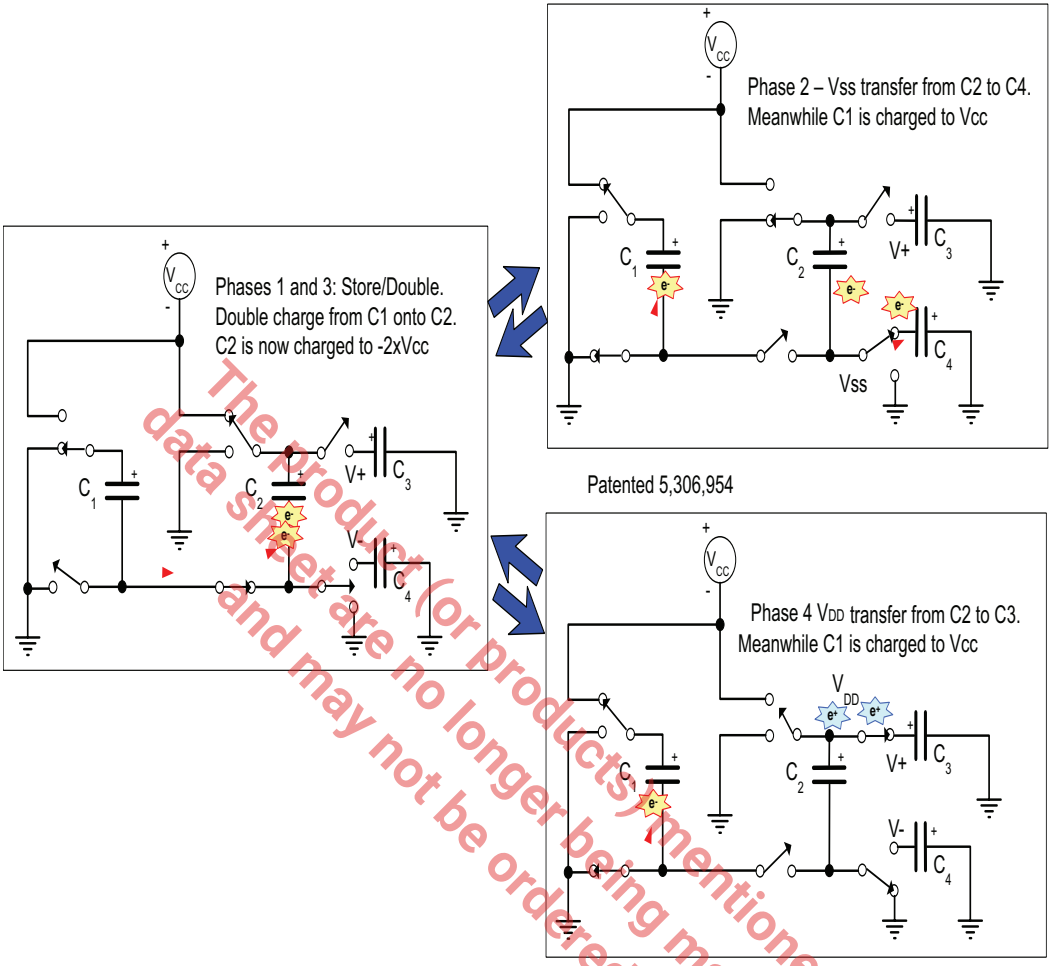

Figure 1. Charge pump phases

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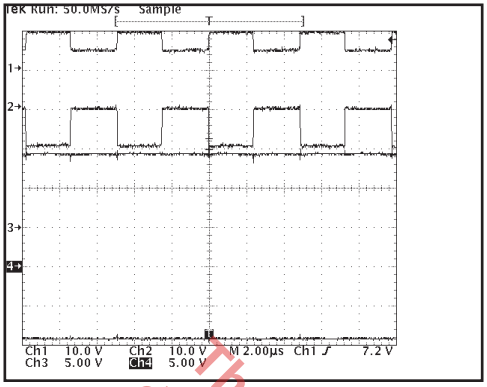

Figure 2, SP233A Charge pump waveforms- no load (1 = C1+, 2 = C2+, 3 = V+, 4 = V-).

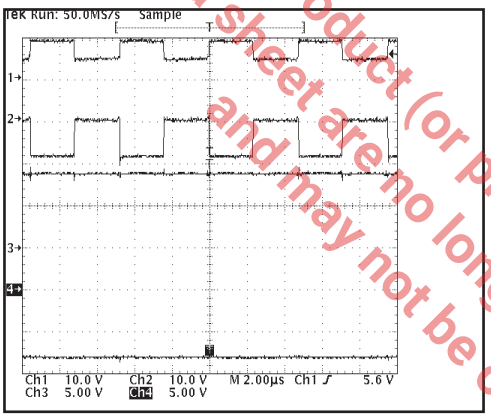

Figure 3, SP233A Charge pump waveforms when fully loaded with 3Kohms (1 = C1+, 2 = C2+, 3 = V+, 4 = V-).

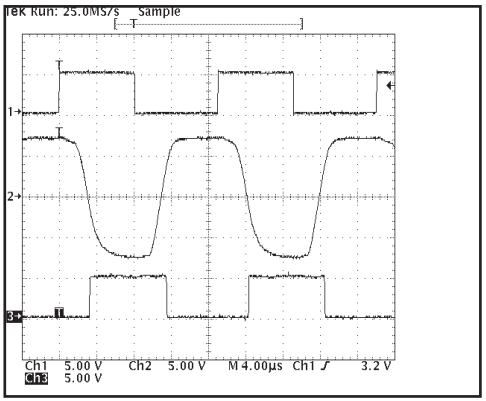

Figure 4, Loopback results at 60KHZ and 2500pF load (1 = TXin, 2 = TXout/RXin, 3 = RXout).

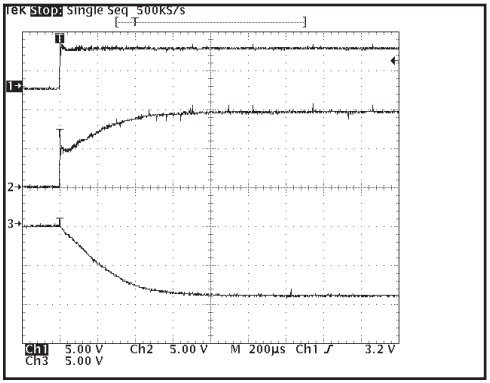

Figure 5, Charge pump outputs at start up (1 = Vcc, 2 = V+, 3 = V-).

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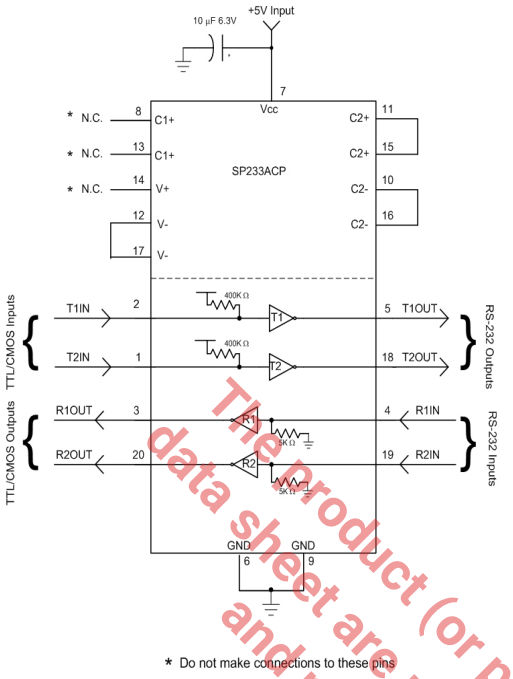

Figure 6, SP233ACP Typical Application circuit

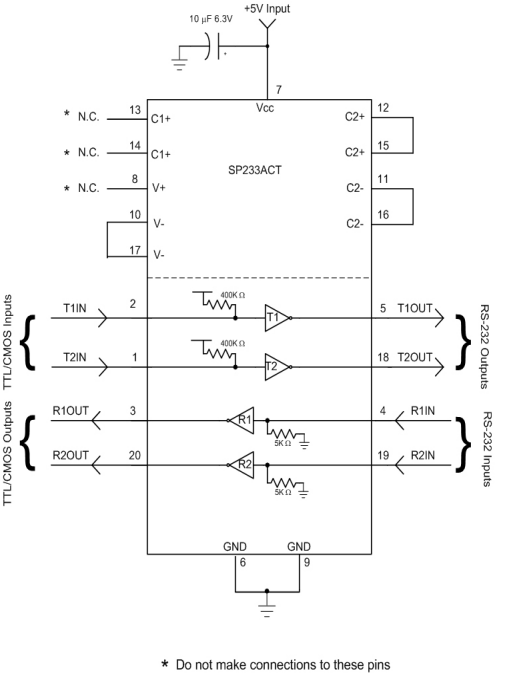

Figure 8, SP233ACT Typical Application circuit

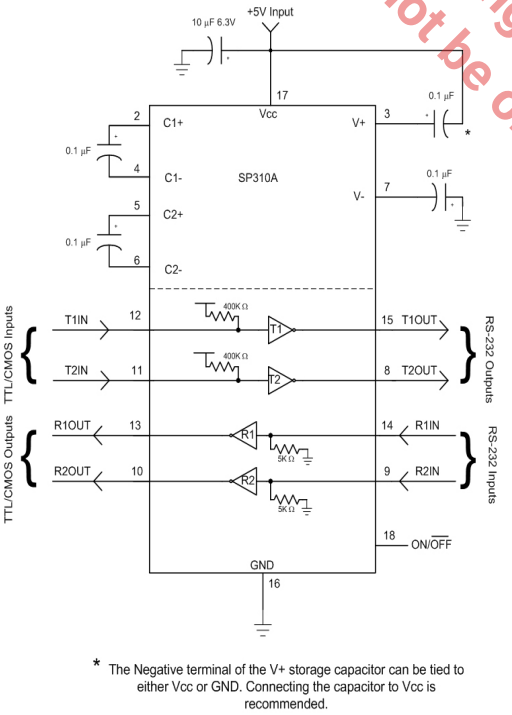

Figure 7, SP310A Typical Application circuit

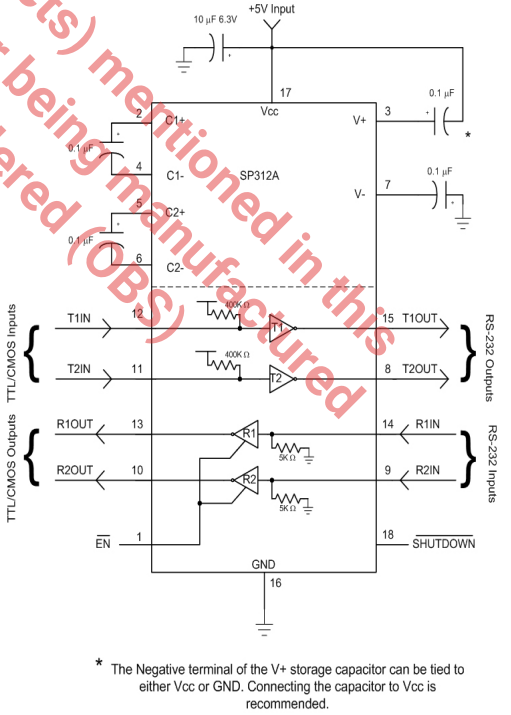

Figure 9, SP312A Typical Application circuit

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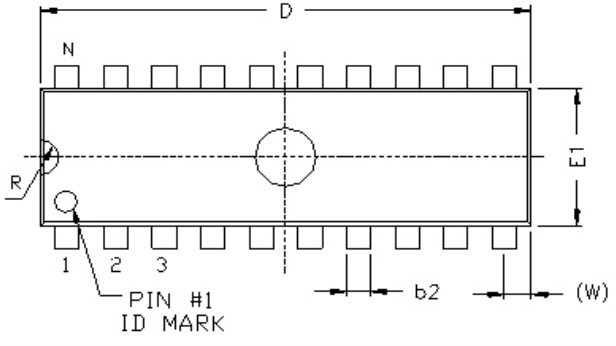
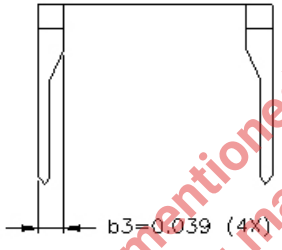
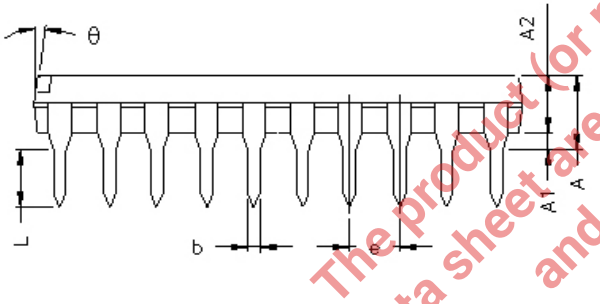
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/28/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/27/07	JL

REMARKS:
FOR 8LD AND 16LD
ALL END LEADS (4X)
ARE HALF LEAD TYPES

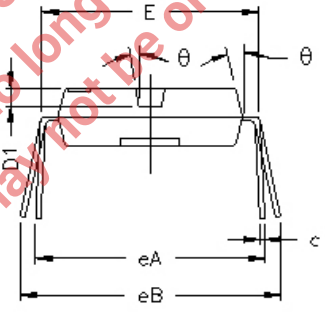


Top View





Side View



Front View

20 Pin PDIP JEDEC MS-001 Variation AD

SYMBOLS	DIMENSIONS IN INCH (Control Unit)			DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.210	—	—	5.33
A1	0.015	—	—	0.38	—	—
A2	0.115	0.130	0.195	2.92	3.30	4.95
b	0.014	0.018	0.022	0.36	0.46	0.56
b2	0.045	0.060	0.070	1.14	1.52	1.78
c	0.008	0.010	0.014	0.20	0.25	0.36
D1	0.030	—	0.060	0.76	—	1.52
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
e	0.100 BSC			2.54 BSC		
eA	0.300 BSC			7.62 BSC		
eB	—	—	0.430	—	—	10.92
L	0.115	0.130	0.150	2.92	3.30	3.81
W	0.075 REF			1.91 REF		
R	0.030 BSC			0.76 BSC		
θ	4°	7°	10°	4°	7°	10°
D	0.980	1.030	1.060	24.89	26.16	26.92
N	20			20		

20 pin PDIP version is obsolete

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

EXAR Powering Connectivity	EXAR CORPORATION		
	20 PIN PDIP PACKAGE OUTLINE		
Packaging Approval:		Drawing No:	20-PIN PDIP
By JL	Date 11/27/07	Revision: B	Sheet: 1 OF 1

REVISION HISTORY			
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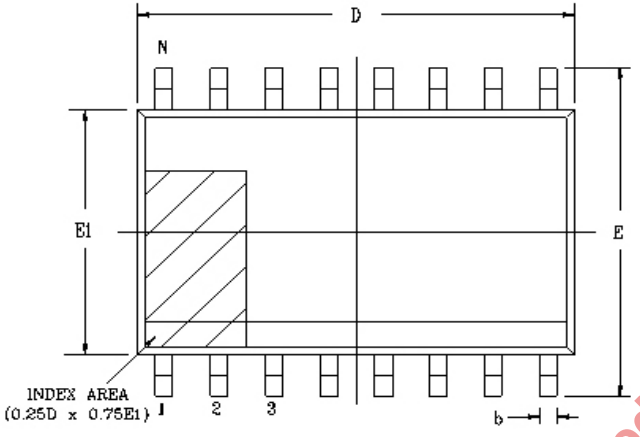
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL



Top View

20 Pin SOICW JEDEC MS-013 Variation AC						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	12.80 BSC			0.504 BSC		
N	20			20		

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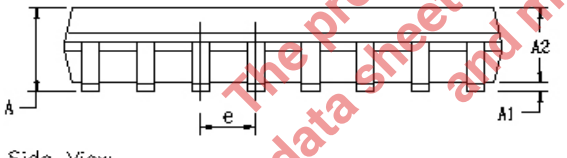
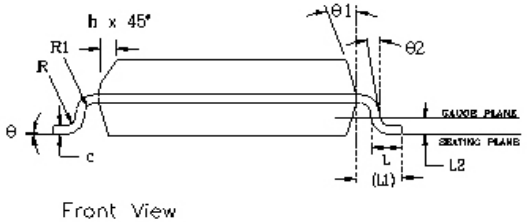


Side View



Front View

EXAR	EXAR CORPORATION		
	20 PIN SOICW PACKAGE OUTLINE		
Packaging Approval:	Drawing No: 20-PIN SOICW		
By: JL	Date: 11/28/07	Revision: B	Sheet: 1 OF 1

SP310A and SP312A WSOIC18 are obsolete

REVISION HISTORY			
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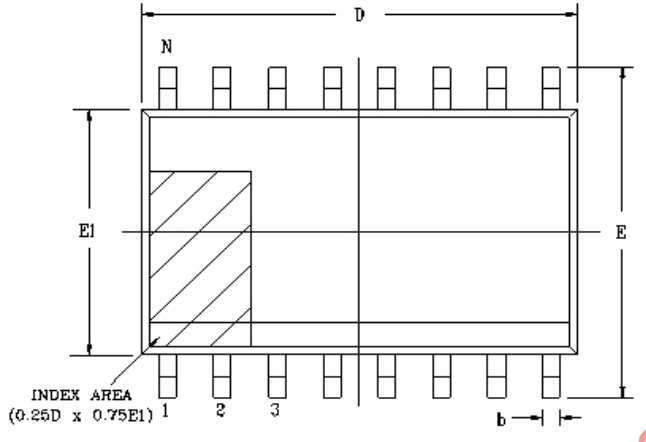
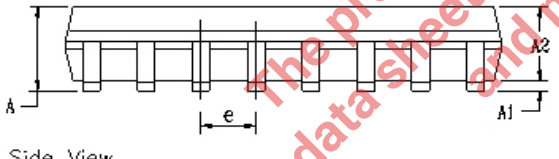
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL



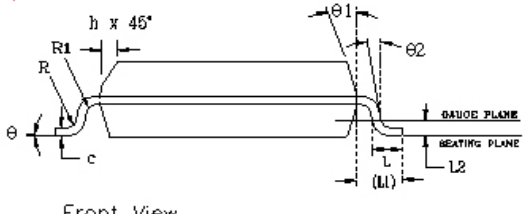
Top View

18 Pin SOICW JEDEC MS-013 Variation AB						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	11.55 BSC			0.455 BSC		
N	18			18		

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).



Side View



Front View

EXAR Powering Connectivity	EXAR CORPORATION		
	18 PIN SOICW PACKAGE OUTLINE		
Packaging Approval:		Drawing No:	18-PIN SOICW
By: JL	Date: 11/21/07	Revision: B	Sheet: 1 OF 1

Part number	Temperature range	Package	Packaging Method	Lead-Free[2]
SP233ACT-L	0 to +70°C	20 pin SOICW	Tube	Yes
SP233ACT-L/TR	0 to +70°C	20 pin SOICW	Tape and Reel	Yes
SP233AET-L	-40 to +85°C	20 pin SOICW	Tube	Yes
SP233AET-L/TR	-40 to +85°C	20 pin SOICW	Tape and Reel	Yes

NOTES:
1. Refer to www.maxlinear.com/SP233A for the most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.
3. SP310A, SP312A and 20 pin PDIP versions of SP233A are obsolete.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

REVISION HISTORY		
Date	Revision	Description
1-31-07	Rev B	Original SP232A/233A/310A/312A Sipex Data sheet
5-13-08	100	Generate new SP233A/310A/312A Data sheet using Exar format.
6-03-11	101	Add Revision History table. Remove SP310ACP-L option per PDN 110510-01.
3-20-20	102	Update to MaxLinear logo. Update Ordering Information.

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