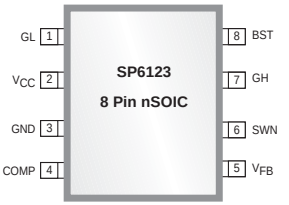
Low Voltage, Synchronous Step-Down PWM Controller

Ideal for 2A to 10A, Small Footprint, DC-DC Power Converters

FEATURES

- Optimized for Single Supply, 3V - 5.5V Applications
- High Efficiency: Greater Than 95% Possible
- Accurate Fixed 300kHz (SP6123) or 500kHz (SP6123A) Frequency Operation
- Fast Transient Response
- Internal Soft Start Circuit
- Accurate 0.8V Reference Allows Low Output Voltages
- Resistor Programmable Output Voltage
- Loss-less Current Limit with High Side $R_{DS(ON)}$ Sensing
- Hiccup Mode Current Limit Protection
- Dual N-Channel MOSFET Synchronous Driver
- Quiescent Current: 500µA, 30µA in Shutdown
- 8-Pin Surface Mount Package



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APPLICATIONS

- DSP
- Microprocessor Core
- I/O & Logic
- Industrial Control
- Distributed Power
- Low Voltage Power

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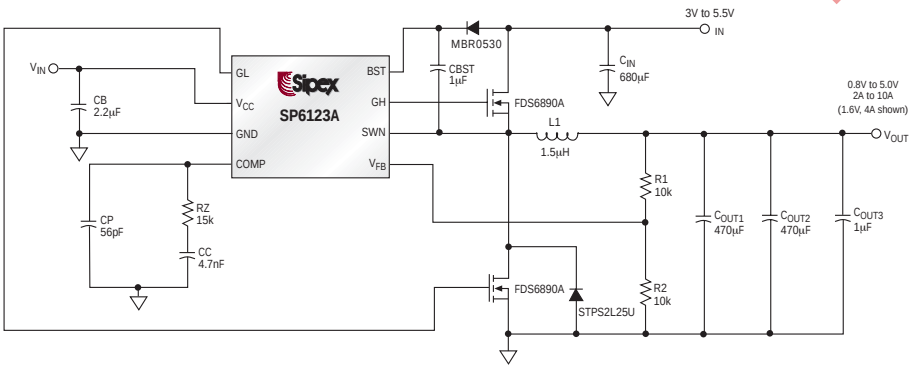
DESCRIPTION

The SP6123 is a fixed frequency, voltage mode, synchronous PWM controller designed to work from a single 5V or 3.3V input supply, providing excellent AC and DC regulation for high efficiency power conversion. Requiring only few external components, the SP6123 packaged in an 8-pin NSOIC, is especially suited for low voltage applications where cost, small size and high efficiency are critical. The operating frequency is internally set to 300kHz (SP6123) or 500kHz (SP6123A), allowing small inductor values and minimizing PC board space. The SP6123 drives an all N-channel synchronous power MOSFET stage for improved efficiency and includes an accurate 0.8V reference for low output voltage applications.

TYPICAL APPLICATION CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 7V
BST 13.2V
BST-SWN 7V

All other pins ..... -0.3V to V_{CC} + 0.3V

Peak Output Current < 10µs
GH,GL 2A

Storage Temperature ..... -65°C to 150°C

Power Dissipation
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating. ..... 2kV HBM

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: 0°C < T_A < 70°C, 3.0V < V_{CC} < 5.5V, C_{COMP} = 22nF, CGH = CGL = 3.3nF, V_{FB} = 0.8V, SWN = GND=0V, typical value for design guideline only.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
QUIESCENT CURRENT					
V_{CC} Supply Current		0.5	1.0	mA	No Switching
V_{CC} Supply Current (Disabled)		30	60	µA	COMP = 0V
ERROR AMPLIFIER					
Error Amplifier Transconductance		0.6		mS	
COMP Sink Current	15	35	60	µA	V_{FB} = 0.9V, COMP = 0.9V, No Faults
COMP Source Current	15	35	60	µA	V_{FB} = 0.7V, COMP = 2V
COMP Output Impedance		3		MΩ	
V_{FB} Input Bias Current			100	nA	
Error Amplifier Reference	0.788	0.8	0.812	V	Trimmed with Error Amp in Unity Gain
OSCILLATOR & DELAY PATH					
Internal Oscillator Frequency	270	300	330	kHz	SP6123
Internal Oscillator Frequency	450	500	550	kHz	SP6123A
Max. Controlled Duty Cycle	90	93		%	
Minimum Duty Cycle			0	%	Comp=0.7V
Minimum GH Pulse Width		100	250	ns	V_{CC} > 4.5V, Ramp up COMP voltage until GH starts switching
CURRENT LIMIT					
Internal Current Limit Threshold	160	200	240	mV	V_{CC} - V_{SWN} ; Temp = 25 °C; V_{BST} - V_{CC} > 2.5V
Current Limit Threshold Temperature Coefficient		0.34		%/C	
Current Limit Time Constant		15		us	
SOFT START, SHUTDOWN, UVLO					
Internal Soft Start Slew Rate SP6123A SP6123	 0.2 0.1	 0.60 0.3	 0.95 0.6	 V/ms V/ms	
COMP Discharge Current	185			µA	COMP = 0.5V, Fault Initiated
COMP Clamp Voltage	0.55	0.65	0.75	V	V_{FB} = 0.9V
COMP Clamp Current	10	30	65	µA	COMP = 0.5V, V_{FB} = 0.9V
Shutdown Threshold Voltage	0.29	0.34	0.39	V	Measured at COMP Pin
Shutdown Input Pull-up Current	2	5	10	µA	COMP = 0.2V, Measured at COMP pin
V_{CC} Start Threshold	2.63	2.8	2.95	V	
V_{CC} Stop Threshold	2.47	2.7	2.9	V	

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified: 0°C < T_A < 70°C, 3.0V < V_{CC} < 5.5V, C_{COMP} = 22nF, CGH = CGL = 3.3nF, V_{FB} = 0.8V, SWN = GND=0V, typical value for design guideline only.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GATE DRIVERS					
GH Rise Time			110	ns	V_{CC} > 4.5V
GH Fall Time			110	ns	V_{CC} > 4.5V
GL Rise Time			110	ns	V_{CC} > 4.5V
GL Fall Time			110	ns	V_{CC} > 4.5V
GH to GL Non-Overlap Time		100		ns	V_{CC} > 4.5V
GL to GH Non-Overlap Time		100		ns	V_{CC} > 4.5V

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PIN DESCRIPTION

PIN N0.	PIN NAME	DESCRIPTION
1	GL	High current driver output for the low side MOSFET switch. It is always low if GH is high. GL swings from GND to V_{CC}.
2	V_{CC}	Positive input supply for the control circuitry and the low side gate driver. Properly bypass this pin to GND with a low ESL/ESR ceramic capacitor.
3	GND	Ground pin. Both power and control circuitry of the IC is referenced to this pin.
4	COMP	Output of the Error Amplifier. It is internally connected to the non-inverting input of the PWM comparator. A lead-lag network is typically connected to the COMP pinto compensate the feedback loop in order to optimize the dynamic performance of the voltage mode control loop. Sleep mode can be invoked by pulling the COMP pin below 0.3V with an external open-drain or open-collector transistor. Supply current is reduced to 30μA (typical) in shutdown. An internal 5μA pull-up ensures start-up.
5	V_{FB}	Feedback Voltage Pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck converter. The output voltage is sensed and can be adjusted through an external resistor divider.
6	SWN	Lower supply rail for the GH high-side gate driver. It also connects to the Current Limit comparator. Connect this pin to the switching node at the junction between the two external power MOSFET transistors. This pin monitors the voltage drop across the $R_{DS(ON)}$ of the high side N-channel MOSFET while it is conducting. When this drop exceeds the internal 200mV threshold, the overcurrent comparator sets the fault latch and terminates the output pulses. The controller stops switching and goes through a hiccup sequence. This prevents excessive power dissipation in the external power MOSFETS during an overload condition. An internal delay circuit prevents that very short and mild overload conditions, that could occur during a load transient, from activating the current limit circuit.
7	GH	High current driver output for the high side MOSFET switch. It is always low if GL is high or during a fault. GH swings from SWN to BST.
8	BST	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the application schematic of page #1. Voltage between BST and SWN should not exceed 5.5V.

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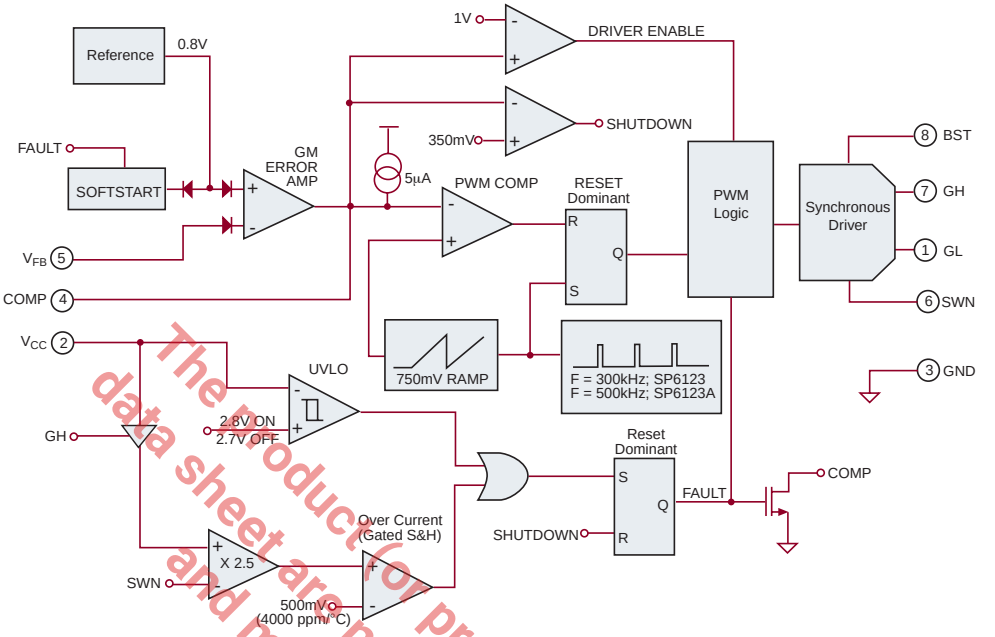
BLOCK DIAGRAM



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OPERATION

General Overview

The SP6123 is a constant frequency, voltage mode, synchronous PWM controller designed for low voltage, DC/DC step down converters. It is intended to provide complete control for a high power, high efficiency, precisely regulated output voltage from a highly integrated 8-pin solution.

The internal free-running oscillator accurately sets the PWM frequency at 300kHz or 500kHz without requiring any external elements and allows the use of physically small, low value external components without compromising performance. A transconductance amplifier is used for the error amplifier, which compares an attenuated sample of the output voltage with a precision, 0.8V reference voltage. The output of the error amplifier (COMP), is compared to a 0.75V peak-to-peak ramp waveform to provide PWM control. The COMP pin provides access to the output of the error amplifier and allows the use of external components to stabilize the voltage loop.

High efficiency is obtained through the use of synchronous rectification. Synchronous regulators replace the catch diode in the standard buck converter with a low $R_{DS(ON)}$ N-channel MOSFET switch allowing for significant efficiency improvements. The SP6123 includes two fast MOSFET drivers with internal non-overlap circuitry and drives a pair of N-channel power transistors. The SP6123 includes an internal soft-start circuit that provides controlled ramp up of the output voltage, preventing overshoot and inrush current at power up.

Current limiting is implemented by monitoring the voltage drop across the $R_{DS(ON)}$ of the high side N-channel MOSFET while it is conducting, thereby eliminating the need for an external sense resistor. The overcurrent comparator has a built-in threshold of 200mV .

When the overcurrent threshold is exceeded, the overcurrent comparator sets the fault latch and terminates the output pulses. The controller stops switching and goes through a hiccup sequence. This prevents excessive power dissipation in the external power MOSFETs during an overload condition. An internal delay circuit prevents that very short and mild overload conditions, that could occur during a load transient, activate the current limit circuit.

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OPERATION: continued

A low power sleep mode can be invoked in the SP6123 by externally forcing the COMP pin below 0.3V. Quiescent supply current in sleep mode is typically less than 30µA. An internal 5µA pull-up current at the COMP pin brings the SP6123 out of shutdown mode.

An internal 0.8V 1.5% reference allows output voltage adjustment for low voltage applications.

The SP6123 also includes an accurate under-voltage lockout that shuts down the controller when the input voltage falls below 2.7V. Output overvoltage protection is achieved by turning off the high side switch and turning on the low side N-channel MOSFET 100% of the time.

Enable

Low quiescent mode or "Sleep Mode" is initiated by pulling the COMP pin below 0.3V with an external open-drain or open-collector transistor. Supply current is reduced to 30µA (typical) in shutdown. On power-up, assuming that VCC has exceeded the UVLO start threshold (2.8V), an internal 5µA pull-up current at the COMP pin brings the SP6123 out of shutdown mode and ensures start-up. During normal operating conditions and in absence of a fault, an internal clamp prevents the COMP pin from swinging below 0.6V. This guarantees that during mild transient conditions, due either to line or load variations, the SP6123 does not enter shutdown unless it is externally activated.

During Sleep Mode, the high side and low side MOSFETS are turned off and the internal soft start voltage is held low.

UVLO

Assuming that there is not shutdown condition present, then the voltage on the V_{CC} pin determines operation of the SP6123. As V_{CC} rises, the UVLO block monitors V_{CC} and keeps the high side and low side MOSFETS off and the internal SS voltage low until V_{CC} reaches 2.8V. If no faults are present, the SP6123 will initiate a soft start when V_{CC} exceeds 2.8 V.

Hysteresis (about 100mV) in the UVLO comparator provides noise immunity at start-up.

Soft Start

Soft start is required on step-down controllers to prevent excess inrush current through the power train during start-up. Typically this is managed by sourcing a controlled current into a timing capacitor and then using the voltage across this capacitor to slowly ramp up either the error amp reference or the error amp output (COMP). The control loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady-state duty cycle as the output voltage increases to its regulated value. As a result of controlling the inductor volt*second product during startup, inrush current is also controlled.

In the SP6123 the duration of the soft-start is controlled by an internal timing circuit that provides a 0.27V/ms slew-rate, which is used during startup and overcurrent to set the hiccup time. The SP6123 implements soft-start by ramping up the error amplifier reference voltage providing a controlled slew-rate of the output voltage, thereby preventing overshoot and inrush current at power up.

The presence of the output capacitor creates extra current draw during startup. Simply stated, dV_{OUT}/dt requires an average sustained current in the output capacitor and this current must be considered while calculating peak inrush current and over current thresholds. An approximate expression to determine the excess inrush current due to the dV_{OUT}/dt of the output capacitor C_{OUT} is:

$$I_{inrush} = C_{OUT} \times S_{SS} \times \frac{V_{OUT}}{0.8V}$$

Where,

S_{SS} = Softstart slew rate, 0.6V/ms for SP6123A and 0.3V/ms for SP6123.

As the figure shows, the SS voltage controls a variety of signals. First, provided all the external fault conditions are removed, an internal 5µA pull-up at the COMP pin brings the SP6123 out of shutdown mode. The internal timing circuit is then activated and controls the ramp-up of the error amp reference voltage. The COMP pin is pulled to 0.7V by the internal

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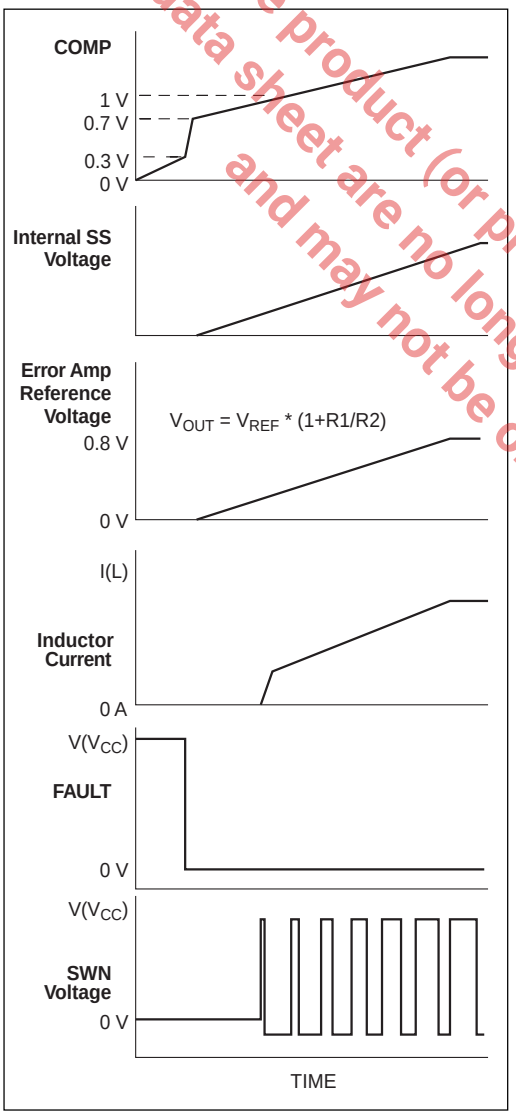
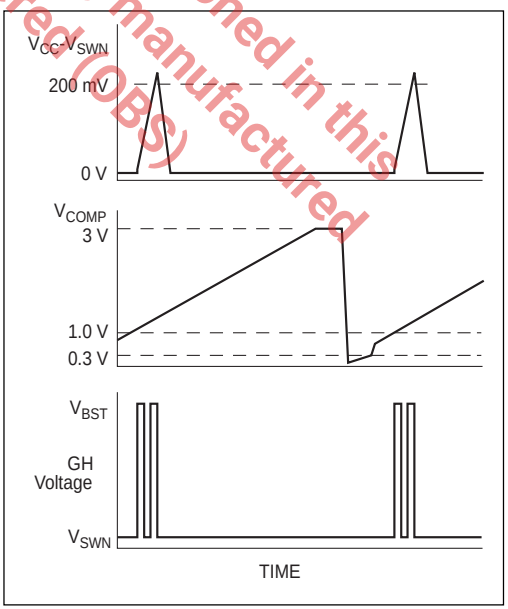
clamp and then gradually charges preventing the error amplifier from forcing the loop to maximum duty cycle. As the COMP voltage crosses about 1V (valley voltage of the PWM ramp), the driver begins to switch the high side MOSFET with narrow pulses in an effort to keep the converter output regulated . The SP6123 operates at low duty cycle as the COMP voltage increases above 1V. As the error amp reference ramps upward, the driver pulses widen until a steady state value is reached and the output voltage is regulated to the final value ending the soft start charge cycle.



Hiccup Mode

When the converter enters a fault mode, the SP6123 holds the high side and low side MOSFETs off for a finite period of time. Provided that the SP6123 is enabled, this time is set by the internal charge of the soft-start capacitor. In the event of an overcurrent condition, the current sense comparator sets the fault latch, which in turn discharge the internal SS capacitor, the COMP pin and holds the output drivers off. During this condition, the SP6123 stays off for the time it takes to discharge the COMP pin down to the 0.27V shutdown threshold. At this point, the fault latch is reset, but before the SP6123 is allowed to attempt restart, the COMP pin has to charge back to 1V before any output switching can be initiated. Then, the regulator attempts to restart normally by delivering short gate pulses and if the overcurrent condition is still present, the cycle will repeat itself. However, if upon restart, the overcurrent condition is still present, the SP6123 will detect the fault and remain in a fault state until COMP reaches about V_{CC}-1V thereby increasing the MOSFET off-time. This protection scheme minimizes thermal stress to the regulator components as the overcurrent condition persists.

The simplified waveforms that describe the hiccup mode operation are shown below.



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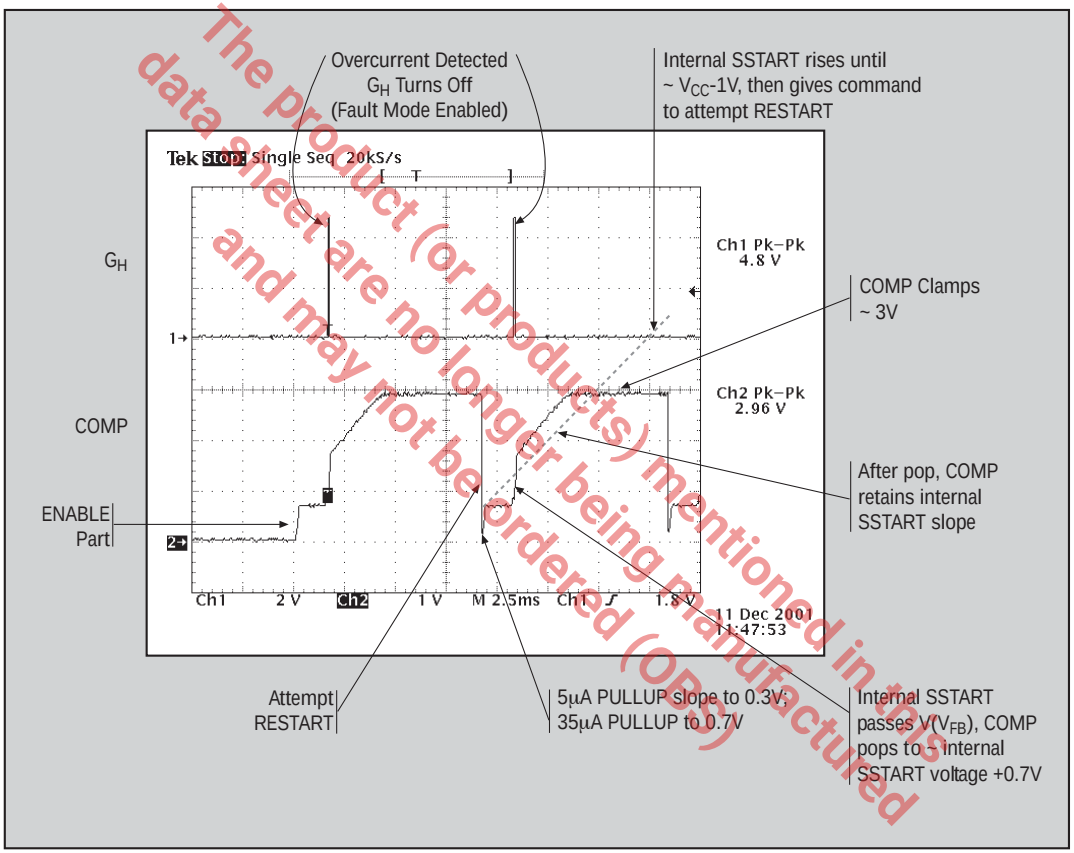
A more detailed description of the waveform is shown below.

SP6123 OVER CURRENT (HICCUP MODE)

Test Conditions

V_{FB} = 0.7V
V_{CC} = 5.0V
BST = 5.0V
SWN - tied to GND through 1k Resistor
COMP – released from GND



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Over Current Protection

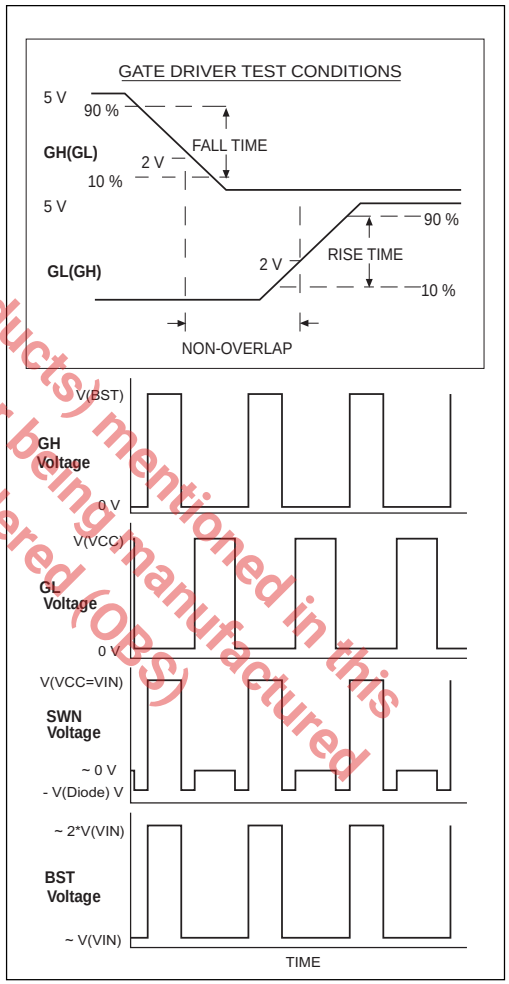
Over current protection on the SP6123 is implemented through detection of an excess voltage condition across the high side NMOS switch during conduction. This is typically referred to as high side $R_{DS(ON)}$ detection and eliminates the need of an external sense resistor. The over current comparator charges an internal sampling capacitor each time $V(V_{CC})$-V(SWN) exceeds the 200mV (typ) internal threshold and the GH voltage is high. The discharge/charge current ratio on the sampling capacitor is about 2%. Therefore, provided that the over current condition persists, the capacitor voltage will be pumped up during each time GH switches high. This voltage will trigger an over current condition upon reaching a CMOS inverter threshold. There are many advantages to this approach. First, the filtering action of the gated scheme protects against false and undesirable triggering that could occur during a minor transient overload condition or supply line noise. Furthermore, the total amount of time to trigger the fault depends on the on-time of the high side NMOS switch. Fifteen, 1µs pulses are equivalent to thirty, 500ns pulses or one, 15µs pulse, however, depending on the period, each scenario takes a different amount of total time to trigger a fault. Therefore the fault becomes an indicator of average power in the high side switch. The 200mV overcurrent threshold has a 3400 ppm/°C temperature coefficients in an effort to first order match the thermal characteristics of the $R_{DS(ON)}$ of the high side NMOS switch. It assumed that the SP6123 will be used in compact designs where there is a high amount of thermal coupling between the high side switch and the controller.

Output Drivers

The SP6123, unlike some other bipolar controller IC's, incorporates gate drivers with rail-to-rail swing that help prevent spurious turn on due to capacitive coupling. The driver stage consists of one high side NMOS, 4Ω driver, GH, and one low side, 4 Ω, NMOS driver, GL, optimized for driving external power MOSFET's in a synchronous buck topology. The output drivers also provide gate drive non-overlap mechanism that provides a dead time between GH and GL transitions to avoid potential shoot-through problems in the external MOSFETs.

The following figure shows typical waveforms for the output drivers.

As with all synchronous designs, care must be taken to ensure that the MOSFETs are properly chosen for non-overlap time, enhancement gate drive voltage, "on" resistance $R_{DS(ON)}$, reverse transfer capacitance Crss, input voltage and maximum output current.



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Inductor Selection

There are many factors to consider in selecting the inductor including cost, efficiency, size and EMI. In a typical SP6123 circuit, the inductor is chosen primarily for value, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and more output capacitance to smooth out the larger ripple current. The inductor must also be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}\,(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)}\,F_S\,K_r\,I_{OUT(\max)}}$$

where:

F_S = switching frequency

K_r = ratio of the peak to peak inductor ripple current to the maximum output current

The peak to peak inductor ripple current is:

$$I_{PP} = \frac{V_{OUT}\,(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)}\,F_S\,L}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements. The core material must be large enough not to saturate at the peak inductor current

$$I_{PEAK} = I_{OUT(\max)} + \frac{I_{PP}}{2}$$

and provide low core loss at the high switching frequency. Low cost powdered iron cores have a gradual saturation characteristic but can introduce considerable ac core loss, especially when the inductor value is relatively low and the ripple current is high. Ferrite materials, on the other hand, are more expensive and have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss and the design only needs to prevent saturation.

The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetic vendor.

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(Cu)} = I^2_{L(RMS)}\,R_{WINDING}$$

where $I_{L(RMS)}$ is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} = I_{OUT(max)}\sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT(max)}}\right)^2}$$

Output Capacitor Selection

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP6123 adjusts the inductor current to the new value. Therefore the capacitance must be large enough so that the output voltage is held up while the inductor current ramps up or down to

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the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the ESR value multiplied by the change in load current. Because of the fast transient response provided by the SP6123 when exposed to output load transient, the output capacitor is typically chosen for ESR , not for capacitance value.

The output capacitor's ESR, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PP}}$$

where:

ΔV_{OUT} = peak to peak output voltage ripple

I_{PP} = peak to peak inductor ripple current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP}\,(1-D)}{C_{OUT}F_S}\right)^2 + (I_{PP}R_{ESR})^2}$$

where:

D = duty cycle equal to V_{OUT}/V_{IN}

C_{OUT} = output capacitance value

Recommended capacitors that can be used effectively in SP6123 applications are: low-ESR aluminum electrolytic capacitors, OS-CON capacitors that provide a very high performance/ size ratio for electrolytic capacitors and low-ESR tantalum capacitors. AVX TPS series and Kemet T510 surface mount capacitors are popular tantalum capacitors that work well in SP6123 applications. POSCAP from Sanyo is a solid electrolytic chip capacitor that has low ESR and high capacitance. For the same ESR value, POSCAP has lower profile compared with tantalum capacitor.

Panasonic offers the SP series of specialty polymer aluminum electrolytic surface mount capacitors. These capacitors have a lower ESR than tantalum capacitors, reducing the total number of capacitance required for a given transient response.

Input Capacitor Selection

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. Most of this current is supplied by the input bypass capacitors. The RMS value of input capacitor current is determined at the maximum output current and under the assumption that the peak to peak inductor ripple current is low, it is given by:

$$I_{CIN(rms)} = I_{OUT(max)} \sqrt{D(1-D)}$$

The worse case occurs when the duty cycle, D, is 50% and gives an RMS current value equal to $I_{OUT}/2$. Select input capacitors with adequate ripple current rating to ensure reliable operation.

The power dissipated in the input capacitor is:

$$P_{CIN} = I^2_{CIN(rms)}\ R_{ESR(CIN)}$$

This can become a significant part of power losses in a converter and hurt the overall energy transfer efficiency.

The input voltage ripple primarily depends on the input capacitor ESR and capacitance. Ignoring the inductor ripple current, the input voltage ripple can be determined by:

$$\Delta V_{IN} = I_{out(\max)}\ R_{ESR(CIN)} + \frac{I_{OUT(MAX)} V_{OUT} (V_{IN} - V_{OUT})}{F_S C_{IN} V_{IN}^2}$$

The capacitor type suitable for the output capacitors can also be used for the input capacitors. However, exercise extra caution when tantalum capacitors are considered. Tantalum capacitors are known for catastrophic failure when exposed to surge current, and input capacitors are prone to such surge current when power supplies are connected 'live' to low impedance

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power sources. Certain tantalum capacitors, such as AVX TPS series, are surge tested. For generic tantalum capacitors, use 2:1 voltage derating to protect the input capacitors from surge fallout.

MOSFET Selection

The losses associated with MOSFETs can be divided into conduction and switching losses. Conduction losses are related to the on resistance of MOSFETs, and increase with the load current. Switching losses occur on each on/off transition when the MOSFETs experience both high current and voltage. Since the bottom MOSFET switches current from/to a paralleled diode (either its own body diode or an external Schottky diode), the voltage across the MOSFET is no more than 1V during switching transition. As a result, its switching losses are negligible. The switching losses are difficult to quantify due to all the variables affecting turn on/off time. However, making the assumption that the turn on and turn off transition times are equal, the transition time can be approximated by:

$$t_T = \frac{C_{ISS} V_{IN}}{I_G},$$

where C_{ISS} is the MOSFET's input capacitance, or the sum of the gate-to-source capacitance, C_{GS}, and the drain-to-gate capacitance, C_{GD}. This parameter can be directly obtained from the MOSFET's data sheet.

I_G is the gate drive current provided by the SP6123 (approximately 1A at V_{IN}=5V) and V_{IN} is the input supply voltage.

Therefore an approximate expression for the switching losses associated with the high side MOSFET can be given as:

$$P_{SH(max)} = (V_{IN(max)} + V_F) I_{OUT(max)} t_T F_S,$$

where t_T is the switching transition time and V_F is the free wheeling diode drop.

Switching losses need to be taken into account for high switching frequency, since they are directly proportional to switching frequency. The conduction losses associated with top and bottom MOSFETs are determined by

$$P_{CH(max)} = R_{DS(ON)} I_{OUT(max)}^2 D$$

$$P_{CL(max)} = R_{DS(ON)} I_{OUT(max)}^2 (1 - D),$$

where:

$P_{CH(max)}$ = conduction losses of the high side MOSFET

$P_{CL(max)}$ = conduction losses of the low side MOSFET

$R_{DS(ON)}$ = drain to source on resistance.

The total power losses of the top MOSFET are the sum of switching and conduction losses. For synchronous buck converters of efficiency over 90%, allow no more than 4% power losses for high or low side MOSFETs. For input voltages of 3.3V and 5V, conduction losses often dominate switching losses. Therefore, lowering the $R_{DS(ON)}$ of the MOSFETs always improves efficiency even though it gives rise to higher switching losses due to increased C_{ISS} .

Total gate charge is the charge required to turn the MOSFETs on and off under the specified operating conditions (V_{GS} and V_{DS}). The gate charge is provided by the SP6123 gate drive circuitry. (At 500kHz switching frequency, the gate charge is the dominant source of power dissipation in the SP6123). At low output levels, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high side and low side MOSFETs is:

$$I_{G(av)} = Q_{GH} F_S + Q_{GL} F_S, \text{ where}$$

Q_{GH} and Q_{GL} are the total charge for the high side and the low side MOSFETs respectively.

Considering that the gate charge current comes from the input supply voltage V_{IN}, the power dissipated in the SP6123 due to the gate drive is:

$$P_{GATE\ DRIVE} = V_{IN} I_{G(av)}$$

Top and bottom MOSFETs experience unequal conduction losses if their on time is unequal. For applications running at large or small duty cycle, it makes sense to use different top and bottom MOSFETs. Alternatively, parallel multiple MOSFETs to conduct large duty factor.

$R_{DS(ON)}$ varies greatly with the gate driver voltage. The MOSFET vendors often specify $R_{DS(ON)}$ on multiple gate to source voltages (V_{GS}), as well as provide typical curve of $R_{DS(ON)}$ versus

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V_{GS}. For 5V input, use the $R_{DS(ON)}$ specified at 4.5V V_{GS}. At the time of this publication, vendors, such as Fairchild, Siliconix and International Rectifier, have started to specify $R_{DS(ON)}$ at V_{GS} less than 3V. This data is necessary for designs where the MOSFETs are driven with 3.3V.

Thermal calculation must be conducted to ensure the MOSFET can handle the maximum load current. The junction temperature of the MOSFET, determined as follows, must stay below the maximum rating.

$$T_{J(\max)} = T_{A(\max)} + \frac{P_{MOSFET(\max)}}{R_{\theta JA}},$$

where

$T_{A(max)}$ = maximum ambient temperature

$P_{MOSFET(max)}$ = maximum power dissipation of the MOSFET

$R_{\theta JA}$ = junction to ambient thermal resistance.

$R_{\theta JA}$ of the device depends greatly on the board layout, as well as device package. Significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. For example, in a SO-8 package, placing two 0.04 square inches copper pad directly under the package, without occupying additional board space, can increase the maximum power dissipation from approximately 1 to 1.2W. For DPAK package, enlarging the tap mounting pad to 1 square inches reduces the $R_{\theta JA}$ from 96°C/W to 40°C/W.

Schottky Diode Selection

When paralleled with the bottom MOSFET, an optional Schottky diode can improve efficiency and reduce noise. Without this Schottky diode, the body diode of the bottom MOSFET conducts the current during the non-overlap time when both MOSFETs are turned off. Unfortunately, the body diode has high forward voltage and reverse recovery problem. The reverse recovery of the body diode causes additional switching noises when the diode turns off. The Schottky diode alleviates this noise and additionally improves efficiency thanks to its low forward voltage. The reverse voltage across the diode is equal to input voltage, and the diode must be able to handle the peak current equal to the maximum load current.

The power dissipation of the Schottky diode is determined by

$$P_{DIODE} = 2V_F I_{OUT} T_{NOL} F_S$$

where

T_{NOL} = non-overlap time between G_L and G_H.

V_F = forward voltage of the Schottky diode.

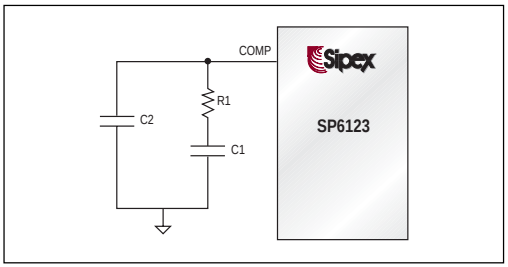

Figure 1. The RC network connected to the COMP pin provides a pole and a zero to control loop.

Loop Compensation Design

The goal of loop compensation is to manipulate loop frequency response such that its gain crosses over 0db at a slope of -20db/dec. The SP6123 has a transconductance error amplifier and requires the compensation network to be connected between the COMP pin and ground, as shown in Figure 1.

The first step of compensation design is to pick the loop crossover frequency. High crossover frequency is desirable for fast transient response, but often jeopardize the system stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by

$$f_{Z(ESR)} = \frac{1}{2\pi C_{OUT} R_{ESR}}$$

Crossover frequency of 20kHz is a sound first try if low ESR tantalum capacitors or POSCAPs are used at the output. The next step is to calculate the complex conjugate poles contributed by the LC output filter,

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$$f_{P(LC)} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter, and feedback resistor divider. In order to crossover at the selected frequency f_{co}, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. In the RC network shown in Figure 1, the product of R1 and the error amplifier transconductance determines this gain. Therefore, R1 can be determined from the following equation that takes into account the typical error amplifier transconductance, reference voltage and PWM ramp built into the SP6123.

$$R_1 = \frac{2083 V_{OUT} f_{CO} f_{Z(ESR)}}{V_{IN} f_{P(LC)}^2}$$

In Figure 1, R1 and C1 provides a zero f_{Z1} which needs to be placed at or below $f_{P(LC)}$. If f_{Z1} is made equal to $f_{P(LC)}$ for convenience, the value of C_1 can be calculated as

$$C_1 = \frac{1}{2\pi f_{P(LC)} R_1}$$

The optional C_2 generates a pole f_{P1} with R_1 to cut down high frequency noise for reliable operation. This pole should be placed one decade higher than the crossover frequency to avoid erosion of phase margin. Therefore, the value of the C_2 can be derived from

$$C_2 = \frac{1}{20\pi f_{CO} R_1}$$

Figure 2 illustrates the overall loop frequency response and frequency of each pole and zero. To fine-tune the compensation, it is necessary to physically measure the frequency response using a network analyzer.

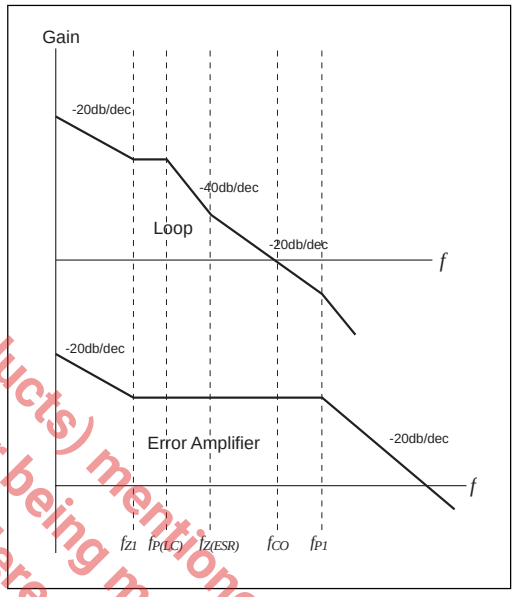

Figure 2. Frequency response of a stable system and its error amplifier.

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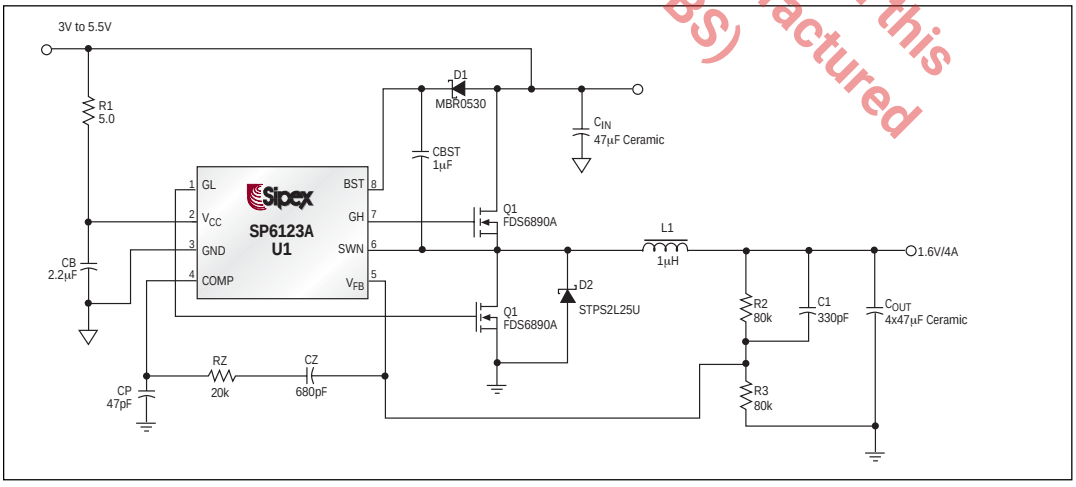

Figure 3. SP6123 Buck converter design with ceramic output capacitors.

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Most electrolytic and tantalum capacitors come with adequate ESR value to generate a zero below power supplies' crossover frequency. This is crucial to a stable close loop system. However, this same system can become unstable if ceramic output capacitors are used. The low ESR associated with ceramic capacitors can push the ESR zero above the crossover frequency and often higher than 1MHz. In this case, type III compensation is required to provide additional low frequency zero for adequate phase margin and thus stable operation.

The design of type III compensation using SP6123 transconductance error amplifier is quite straightforward. First, the resonant frequency of the LC output filter could be derived from

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_{OUT}}} = 11.6kHz$$

The values and references used in all the calculations agree with the schematic shown in Figure 3. Select values of R2, C1, R_Z and C_Z to place two zeros below or equal to the LC resonant frequency. Those two zeros are located at:

$$f_{Z1} = \frac{1}{2\pi R_2 C_1} = 6kHz$$

$$f_{Z2} = \frac{1}{2\pi R_Z C_Z} = 11.7kHz$$

There is low frequency pole determined by both the error amplifier gain and feedback gain. It occurs at

$$f_{P1} = \frac{1}{2\pi(R_2 // R_3) C_Z G_M R_{OUT}} = 3.25Hz$$

In SP6123, G_M (error amplifier transconductance) and R_{OUT} (error amplifier output impedance) are specified at 0.6ms and 3MΩ, respectively.

For frequencies above the second zero f_{Z2}, the feedback gain rises at 20dB/dec and is equal to

$$A_{FB} = 2\pi f R_Z C_1$$

However, the error amplifier gain A_{EA} declines at -20dB/dec due to C_P.

$$A_{EA} = \frac{G_M}{2\pi f C_P}$$

When A_{FB} is less than A_{EA}, the compensated error amplifier gain is dominated by A_{FB}. As a result, it shows up as a positive 20dB/dec slope. However, when the rising A_{FB} crosses the falling A_{EA} at one particular frequency, the compensated error amplifier gain is now solely determined by A_{EA}. Therefore, the 20dB/dec slope is converted to a -20dB/dec slope, and the bode plot demonstrates a double pole at this frequency which is equal to

$$f_{P2} = \frac{1}{2\pi}\sqrt{\frac{GM}{C_P C_1 R_Z}} = 221kHz$$

Select C_P such that f_{P2} is located at least a decade higher than the crossover frequency.

As shown in Figure 4, this type III compensation generates a close loop system with 50 degree phase margin and crossover frequency at 20kHz. This ensures a stable regulated power supply with tight DC regulation and fast transient response.

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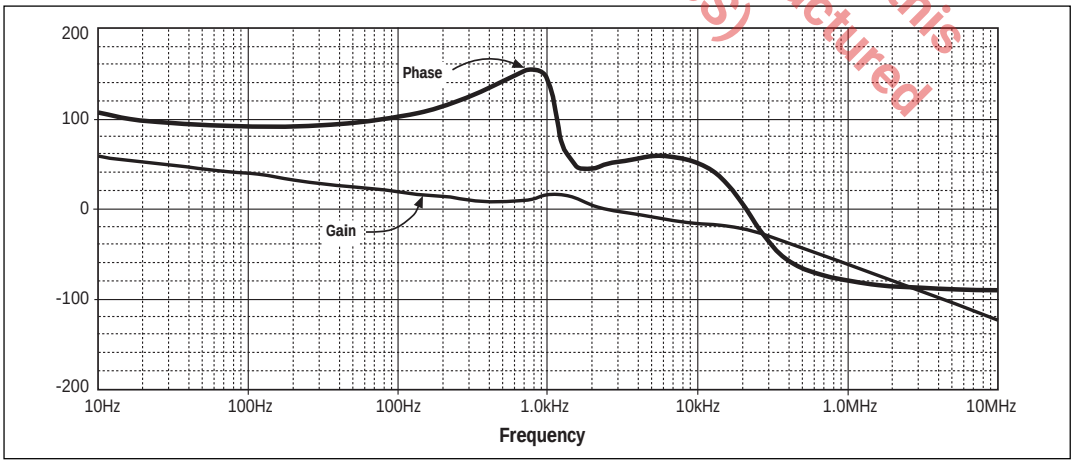

Figure 4. Bode Plot for schematic shown in Figure 3. V_{IN} = 3.3V and V_{OUT} = 1.6V, no load.

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Overcurrent Protection

Over current protection on the SP6123 is implemented through detection of an excess voltage condition across the high side switch during conduction. This is typically referred to as high side $R_{DS(ON)}$ detection. By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limit circuit eliminates the sense resistor that would otherwise be required and the corresponding loss associated with it. This improves the overall efficiency and reduces the number of components in the power path benefiting size and cost. $R_{DS(ON)}$ sensing is by default inaccurate and is primarily meant to protect the power supply during a fault condition. The overcurrent trip point will vary from unit to unit as the $R_{DS(ON)}$ of MOSFET varies. The SP6123 provides a built-in 200mV threshold between the V_{CC} and SWN pins.

The overcurrent threshold can be calculated as

$$I_{MAX} = \frac{200mV}{R_{DS(ON)}}$$

To ensure accurate current sensing, the V_{CC} pin should be connected directly to the drain of the high side MOSFET. A RC filter on the V_{CC} pin is not recommended because it would artificially alter the current signal and reduce the overcurrent threshold from the value given by the equation.

Output Voltage Program

As shown in Figure 5, the voltage divider connecting to the V_{FB} pin programs the output voltage according to

$$V_{OUT} = 0.8(1 + \frac{R_1}{R_2})$$

where 0.8V is the internal reference voltage.

Select R2 in the range of 10k to 100k, and R1 can be calculated using

$$R_1 = \frac{R_2(V_{OUT} - 0.8)}{0.8}$$

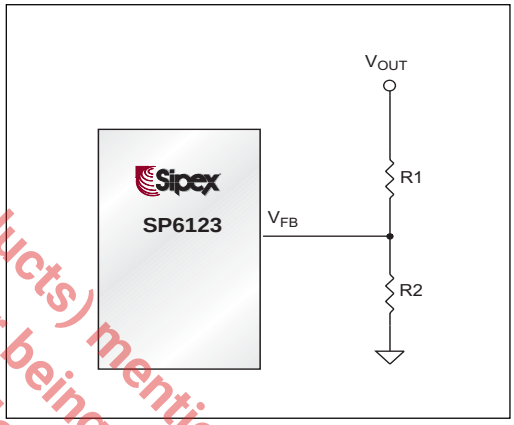

Figure 5. A voltage divider connected to the V_{FB} pin programs the output voltage.

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PCB layout plays a critical role in proper function of the converters and EMI control. In switch mode power supplies, loops carrying high di/dt give rise to EMI and ground bounces. The goal of layout optimization is to identify these loops and minimize them. It is also crucial on how to connect the controller ground such that its operation is not affected by noise. The following guideline should be followed to ensure proper operation.

1. A ground plane is recommended for minimizing noises, copper losses and maximizing heat dissipation.

2. Begin the layout by placing the power components first. Orient the power circuitry to achieve a clean power flow path. If possible make all the connections on one side of the PCB with wide, copper filled areas.

3. Connect the ground of feedback divider and compensation components directly to the GND pin of the IC using a dedicated ground trace. Then connect this pin as close as possible to the ground of the output capacitor.

4. The V_{CC} bypass capacitor should be right next to the V_{CC} and GND pins.

5. The trace connecting the feedback resistors to the output should be short, direct and far away from the switch node, and switching components.

6. Minimize the trace between G_H/G_L and the gates of the MOSFETs to reduce the impedance driving the MOSFETs. This is especially important for the bottom MOSFET that tends to turn on through its Miller capacitor when the switch node swings high.

7. Minimize the loop composed of input capacitors, top/bottom MOSFETs and Schottky diode. This loop carries high di/dt current. Also increase the trace width to reduce copper losses.

8. Maximize the trace width of the loop connecting the inductor, output capacitors, Schottky diode and bottom MOSFET.

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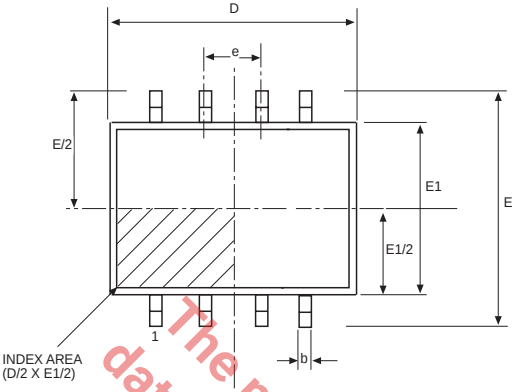
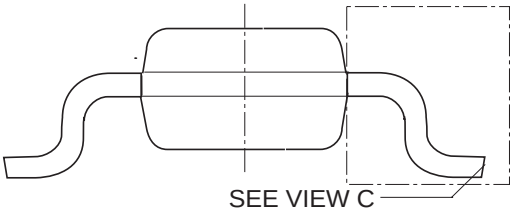
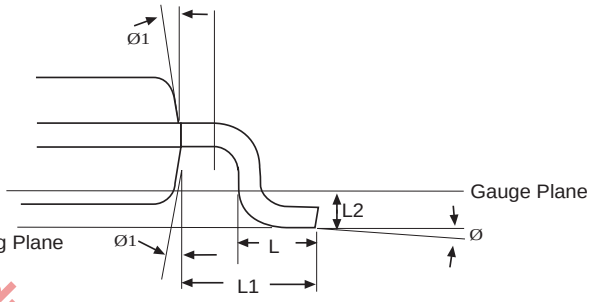
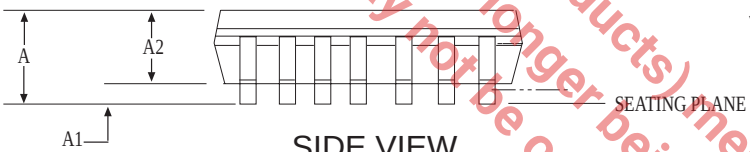


TOP VIEW





VIEW C



SIDE VIEW

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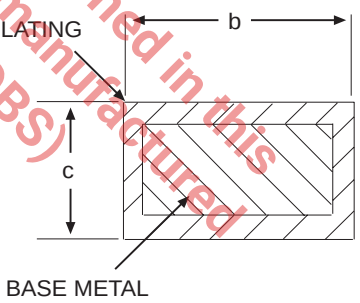
8 Pin NSOIC (JEDEC MS-012, AA - VARIATION)	DIMENSIONS Minimum/Maximum (mm)		
COMMON HEIGHT DIMENSION			
SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
Ø	0º	-	8º
Ø1	5º	-	15º



CONTACT AREA

PACKAGE: 8 PIN NSOIC

(Narrow refers to symbol E1)

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ORDERING INFORMATION

Part Number	Operating Temperature Range	Package Type
500kHz		
SP6123ACN	0˚C to +70˚C	8-Pin NSOIC
SP6123ACN/TR	0˚C to +70˚C	8-Pin NSOIC
300kHz		
SP6123CN	0˚C to +70˚C	8-Pin NSOIC
SP6123CN/TR	0˚C to +70˚C	8-Pin NSOIC

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP6123CN/TR = standard; SP6123CN-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 2500 for NSOIC.

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Sipex Corporation

ANALOG EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

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