

	Title: QFN/DFN Assembly Application Notes	Document No. AAN-10004 Rev: 000	Revision Date June 20, 2016
		Page 1 of 7	

Contents

1.0 Introduction

2.0 Package Characteristics

3.0 PCB design guidelines

- 3.1 Land pad styles
- 3.2 Land pattern terminals
- 3.3 Land pattern of Lead and Exposed design
- 3.4 Dimension guideline summary

4.0 Stencil design guidelines

- 4.1 Solder stencils
- 4.2 Lead finger stencil design
- 4.3 Exposed pad stencil design

5.0 Solder reflow

6.0 Appendix

- 6.1 MSL (Moisture Sensitivity Level) Classification

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	Title: QFN/DFN Assembly Application Notes	Document No. AAN-10004 Rev: 000	Revision Date June 20, 2016
	Page 2 of 7		

1.0 Introduction

Quad flatpack no-lead (QFN) package is near CSP plastic encapsulated package using conventional copper lead frame technology. This construction benefits from being a cost effective advanced packaging solution which helps to maximize board space with improved electrical and thermal performance.

Meanwhile, Consumer-electronics manufacturers are striving to reduce product size to meet world wide trend such as smaller, thinner, and thermally enhanced packages. A performance analysis has shown that QFN packages have better thermal performance than other packages. Other benefits are low inductance and capacitance, small package volume, smaller board routing area, no external leads, compared to conventional leaded packages.

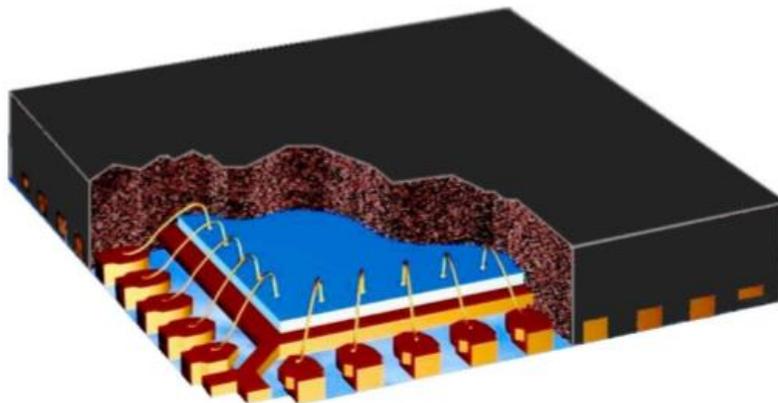


Figure 1. Cross section of a Generic QFN Package

2.0 Package Characteristics

Figure 2. shows cross section view of QFN PKG and the structure has been described as below.

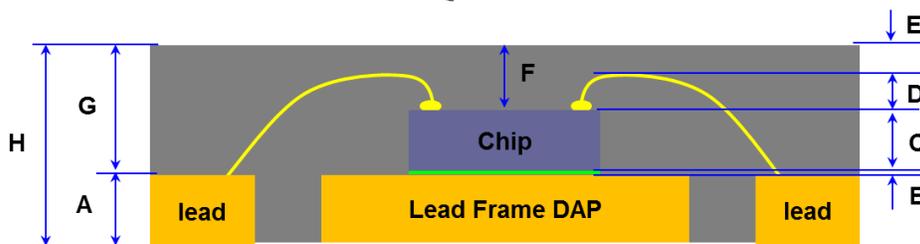


Figure 2. Typical cross sections

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A : Leadframe, B : Adhesive, C : Chip thickness, D : Loop height of wire,
E : Mold to wire gap, F : Mold clearance, G : Mold thickness, H : Total height

Figure 3 shows dimensions on package outline drawings and it should be changed per PKG size.

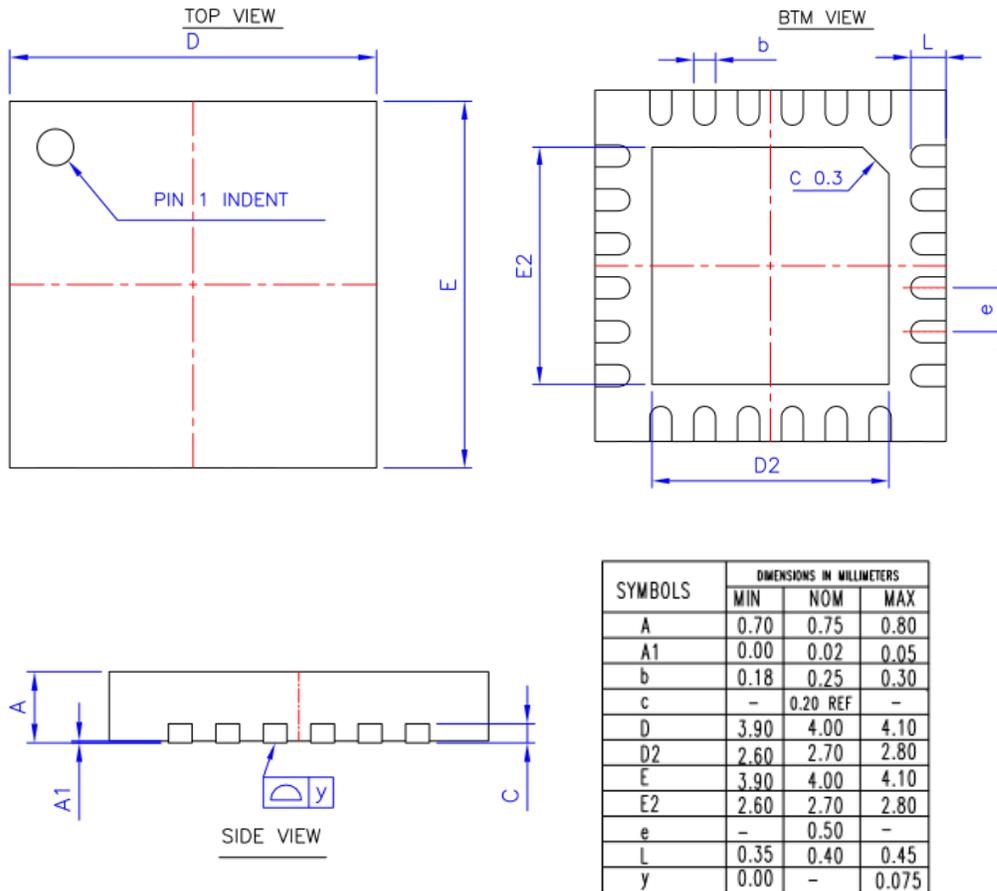


Figure 3. QFN Package dimension (e.g. 24QFN 4x4)

3.0 PCB design guidelines

3.1 Land pad styles

Non Solder Mask Defined (NSMD) type is recommended over Solder Mask Defined (SMD) type because of tighter tolerance on copper etching than solder masking. NSMD type can give a larger copper pad area and it leads to improved solder joint reliability.



3.2 Land pattern terminals

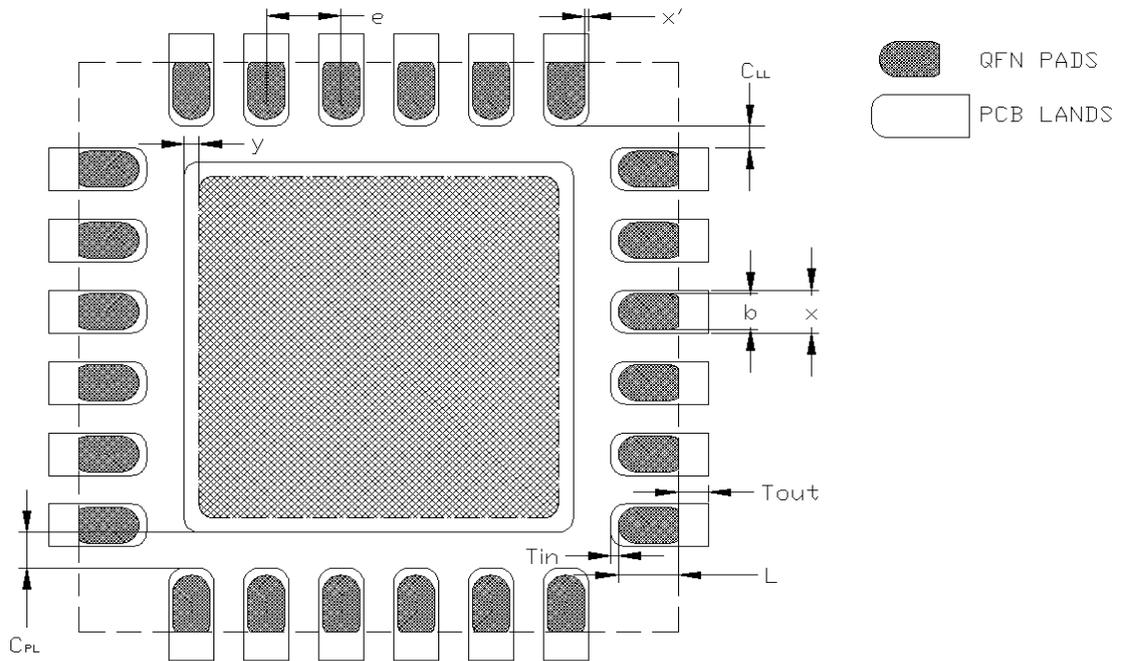


Figure 4. Typical QFN Land pattern Layout with Package overlay

Symbol	Description
e	QFN Lead Pitch
b	QFN Lead Width
x	Terminal Land Width
y	Minimum distance between QFN exposed die pad to PCB thermal land
Tout	Outward Extension
Tin	Inward Extension
x'	Sideward Extension
L	QFN Lead Length
C _{LL} *	Minimum distance between two perpendicular lands in any corner
C _{PL} *	Minimum distance between Central paddle to inside edge of thermal land

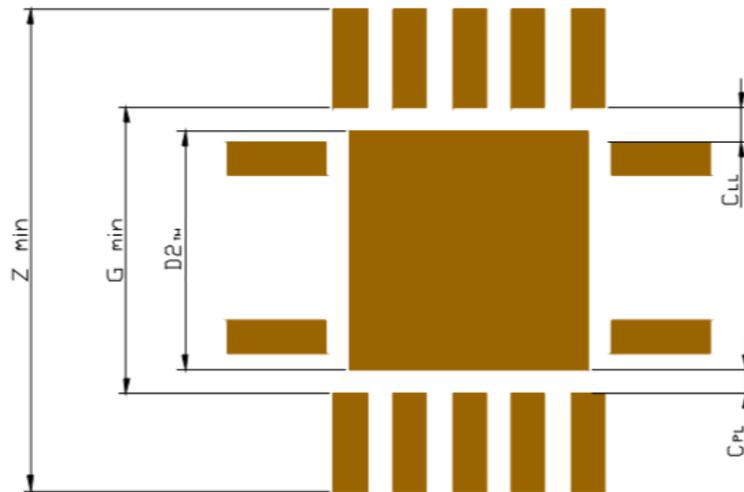
* Note: Clearance dimensions C_{LL} and C_{PL} defined to prevent solder bridging

3.3 Land pattern design of Lead & Exposed pad

The followings are design guideline for each land pattern.

- Tout : 0.2mm~0.5mm is recommended.
- Tin : 0.05mm is recommended.
- x' : More than 0.025mm for lead pitches equal to or greater than 0.65mm
Min 0.025mm for lead pitches less than 0.65mm
- Cpl : More than 0.2mm is recommended.
- y : 0~0.15mm is recommended but it should be decided by Cpl.

Based on above guideline, the followings should be considered when land pattern is drawn.



Symbol	Description
Z min	Terminal land pad – outside dimension
G min	Terminal land pad – inside dimension
D2th / E2th	Terminal land pad of exposed pad (D2 / E2)

$$D2th > D2 \text{ only if } D2th < Gmin - (2 \times Cpl)$$

$$E2th > E2 \text{ only if } E2th < Gmin - (2 \times Cpl)$$

$$D2th \text{ max} = Gmin - (2 \times Cpl)$$

$$E2th \text{ max} = Gmin - (2 \times Cpl)$$

$$Zmin = D + \text{the profile tolerance of PKG boxy} + (2 \times Tout)$$

$$Gmin = D - (2 \times Lmax) - (2 \times Tin)$$

3.4 Dimension guideline summary per lead pitch

Typical Nominal Package I/O Lead Dimensions (mm)			I/O Land “Design Dimension” Guidelines (mm)						
Lead Pitch (e)	Lead Width (b)	Lead Length (L)	Land Width (x)	y	Tout	Tin	x’	C _{LL}	C _{PL}
0.8	0.30	0.55	0.35	0~0.15	0.20	Min. 0.05	Min. 0.025	Min. 0.15	Min. 0.20
0.65	0.30	0.4~0.55	0.35						
0.5	0.25	0.4~0.55	0.30						
0.4	0.20	0.4	0.25						

4.0 Stencil design guidelines

4.1 Solder stencils

- Stencils are made of polymer or stainless steel or brass.
- Apertures walls should be trapezoidal to ensure uniform release of the solder paste and to reduce smearing.
- The solder-joint thickness for QFN terminal leads should be 50um to 75um
- As a general rule, stencil thickness is 100~150um and 125um is recommended for QFN packages.

4.2 Lead finger stencil design

- For stencil thickness of 100um, area ratio is 0.86, terminal-pad paste transfer efficiency is 89%, 100% for the thermal pad
- For stencil thickness of 125um, area ratio is >0.66, terminal-pad paste transfer efficiency is 73%, 100% for the thermal pad

4.3 Exposed pad stencil design

- The slotted thermal pad stencil design is recommended to prevent QFN package from floating during reflow and to allow adequate room for outgassing of paste during reflow.

5.0 Solder reflow

This guidelines follow Exar’s surface mount devices classified to the levels defined in J-STD-020 and pls refer to AAN-0000002 spec in Exar.

	Title: QFN/DFN Assembly Application Notes	Document No. AAN-10004 Rev: 000	Revision Date June 20, 2016
		Page 7 of 7	

6.0 Appendix

6.1 Exar's General MSL (Moisture Sensitivity Level) Classification (Please refer to actual product specification for exceptions.)	* < or = 3x3 : MSL1@260'C * 3x3 < PKG body < or = 5x5 : MSL2@260'C * > 5x5 : MSL3@260'C
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