# MxL86280C

Ethernet Switch

# 8-Port Ethernet Switch with Eight 2.5 Gigabit PHYs

MxL86280C

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## Data Sheet

Revision 1.6, 2025-09-26
Reference ID 620856

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**Revision History**

| | |
|---|---|
| **Current:** | **Revision 1.6, 2025-09-26** |
| **Previous:** | **Revision 1.5, 2025-04-10** |
| **Page** | **Major changes since previous revision** |
| 117 | **Section 5.2 PHY-specific Management Registers**:<br>• Removed **Internal Test Modes CDIAG and ABIST (Register 0.31)**. |
| 272 | **Table 58 Product and Package Naming**:<br>• Changed shipping format information and ordering part number. |
| **Page** | **Major changes in Revision 1.4** |
| 270 | **Table 56 JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network**:<br>• Updated table. |
| | |

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# Preface

This Data Sheet describes the features and system architecture of the Ethernet Switch MxL86280C, which is an 8-Port Ethernet Switch with Eight 2.5 Gigabit PHYs.

## Document Conventions

In the interest of brevity, this document uses short names to represent full product names.

**MxL86280C** Ethernet Switch MxL86280C

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## Document Information

This document's identifying information is:

**Document Reference (Citation) Name**

*MxL86280C Ethernet Switch Data Sheet Rev. 1.6*

**File Name**

`620856_MxL86280C_DS_Rev1.6.pdf`

**Organization of this Document**

- **Chapter 1, Product Overview**
  This chapter provides an overview of the MxL86280C.
- **Chapter 2, External Signals**
  This chapter provides a pinout of the MxL86280C device package.
- **Chapter 3, Functional Description**
  This chapter provides the functional description for the MxL86280C.
- **Chapter 4, MDIO and MMD Register Interface Description**
  This chapter describes the MDIO and MMD registers available to support the MxL86280C feature set.
- **Chapter 5, PHY MDIO Registers Detailed Description**
  This chapter describes the fields and reset values of the MDIO registers.
- **Chapter 6, PHY MMD Registers Detailed Description**
  This chapter describes the fields and reset values of the MMD registers.
- **Chapter 7, Electrical Characteristics**
  This chapter provides the electrical characteristics for the MxL86280C.
- **Chapter 8, Package Outline**
  This chapter provides a package outline for the MxL86280C.
- **Chapter 9, Product Ordering Information**
  This chapter provides the product ordering details for the MxL86280C.
- **Standards References**

# 1 Product Overview

The MxL86280C device is a highly integrated, low power, non-blocking multi-port Ethernet Switch. It offers a cost-optimized solution well-suited for switches. The MxL86280C has eight integrated Ethernet BASE-T PHYs which support four data rates: 2500, 1000, 100, and 10 Mbps.

On the Ethernet Twisted Pair Interface (TPI), the MxL86280C is compliant with the standards from IEEE 802.3 referenced in [2]:

- 2.5GBASE-T (IEEE 802.3 Clause 126, NBASE-T)
- 1000BASE-T (IEEE 802.3 Clause 40)
- 100BASE-TX (IEEE 802.3 Clause 25)
- 10BASE-Te (IEEE 802.3 Clause 14)

This interface supports the Energy-Efficient Ethernet (EEE) feature to reduce idle mode power consumption. Power saving at the system level is also possible with the wake-on-LAN feature. A low-EMI line driver with integrated termination facilitates the PCB design.

With reference to the Open System Interconnection (OSI) model, the MxL86280C implements eight layer 1 physical media access devices, a layer 2 switch, and an MDIO management interface.

Up to 1 MB embedded packet storage SRAM is integrated and 10 kB jumbo frames are supported. The MxL86280C integrates a 1K entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation. It also supports double VLAN tagging, insertion, removal, and translation. The MxL86280C features 16K VLAN-aware MAC addresses with 4-way hashing algorithm for address searching, auto-learning, and auto-aging.

A programmable packet parser and a powerful classification engine allow future-proof designs that enable various data traffic types. The MxL86280C supports IPv4 and IPv6 multicast forwarding, including IGMPv1/IGMPv2/IGMPv3 and MLDv1/MLDv2 snooping.

The MxL86280C features an advanced QoS architecture which prioritizes switch traffic for different classes of applications based on multiple fields of the packet. Multiple queues per port with strict or deficit weighted round robin scheduling and rate shaping are supported. It is possible to re-mark VLAN PCP and IP DSCP.

The MxL86280C supports a standard MDIO management interface as defined in IEEE 802.3 Clause 22 and Clause 45 [2]. The MDIO serial interface is operable with a clock running up to 25 MHz. It allows a management entity (the external chip implementing the MAC) to access standard MDIO/MMD registers to control the MxL86280C's behavior, or to read the link status. The MxL86280C is also configurable via pin strapping.

The MxL86280C is capable of driving up to 24 LEDs (three per BASE-T port). Each LED is independently programmable to indicate the link speed and traffic activities. Several indication schemes are selectable.

External supplies of 0.8 V, 1.2 V, 1.8 V, and 3.3 V are required to power the MxL86280C device.

The MxL86280C uses a ball grid array package (type BGA 18 x18 matrix, size 12 mm x 12 mm).

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## 1.1 Features

This section provides an overview of the features supported by the MxL86280C.

**Communication Interfaces**

- The eight Ethernet BASE-T interfaces support:
  - Ethernet modes and standards
    2.5GBASE-T (IEEE 802.3, NBASE-T), 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3), and 10BASE-Te (IEEE 802.3)
  - Ethernet twisted pair copper cable of category Cat5 or higher
  - Low EMI voltage mode line driver with integrated termination resistors
  - Transformerless Ethernet for backplane applications
  - Auto-Negotiation (ANEG) with extended next page support
  - Auto-MDIX and polarity correction
  - Auto-Downspeed (ADS)
  - 100BASE-TX EEE, 1000BASE-T EEE, 2.5GBASE-T EEE, and power down mode
  - Cable diagnostics: cable open/short detection and cable length estimation
  - Wake-on-LAN (WoL)
  - Jumbo frames of up to 10 kB
- The management interface supports the communication between the Station Manager (STA, per IEEE 802.3) and the MxL86280C using:
  - A Management Data Input/Output (MDIO) slave interface providing access to the standard registers in the MMD
  - An MDIO interface clock of up to 25 MHz
  - 3 MDIO message frame types as described in IEEE 802.3: Clause 22, Clause 22 Extended, and Clause 45 [2]
- The Quad SPI master interface connecting to serial external Quad-SPI flash memory supports:
  - Programmable interface clock: maximum 101 MHz
  - Internal firmware code access from external Quad-SPI flash memory
  - Write access to the Quad-SPI flash memory
  - Different Quad-SPI flash memory sizes up to 512 MB
  - Secure firmware upgrade of the flash memory
- The JTAG interface supports:
  - Boundary scan
  - Test and debug interface
  - Shared pins with GPIO functions
- The LED interface supports:
  - Programmable LED
  - Up to three LEDs per BASE-T port
  - Single and dual color LEDs
  - Connection of LED to ground or 3.3 V
  - Several LED indication schemes (link/activity, duplex/collision, and link speed)
  - Configuration of LED indication via MDIO registers
  - Control of LED brightness via software driver API
  - Alternative configuration of LED pins as GPIO for custom indication
- Supports two external interrupts:
  - Configurable as output to an external controller
  - Configurable as input from external device(s)
  - Configurable edge, level, and polarity

**Clocking and Timing Features**

- The input reference clock options are:

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  - 25 MHz crystal operation
  - 25 MHz direct from an external oscillator
  - An external CML/LVPECL reference clock operating at 50 MHz
- The output reference clock options are two pairs of differential clocks at 50 MHz, and the same frequency as the input reference clock.

### Ethernet MACs

- Eight Ethernet MACs for each BASE-T port, complying with IEEE 802.3:
  - Quad rate, that is, 10 Mbps, 100 Mbps, 1000 Mbps, or 2.5 Gbps operation speed for internal PHY
  - Half-duplex operation mode for 10 Mbps and 100 Mbps
  - Full-duplex operation mode for all speeds
- Enhanced frame size support (Jumbo frames, programmable limit up to 10 Kbyte)
- 802.3X flow control (pause frame) and 802.1Qbb flow control (PFC pause frame) in full-duplex mode. Backpressure (forced collisions) in half-duplex mode.
- Frame padding on egress traffic
- Minimum and maximum frame length check
- Frame Check Sequence (FCS) verification and stripping
- FCS generation and insertion/replacement
- Low Power Idle (LPI) mode as defined by IEEE 802.3 EEE

### Packet Processing

- L2 bridging
  - 16K entry VLAN-aware MAC address table
  - Shared and independent VLAN learning
  - Layer 2 security: IEEE 802.1X port authentication, MAC address filtering, port locking and spoofing detection, MAC address limiting, and broadcast storm control
  - Multiple spanning tree protocol
  - MAC in MAC tunneling (802.1ah), 256 tunnels
- L3 multicast forwarding at virtual-interface level
  - 1K entry VLAN aware IP multicast group table
  - Any Source Multicast (ASM) and Source Specific Multicast (SSM)
  - IPv4 IGMPv1/IGMPv2/IGMPv3 and IPv6 MLDv1/MLDv2 with software/firmware involvement
- VLAN classification
  - 802.1Q, 802.1Q QinQ, 802.1Qbg
  - 1K entry VLAN filtering
  - 1K entry extended VLAN tagging operation with sophisticated single tag and double tag VLAN mapping and translation
  - Private VLAN
- Traffic flow classification (ACL)
  - Programmable packet parsing
  - 512 entry traffic flow classification table
  - 32 concurrent keys with 1k bits in each entry
    Support bit mask and range for some of the keys. Keys include the source port information, packet length, and multiple L2/L3/L4/L4+ packet fields.
  - Multiple concurrent policy actions in each entry
    Destination port(s) assignment (including discard option), port filtering, traffic class assignment, traffic meter assignment, extended VLAN tagging operation assignment, MAC in MAC tunnel assignment, flow counter assignment, OAM handling assignment, cross VLAN policy, cross state policy, color assignment, Link Aggregation Group (LAG) assignment, L2 MAC address learning policy, and interrupt policy
- Advanced QoS
  - Up to 1 MB packet buffer

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  - Total 128 priority queues, up to eight priority queues per port
  - Flexible traffic class assignment
  - Flexible priority marking and re-marking
  - Flexible color marking and re-marking
  - Traffic metering on ingress and/or egress traffic
    srTCM and trTCM,128 meters
  - Per port and per queue shaping
  - Strict priority and DWRR scheduling
- Operation, Maintenance, and Management
  - Packets and bytes counters per MAC, per port, per virtual interface, and per traffic flow
  - Packet mirroring (ingress and egress mirroring to a designated port)
  - Loop detection support with software/firmware involvement
  - Loop-back support
  - IEEE 802.1ag and ITU-T Y.1731 Ethernet OAM delay and loss measurement hardware support
  - LAG support
    32 groups, up to 64 ports or virtual interfaces in a LAG

**Other Features**

- Temperature Sensor (warning, interrupt, reset, and auto-downspeed)

**Power Supply**

- 3.3 V, 1.8 V, 1.2 V, and 0.8 V external power sources

## 1.2 Applications

This section lists the supported modes of operation.

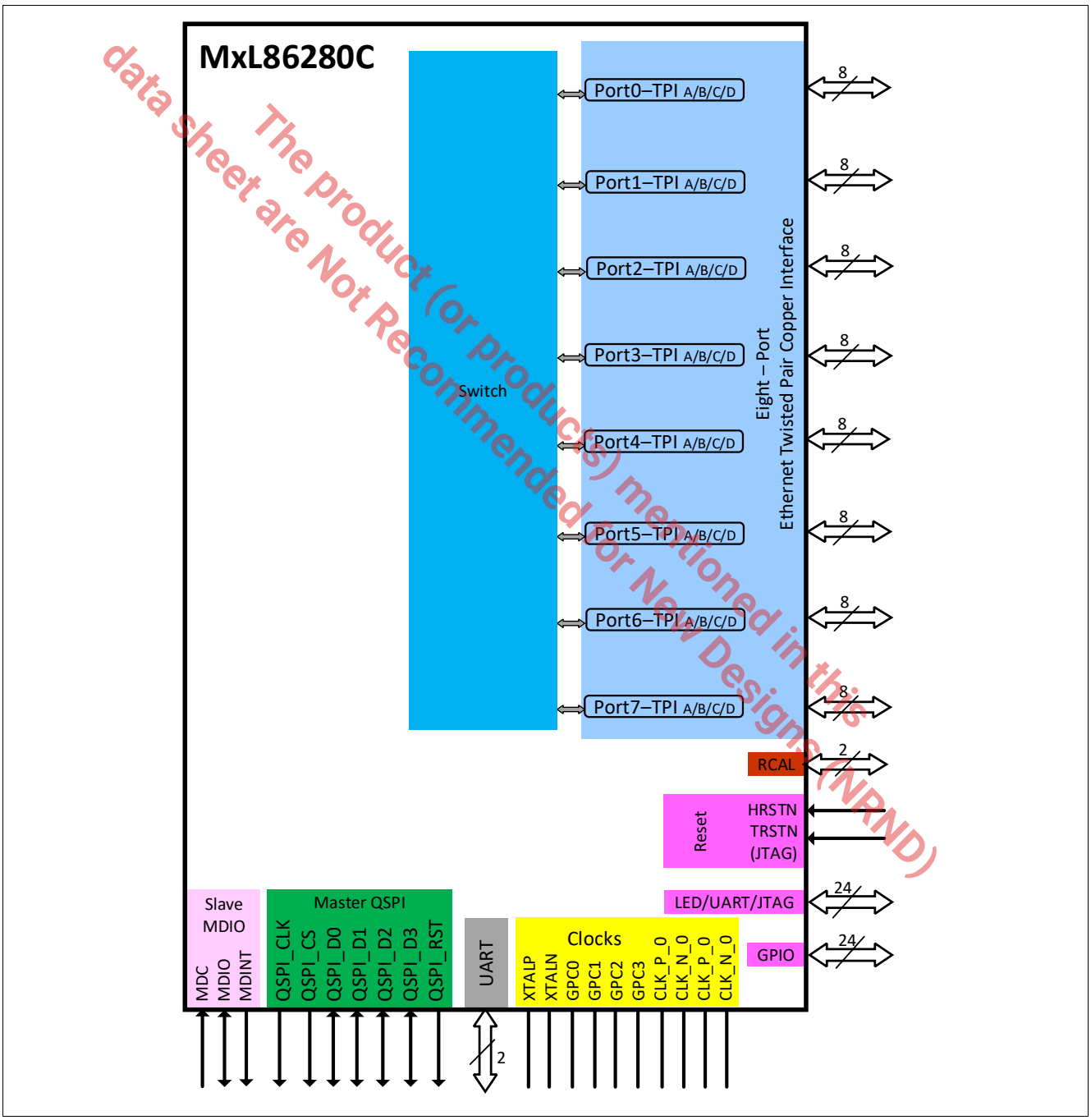
- Unmanaged mode, whereby no reconfiguration during runtime is necessary. MxL86280C-based devices work out of the box with their basic or default feature set. The Flash Configuration Area (FCA) must be used to change the default configuration. The FCA is an area in the flash memory which can be used to realize a limited static functionality set that differs from the default configuration. The FCA is described in [1].
- MDIO-managed mode, whereby the configuration of a lot of features is offered by means of an API via the slave MDIO interface. Contact MaxLinear for access to the API documentation. Pre-configuration of the features in the FCA is also supported.

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## 1.3 Block Diagram

**Figure 1** shows the block diagram of the MxL86280C. The main interfaces are:

- Slave control interface driven by a SoC processor, using MDIO slave
- Interrupt signal MDINT allowing the MxL86280C to notify the external processor about a change of status
- LED control
- Twisted pair interfaces (TPI)
- Master Quad Serial Peripheral Interface (QSPI) interface




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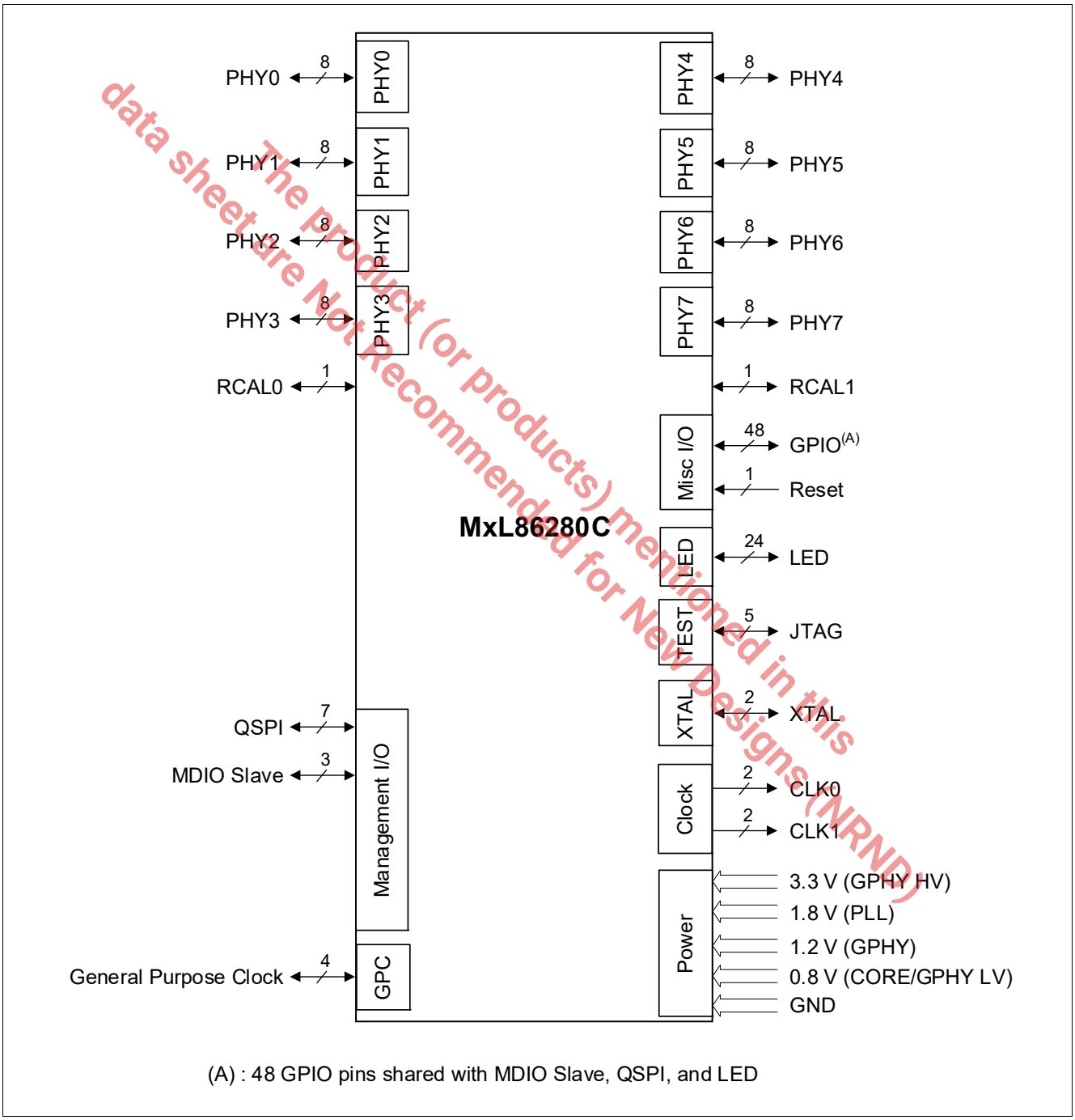
**Figure 1 MxL86280C Block Diagram**

# 2 External Signals

This chapter describes the signal mapping to the package.

## 2.1 Logic Symbol

**Figure 2** gives an overview of the device's external interfaces.




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**Figure 2 MxL86280C External Signal Overview**

## 2.2 External Signal Description

This section provides the ball diagram, abbreviations for pin types and buffer types, and the table of input and output signals.

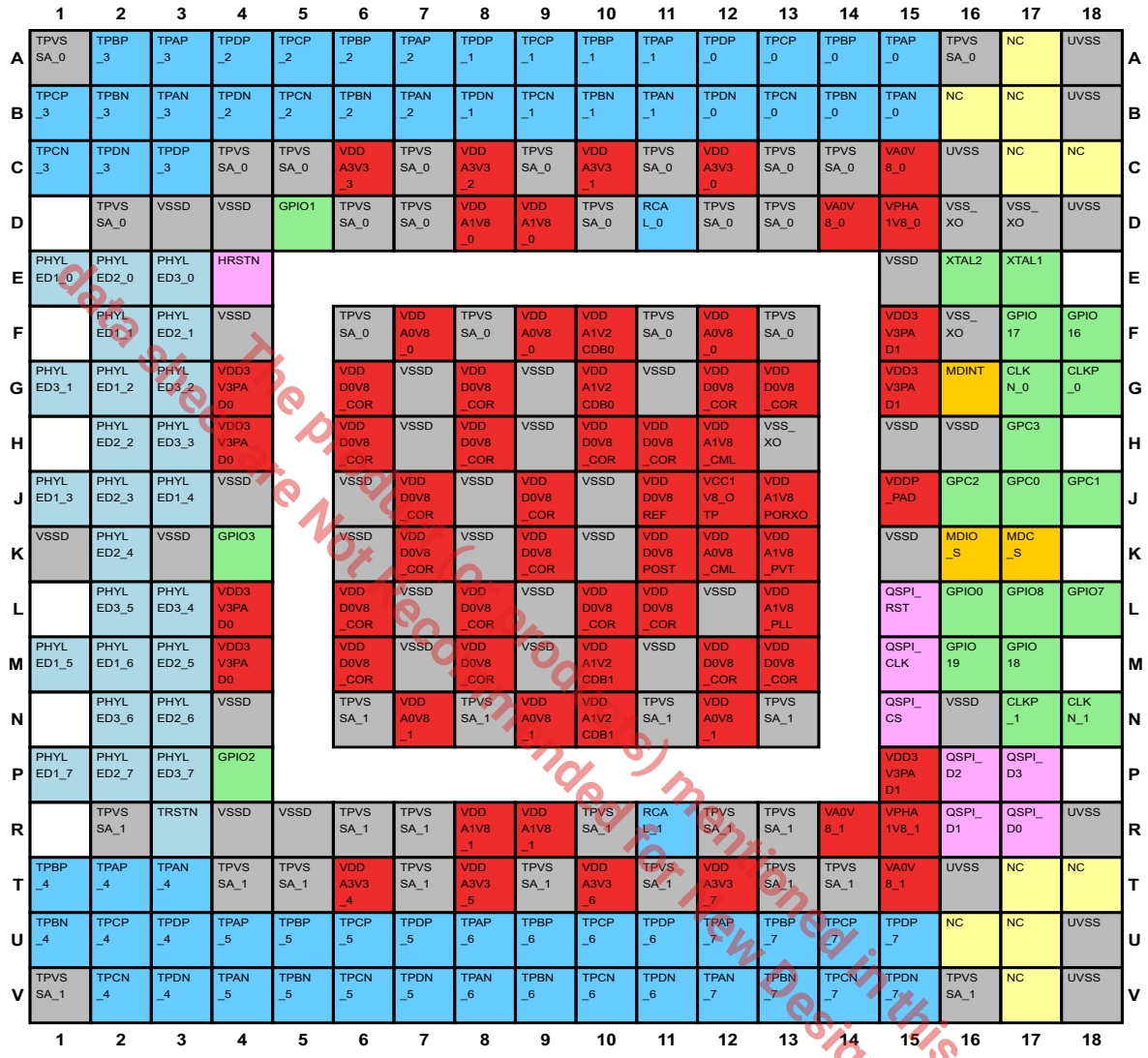
### 2.2.1 Ball Diagram

**Figure 3** shows the ball diagram. **Table 1** lists the ball diagram color codes.

**Table 1 Ball Diagram Color Codes**

| Color | Description |
|---|---|
| White | Unpopulated Balls |
| Red | Power |
| Orange | MDIO Signals |
| Grey | Ground |
| Blue | TPI-related Signals |
| Pink | QSPI, Reset Signals |
| Light Green | Clock, GPIO Signals |
| Light Blue | LED, JTAG Signals |
| Yellow | NC |

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| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | TPVSSA_0 | TPBP_3 | TPAP_3 | TPDP_2 | TPCP_2 | TPBP_2 | TPAP_2 | TPDP_1 | TPCP_1 | TPBP_1 | TPAP_1 | TPDP_0 | TPCP_0 | TPBP_0 | TPAP_0 | TPVSSA_0 | NC | UVSS | A |
| B | TPCP_3 | TPBN_3 | TPAN_3 | TPDN_2 | TPCN_2 | TPBN_2 | TPAN_2 | TPDN_1 | TPCN_1 | TPBN_1 | TPAN_1 | TPDN_0 | TPCN_0 | TPBN_0 | TPAN_0 | NC | NC | UVSS | B |
| C | TPCN_3 | TPDN_3 | TPDP_3 | TPVSSA_0 | TPVSSA_0 | VDDA3V3_3 | TPVSSA_0 | VDDA3V3_2 | TPVSSA_0 | VDDA3V3_1 | TPVSSA_0 | VDDA3V3_0 | TPVSSA_0 | TPVSSA_0 | VA0V8_0 | UVSS | NC | NC | C |
| D | | TPVSSA_0 | VSSD | VSSD | GPIO1 | TPVSSA_0 | TPVSSA_0 | VDDA1V8_0 | VDDA1V8_0 | TPVSSA_0 | RCAL_0 | TPVSSA_0 | TPVSSA_0 | VA0V8_0 | VPHA1V8_0 | VSS_XO | VSS_XO | UVSS | D |
| E | PHYLED1_0 | PHYLED2_0 | PHYLED3_0 | HRSTN | | | | | | | | | | | VSSD | XTAL2 | XTAL1 | | E |
| F | | PHYLED1_1 | PHYLED2_1 | VSSD | | TPVSSA_0 | VDDA0V8_0 | TPVSSA_0 | VDDA0V8_0 | VDDA1V2CDB0 | TPVSSA_0 | VDDA0V8_0 | TPVSSA_0 | | VDD3V3PAD1 | VSS_XO | GPIO17 | GPIO16 | F |
| G | PHYLED3_1 | PHYLED1_2 | PHYLED3_2 | VDD3V3PAD0 | | VDDD0V8_COR | VSSD | VDDD0V8_COR | VSSD | VDDA1V2CDB0 | VSSD | VDDD0V8_COR | VDDD0V8_COR | | VDD3V3PAD1 | MDINT | CLKN_0 | CLKP_0 | G |
| H | | PHYLED2_2 | PHYLED3_3 | VDD3V3PAD0 | | VDDD0V8_COR | VSSD | VDDD0V8_COR | VSSD | VDDD0V8_COR | VDDD0V8_COR | VDDA1V8_CML | VSS_XO | | VSSD | VSSD | GPC3 | | H |
| J | PHYLED1_3 | PHYLED2_3 | PHYLED1_4 | VSSD | | VSSD | VDDD0V8_COR | VSSD | VDDD0V8_COR | VSSD | VDDD0V8REF | VCC1V8_OTP | VDDA1V8PORXO | | VDDP_PAD | GPC2 | GPC0 | GPC1 | J |
| K | VSSD | PHYLED2_4 | VSSD | GPIO3 | | VSSD | VDDD0V8_COR | VSSD | VDDD0V8_COR | VSSD | VDDD0V8POST | VDDA0V8_CML | VDDA1V8_PVT | | VSSD | MDIO_S | MDC_S | | K |
| L | | PHYLED3_5 | PHYLED3_4 | VDD3V3PAD0 | | VDDD0V8_COR | VSSD | VDDD0V8_COR | VSSD | VDDD0V8_COR | VDDD0V8_COR | VSSD | VDDA1V8_PLL | | QSPI_RST | GPIO0 | GPIO8 | GPIO7 | L |
| M | PHYLED1_5 | PHYLED1_6 | PHYLED2_5 | VDD3V3PAD0 | | VDDD0V8_COR | VSSD | VDDD0V8_COR | VSSD | VDDA1V2CDB1 | VSSD | VDDD0V8_COR | VDDD0V8_COR | | QSPI_CLK | GPIO19 | GPIO18 | | M |
| N | | PHYLED3_6 | PHYLED2_6 | VSSD | | TPVSSA_1 | VDDA0V8_1 | TPVSSA_1 | VDDA0V8_1 | VDDA1V2CDB1 | TPVSSA_1 | VDDA0V8_1 | TPVSSA_1 | | QSPI_CS | VSSD | CLKP_1 | CLKN_1 | N |
| P | PHYLED1_7 | PHYLED2_7 | PHYLED3_7 | GPIO2 | | | | | | | | | | | VDD3V3PAD1 | QSPI_D2 | QSPI_D3 | | P |
| R | | TPVSSA_1 | TRSTN | VSSD | VSSD | TPVSSA_1 | TPVSSA_1 | VDDA1V8_1 | VDDA1V8_1 | TPVSSA_1 | RCAL_1 | TPVSSA_1 | TPVSSA_1 | VA0V8_1 | VPHA1V8_1 | QSPI_D1 | QSPI_D0 | UVSS | R |
| T | TPBP_4 | TPAP_4 | TPAN_4 | TPVSSA_1 | TPVSSA_1 | VDDA3V3_4 | TPVSSA_1 | VDDA3V3_5 | TPVSSA_1 | VDDA3V3_6 | TPVSSA_1 | VDDA3V3_7 | TPVSSA_1 | TPVSSA_1 | VA0V8_1 | UVSS | NC | NC | T |
| U | TPBN_4 | TPCP_4 | TPDP_4 | TPAP_5 | TPBP_5 | TPCP_5 | TPDP_5 | TPAP_6 | TPBP_6 | TPCP_6 | TPDP_6 | TPAP_7 | TPBP_7 | TPCP_7 | TPDP_7 | NC | NC | UVSS | U |
| V | TPVSSA_1 | TPCN_4 | TPDN_4 | TPAN_5 | TPBN_5 | TPCN_5 | TPDN_5 | TPAN_6 | TPBN_6 | TPCN_6 | TPDN_6 | TPAN_7 | TPBN_7 | TPCN_7 | TPDN_7 | TPVSSA_1 | NC | UVSS | V |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |

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**Figure 3 Ball Diagram for PG-FCLBGA-277 (Top View)**

### 2.2.2 Abbreviations

Table 2 and Table 3 summarize the abbreviations used in the signal tables.

**Table 2 Abbreviations for Pin Type**

| Abbreviations | Description |
|---|---|
| I | Input-only, digital levels |
| O | Output-only, digital levels |
| I/O | Bidirectional input/output signal, digital levels |
| Prg | Bidirectional pin, programmable to operate either as input or output, digital levels |
| AI | Input-only, analog levels |
| AO | Output-only, analog levels |
| AI/AO | Bidirectional, analog levels |
| PWR | Power |
| GND | Ground |

**Table 3 Abbreviations for Buffer Type**

| Abbreviations | Description |
|---|---|
| A | Analog characteristics, see the AC/DC specification for more information. |
| Prg | Programmable (open-drain/push-pull, pull-up/pull-down characteristic are programmable) |
| PU | Pull up (internal, weak) |

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### 2.2.3 Input/Output Signals

Table 4 to Table 13 provide a detailed description of all the pins.

#### 2.2.3.1 Ethernet Twisted Pair Interface

Unused TPI signals must be unconnected.

**Table 4 Ethernet Twisted Pair Interface Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Ethernet Port Twisted Pair Interface** | | | | |
| A15 | **TPAP_0** | AI/AO | A | **Port 0 Transmit/Receive Positive/Negative** |
| B15 | **TPAN_0** | AI/AO | A | |
| A14 | **TPBP_0** | AI/AO | A | |
| B14 | **TPBN_0** | AI/AO | A | |
| A13 | **TPCP_0** | AI/AO | A | |
| B13 | **TPCN_0** | AI/AO | A | |
| A12 | **TPDP_0** | AI/AO | A | |
| B12 | **TPDN_0** | AI/AO | A | |
| A11 | **TPAP_1** | AI/AO | A | **Port 1 Transmit/Receive Positive/Negative** |
| B11 | **TPAN_1** | AI/AO | A | |
| A10 | **TPBP_1** | AI/AO | A | |
| B10 | **TPBN_1** | AI/AO | A | |
| A9 | **TPCP_1** | AI/AO | A | |
| B9 | **TPCN_1** | AI/AO | A | |
| A8 | **TPDP_1** | AI/AO | A | |
| B8 | **TPDN_1** | AI/AO | A | |
| A7 | **TPAP_2** | AI/AO | A | **Port 2 Transmit/Receive Positive/Negative** |
| B7 | **TPAN_2** | AI/AO | A | |
| A6 | **TPBP_2** | AI/AO | A | |
| B6 | **TPBN_2** | AI/AO | A | |
| A5 | **TPCP_2** | AI/AO | A | |
| B5 | **TPCN_2** | AI/AO | A | |
| A4 | **TPDP_2** | AI/AO | A | |
| B4 | **TPDN_2** | AI/AO | A | |
| A3 | **TPAP_3** | AI/AO | A | **Port 3 Transmit/Receive Positive/Negative** |
| B3 | **TPAN_3** | AI/AO | A | |
| A2 | **TPBP_3** | AI/AO | A | |
| B2 | **TPBN_3** | AI/AO | A | |
| B1 | **TPCP_3** | AI/AO | A | |
| C1 | **TPCN_3** | AI/AO | A | |
| C3 | **TPDP_3** | AI/AO | A | |

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**Table 4 Ethernet Twisted Pair Interface Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| C2 | **TPDN_3** | AI/AO | A | |
| T2 | **TPAP_4** | AI/AO | A | **Port 4 Transmit/Receive Positive/Negative** |
| T3 | **TPAN_4** | AI/AO | A | |
| T1 | **TPBP_4** | AI/AO | A | |
| U1 | **TPBN_4** | AI/AO | A | |
| U2 | **TPCP_4** | AI/AO | A | |
| V2 | **TPCN_4** | AI/AO | A | |
| U3 | **TPDP_4** | AI/AO | A | |
| V3 | **TPDN_4** | AI/AO | A | |
| U4 | **TPAP_5** | AI/AO | A | **Port 5 Transmit/Receive Positive/Negative** |
| V4 | **TPAN_5** | AI/AO | A | |
| U5 | **TPBP_5** | AI/AO | A | |
| V5 | **TPBN_5** | AI/AO | A | |
| U6 | **TPCP_5** | AI/AO | A | |
| V6 | **TPCN_5** | AI/AO | A | |
| U7 | **TPDP_5** | AI/AO | A | |
| V7 | **TPDN_5** | AI/AO | A | |
| U8 | **TPAP_6** | AI/AO | A | **Port 6 Transmit/Receive Positive/Negative** |
| V8 | **TPAN_6** | AI/AO | A | |
| U9 | **TPBP_6** | AI/AO | A | |
| V9 | **TPBN_6** | AI/AO | A | |
| U10 | **TPCP_6** | AI/AO | A | |
| V10 | **TPCN_6** | AI/AO | A | |
| U11 | **TPDP_6** | AI/AO | A | |
| V11 | **TPDN_6** | AI/AO | A | |
| U12 | **TPAP_7** | AI/AO | A | **Port 7 Transmit/Receive Positive/Negative** |
| V12 | **TPAN_7** | AI/AO | A | |
| U13 | **TPBP_7** | AI/AO | A | |
| V13 | **TPBN_7** | AI/AO | A | |
| U14 | **TPCP_7** | AI/AO | A | |
| V14 | **TPCN_7** | AI/AO | A | |
| U15 | **TPDP_7** | AI/AO | A | |
| V15 | **TPDN_7** | AI/AO | A | |
| **Ethernet Port Test Point** | | | | |
| D11 | **RCAL_0** | AI/AO | A | **Test Point for GPHY Ethernet Ports 0 to 3**<br>Test point, do not connect. |
| R11 | **RCAL_1** | AI/AO | A | **Test Point for GPHY Ethernet Ports 4 to 7**<br>Test point, do not connect. |

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### 2.2.3.2 MDIO Interface

**Table 5 MDIO Management Interface Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **MDIO Slave Interface** | | | | |
| G16 | **MDINT** | O | Prg | **MDIO Interrupt from Any GPHY**<br>The interrupt interrupts an external block such as a higher-level management entity or a device controller of an SoC, on detection of certain events and states inside the GPHY device.<br>Voltage Domain: 1.8 V / 3.3 V |
| | GPIO4 | Prg | | **General Purpose IO 4**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 1.8 V / 3.3 V |
| K17 | **MDC_S** | I | Prg | **MDIO Slave Clock**<br>The external controller provides the serial clock of up to 25 MHz on this input.<br>Voltage Domain: 1.8 V / 3.3 V |
| | GPIO5 | Prg | | **General Purpose IO 5**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 1.8 V / 3.3 V |
| K16 | **MDIO_S** | I/O | Prg | **MDIO Slave Data Input/Output**<br>The external controller uses this signal to address internal registers and to transfer data to and from the internal registers.<br>Voltage Domain: 1.8 V / 3.3 V |
| | GPIO6 | Prg | | **General Purpose IO 6**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 1.8 V / 3.3 V |

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### 2.2.3.3 QSPI Interface

**Table 6 QSPI Management Interface Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| R17 | **QSPI_D0** | I/O | Prg | **QSPI Data 0**<br>QSPI interface data 0<br>Voltage Domain: 3.3 V |
| | GPIO9 | Prg | **General Purpose IO 9**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| R16 | **QSPI_D1** | I/O | Prg | **QSPI Data 1**<br>QSPI interface data 1<br>Voltage Domain: 3.3 V |
| | GPIO10 | Prg | **General Purpose IO 10**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| P16 | **QSPI_D2** | I/O | Prg | **QSPI Data 2**<br>QSPI interface data 2<br>Voltage Domain: 3.3 V |
| | GPIO11 | Prg | **General Purpose IO 11**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| P17 | **QSPI_D3** | I/O | Prg | **QSPI Data 3**<br>QSPI interface data 3<br>Voltage Domain: 3.3 V |
| | GPIO12 | Prg | **General Purpose IO 12**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| M15 | **QSPI_CLK** | O | Prg | **QSPI Clock**<br>QSPI interface clock output<br>Voltage Domain: 3.3 V |
| | GPIO13 | Prg | | **General Purpose IO 13**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |

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**Table 6 QSPI Management Interface Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| N15 | **QSPI_CS** | O | Prg | **QSPI Chip Select**<br>QSPI interface chip select<br>Voltage Domain: 3.3 V |
| | GPIO14 | Prg | | **General Purpose IO 14**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| L15 | **QSPI_RST** | O | Prg | **QSPI Reset**<br>QSPI Reset<br>Voltage Domain: 3.3 V |
| | GPIO15 | Prg | | **General Purpose IO 15**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |

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The product (or products) mentioned in this

### 2.2.3.4 Reset Interface

**Table 7 Reset Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| E4 | **HRSTN** | I | PU | **Hardware Reset**<br>Asynchronous active low device reset<br>Voltage Domain: 3.3 V |

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### 2.2.3.5 LED/UART/JTAG Interface

**Table 8 LED and Debug Interface Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **LED Signals** | | | | |
| E1 | **PHYLED1_0** | I/O | | **GPHY LED1 for Port 0**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO20 | Prg | Prg | **General Purpose IO 20**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |
| E2 | **PHYLED2_0** | I/O | | **GPHY LED2 for Port 0**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO21 | Prg | Prg | **General Purpose IO 21**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | FW_URXD | I | | **Firmware UART Data Input**<br>Firmware UART interface data input<br>Voltage Domain: 3.3 V |
| E3 | **PHYLED3_0** | I/O | | **GPHY LED3 for Port 0**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO22 | Prg | Prg | **General Purpose IO 22**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| F2 | **PHYLED1_1** | I/O | | **GPHY LED1 for Port 1**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO23 | Prg | Prg | **General Purpose IO 23**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |

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**Table 8 LED and Debug Interface Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| F3 | **PHYLED2_1** | I/O | | **GPHY LED2 for Port 1**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO24 | Prg | Prg | **General Purpose IO 24**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| G1 | **PHYLED3_1** | I/O | | **GPHY LED3 for Port 1**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO25 | Prg | Prg | **General Purpose IO 25**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| G2 | **PHYLED1_2** | I/O | | **GPHY LED1 for Port 2**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO26 | Prg | Prg | **General Purpose IO 26**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | TDI | I | | **JTAG Serial Test Data Input**<br>Voltage Domain: 3.3 V<br>*Note: No external pull-up required.* |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |
| H2 | **PHYLED2_2** | I/O | | **GPHY LED2 for Port 2**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO27 | Prg | Prg | **General Purpose IO 27**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | TMS | I | | **JTAG Test Mode Select**<br>Voltage Domain: 3.3 V<br>*Note: No external pull-up required.* |
| G3 | **PHYLED3_2** | I/O | | **GPHY LED3 for Port 2**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO28 | Prg | Prg | **General Purpose IO 28**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |

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**Table 8 LED and Debug Interface Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| J1 | **PHYLED1_3** | I/O | | **GPHY LED1 for Port 3**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO29 | Prg | Prg | **General Purpose IO 29**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | TCK | I | | **JTAG Test Clock**<br>The signals TDI, TDO, and TMS are synchronous, subject to this JTAG test clock.<br>Voltage Domain: 3.3 V |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |
| J2 | **PHYLED2_3** | I/O | | **GPHY LED2 for Port 3**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO30 | Prg | Prg | **General Purpose IO 30**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | TDO | I/O | | **JTAG Serial Test Data Output**<br>JTAG test data output.<br>Voltage Domain: 3.3 V<br>*Note: No external pull-up required.* |
| H3 | **PHYLED3_3** | I/O | | **GPHY LED3 for Port 3**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO31 | Prg | Prg | **General Purpose IO 31**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| J3 | **PHYLED1_4** | I/O | | **GPHY LED1 for Port 4**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO32 | Prg | Prg | **General Purpose IO 32**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |

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**Table 8 LED and Debug Interface Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| K2 | **PHYLED2_4** | I/O | | **GPHY LED2 for Port 4**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO33 | Prg | Prg | **General Purpose IO 33**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| L3 | **PHYLED3_4** | I/O | | **GPHY LED3 for Port 4**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO34 | Prg | Prg | **General Purpose IO 34**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| M1 | **PHYLED1_5** | I/O | | **GPHY LED1 for Port 5**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO35 | Prg | Prg | **General Purpose IO 35**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |
| M3 | **PHYLED2_5** | I/O | | **GPHY LED2 for Port 5**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO36 | Prg | Prg | **General Purpose IO 36**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| L2 | **PHYLED3_5** | I/O | | **GPHY LED3 for Port 5**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO37 | Prg | Prg | **General Purpose IO 37**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |

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**Table 8 LED and Debug Interface Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| M2 | **PHYLED1_6** | I/O | | **GPHY LED1 for Port 6**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO38 | Prg | Prg | **General Purpose IO 38**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |
| N3 | **PHYLED2_6** | I/O | | **GPHY LED2 for Port 6**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO39 | Prg | Prg | **General Purpose IO 39**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| N2 | **PHYLED3_6** | I/O | | **GPHY LED3 for Port 6**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO40 | Prg | Prg | **General Purpose IO 40**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| P1 | **PHYLED1_7** | I/O | | **GPHY LED1 for Port 7**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO41 | Prg | Prg | **General Purpose IO 41**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | FW_UTXD | O | | **Firmware UART Data Output**<br>Firmware UART interface data output<br>Voltage Domain: 3.3 V |
| P2 | **PHYLED2_7** | I/O | | **GPHY LED2 for Port 7**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO42 | Prg | Prg | **General Purpose IO 42**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |

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**Table 8 LED and Debug Interface Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| P3 | **PHYLED3_7** | I/O | | **GPHY LED3 for Port 7**<br>LED control output, drives single-color or dual color LEDs.<br>Voltage Domain: 3.3 V |
| | GPIO43 | Prg | Prg | **General Purpose IO 43**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| R3 | **TRSTN** | I | | **JTAG Test Enabling**<br>At logic HIGH, the GPIO pins are used as JTAG interface (TCK, TDI, TDO, and TMS).<br>At logic LOW, the GPIO pins are used in their normal application mode.<br>Voltage Domain: 3.3 V |

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### 2.2.3.6 Miscellaneous Signals

**Table 9 Miscellaneous Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Reset and Clocking** | | | | |
| E17 | **XTAL1** | AI | A | **Crystal: Oscillator Input**<br>A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must tie both pins to GND. |
| | CLK | AI | A | **Crystal Oscillator: Clock Input**<br>A clock of 25 or 50 MHz must be connected to CLK. See Section 7.7.2 for the clock details. XTAL2 must not be connected. |
| E16 | **XTAL2** | AO | A | **Crystal: Oscillator Output**<br>A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must tie both pins to GND. |
| G18 | **CLKP_0** | AO | A | **Differential Reference Clock Output 0**<br>These pins provide the 25, or 50 MHz differential reference clock used for a clock slave device. |
| G17 | **CLKN_0** | AO | A | **Differential Reference Clock Output 0**<br>These pins provide the 25, or 50 MHz differential reference clock used for a clock slave device. |
| N17 | **CLKP_1** | AO | A | **Differential Reference Clock Output 1**<br>These pins provide the 25, or 50 MHz differential reference clock used for a clock slave device. |
| N18 | **CLKN_1** | AO | A | **Differential Reference Clock Output 1**<br>These pins provide the 25, or 50 MHz differential reference clock used for a clock slave device. |
| J17 | **GPC0** | Prg | | **General Purpose Clock 0**<br>General purpose clock for external devices. Either input or output mode.<br>Voltage Domain: 3.3 V |
| | GPIO44 | Prg | Prg | **General Purpose IO 44**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | WSP_UTXD | Prg | Prg | **Software UART Data Output**<br>Voltage Domain: 3.3 V |

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The product (or products) mentioned in this

**Table 9 Miscellaneous Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| J18 | **GPC1** | Prg | | **General Purpose Clock 1**<br>General purpose clock for external devices. Either input or output mode.<br>Voltage Domain: 3.3 V |
| | GPIO45 | Prg | Prg | **General Purpose IO 45**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | WSP_UTXD | Prg | Prg | **Software UART Data Output**<br>Voltage Domain: 3.3 V |
| J16 | **GPC2** | Prg | | **General Purpose Clock 2**<br>General purpose clock for external devices. Either input or output mode.<br>Voltage Domain: 3.3 V |
| | GPIO46 | Prg | Prg | **General Purpose IO 46**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | WSP_URXD | Prg | Prg | **Software UART Data Input**<br>Voltage Domain: 3.3 V |
| H17 | **GPC3** | Prg | | **General Purpose Clock 3**<br>General purpose clock for external devices. Either input or output mode.<br>Voltage Domain: 3.3 V |
| | GPIO47 | Prg | Prg | **General Purpose IO 47**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| L16 | **GPIO0** | Prg | Prg | **General Purpose IO 0**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 1.8 V / 3.3 V |
| | EXTINT0 | Prg | Prg | **External Interrupt 0**<br>Voltage Domain: 1.8 V / 3.3 V |
| D5 | **GPIO1** | Prg | Prg | **General Purpose IO 1**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| | EXTINT1 | Prg | Prg | **External Interrupt 1**<br>Voltage Domain: 3.3 V |
| | WSP_URXD | Prg | Prg | **Software UART Data Input**<br>Voltage Domain: 3.3 V |

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**Table 9 Miscellaneous Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| P4 | **GPIO2** | Prg | Prg | **General Purpose IO 2**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| K4 | **GPIO3** | Prg | Prg | **General Purpose IO 3**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| L18 | **GPIO7** | Prg | Prg | **General Purpose IO 7**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 1.8 V / 3.3 V |
| L17 | **GPIO8** | Prg | Prg | **General Purpose IO 8**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 1.8 V / 3.3 V |
| F18 | **GPIO16** | Prg | Prg | **General Purpose IO 16**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| F17 | **GPIO17** | Prg | Prg | **General Purpose IO 17**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| M17 | **GPIO18** | Prg | Prg | **General Purpose IO 18**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |
| M16 | **GPIO19** | Prg | Prg | **General Purpose IO 19**<br>Either input or output mode. The output characteristic is either open drain or push-pull.<br>Voltage Domain: 3.3 V |

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### 2.2.3.7 Power Supply for GPHY

**Table 10 Power Supply Pins for GPHY**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| C12 | **VDDA3V3_0** | PWR | | **GPHY 0 High Voltage Domain Supply**<br>This is the PHY 0 AFE 3.3 V supply. |
| C10 | **VDDA3V3_1** | PWR | | **GPHY 1 High Voltage Domain Supply**<br>This is the PHY 1 AFE 3.3 V supply. |
| C8 | **VDDA3V3_2** | PWR | | **GPHY 2 High Voltage Domain Supply**<br>This is the PHY 2 AFE 3.3 V supply. |
| C6 | **VDDA3V3_3** | PWR | | **GPHY 3 High Voltage Domain Supply**<br>This is the PHY 3 AFE 3.3 V supply. |
| T6 | **VDDA3V3_4** | PWR | | **GPHY 4 High Voltage Domain Supply**<br>This is the PHY 4 AFE 3.3 V supply. |
| T8 | **VDDA3V3_5** | PWR | | **GPHY 5 High Voltage Domain Supply**<br>This is the PHY 5 AFE 3.3 V supply. |
| T10 | **VDDA3V3_6** | PWR | | **GPHY 6 High Voltage Domain Supply**<br>This is the PHY 6 AFE 3.3 V supply. |
| T12 | **VDDA3V3_7** | PWR | | **GPHY 7 High Voltage Domain Supply**<br>This is the PHY 7 AFE 3.3 V supply. |
| D8 | **VDDA1V8_0** | PWR | | **GPHY 0, 1, 2, 3 AFE Voltage Domain Supply**<br>This is the 1.8 V supply for PHY 0 to PHY 3 AFE voltage domain. It supplies mixed signal blocks in the AFE. |
| R8 | **VDDA1V8_1** | PWR | | **GPHY 4, 5, 6, 7 AFE Voltage Domain Supply**<br>This is the 1.8 V supply for PHY 4 to PHY 7 AFE voltage domain. It supplies mixed signal blocks in the AFE. |
| F7, F12 | **VDDA0V8_0** | PWR | | **GPHY 0, 1, 2, 3 Low Voltage Domain Supply**<br>This is the supply for PHY 0 to PHY 3 low voltage domain. It supplies mixed signal blocks in the AFE. |
| N7, N12 | **VDDA0V8_1** | PWR | | **GPHY 4, 5, 6, 7 Low Voltage Domain Supply**<br>This is the supply for PHY 4 to PHY 7 low voltage domain. It supplies mixed signal blocks in the AFE. |
| G4, H4, L4, M4 | **VDD3V3PAD0** | PWR | | **Power Supply Digital Domain 3.3 V**<br>3.3 V Voltage Digital Power Supply |
| F15, G15, P15 | **VDD3V3PAD1** | PWR | | **Power Supply Digital Domain 3.3 V**<br>3.3 V Voltage Digital Power Supply |
| J15 | **VDDP_PAD** | PWR | | **Power Supply Digital Domain 1.8 V / 3.3 V**<br>3.3 V or 1.8 V Pad Voltage Digital Power Supply based on pin strapping. |

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**Table 10 Power Supply Pins for GPHY** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| G6, H6, G8, H8, H10, H11, G12, G13, J7, K7, J9, K9, L6, M6, L8, M8, L10, L11, M12, M13 | **VDDD0V8_COR** | PWR | | **Power Supply Digital Domain 0.8 V**<br>0.8 V Core Voltage Digital Power Supply |
| J13 | **VDDA1V8PORXO** | PWR | | **Power Supply Domain 1.8 V** |
| D9 | **VDDA1V8_0** | PWR | | **Power Supply Domain 1.8 V** |
| R9 | **VDDA1V8_1** | PWR | | **Power Supply Domain 1.8 V** |
| F10, G10 | **VDDA1V2CDB0** | PWR | | **Power Supply Domain 1.2 V** |
| M10, N10 | **VDDA1V2CDB1** | PWR | | **Power Supply Domain 1.2 V** |
| F9 | **VDDA0V8_0** | PWR | | **Power Supply Domain 0.8 V** |
| N9 | **VDDA0V8_1** | PWR | | **Power Supply Domain 0.8 V** |
| L13 | **VDDA1V8_PLL** | PWR | | **Power Supply Domain 1.8 V** |
| J11 | **VDDD0V8REF** | PWR | | **Power Supply Digital Domain 0.8 V** |
| K11 | **VDDD0V8POST** | PWR | | **Power Supply Digital Domain 0.8 V** |
| H12 | **VDDA1V8_CML** | PWR | | **Power Supply Domain 1.8 V** |
| K12 | **VDDA0V8_CML** | PWR | | **Power Supply Domain 0.8 V** |
| K13 | **VDDA1V8_PVT** | PWR | | **Power Supply Domain 1.8 V** |
| J12 | **VCC1V8_OTP** | PWR | | **Power Supply Domain 1.8 V** |
| C15, D14 | **VA0V8_0** | PWR | | **0.8 V Analog Domain Supply** |
| D15 | **VPHA1V8_0** | PWR | | **1.8 V Domain Supply** |
| R14, T15 | **VA0V8_1** | PWR | | **0.8 V Analog Domain Supply** |
| R15 | **VPHA1V8_1** | PWR | | **1.8 V Domain Supply** |

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### 2.2.3.8 Power Supply for TPI (AFE)

**Table 11 Power Supply Pins for TPI (AFE)**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| A1, A16, C4, C5, C7, C9, C11, C13, C14, D2, D6, D7, D10, D12, D13, F6, F8, F11, F13 | **TPVSSA_0** | GND | | **Analog Ground** |
| N6, N8, N11, N13, R2, R6, R7, R10, R12, R13, T4, T5, T7, T9, T11, T13, T14, V1, V16 | **TPVSSA_1** | GND | | **Analog Ground** |

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### 2.2.3.9 Ground

**Table 12 Ground Pins**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| D3, D4, E15, F4, G7, H7, G9, H9, G11, H15, H16, J4, J6, K6, J8, K8, J10, K10, K1, K3, K15, L7, M7, L9, M9, M11, L12, N4, N16, R4, R5 | **VSSD** | GND | | **Digital Ground** |
| A18, B18, C16, D18, R18, T16, U18, V18 | **UVSS** | GND | | **Ground** |
| D16, D17, F16, H13 | **VSS_XO** | GND | | **XO Device Ground**<br>XO ground |

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### 2.2.3.10 Not Connected Signals

**Table 13 Not Connected Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| A17, B16, B17, C17, C18, T17, T18, U16, U17, V17 | **NC** | - | - | **No Connect**<br>These pins should not be connected. |

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# 3 Functional Description

## 3.1 Power Supply, Clock, and Reset

This section provides the information required to power up the MxL86280C.

### 3.1.1 Power Supply

These four power supply rails are required: 3.3 V, 0.8 V, 1.8 V, and 1.2 V. **Section 7.7.1** contains the power-up sequence.

### 3.1.2 Clock

An internal PLL circuit generates the required internal clocks, based on an external reference clock.

The available options are:

- An external 25 MHz crystal connected to the MxL86280C. **Section 7.7.8** documents the required crystal specification.
- 25 MHz direct from an external oscillator
- An external CML/LVPECL reference clock operating at 50 MHz

The MxL86280C provides two pairs of CML differential clock output to drive other chips. The available clock frequencies are:

- Input reference clock frequency
- 50 MHz

### 3.1.3 Reset Generation

The external hardware reset input (HRSTN pin) resets all the hardware modules including the pin strapping information during boot:

- Driving the HRSTN pin low causes an asynchronous reset of the MxL86280C system.
- Releasing the HRSTN pin high triggers the power-on sequence.

The HRSTN pin is internally connected to a weak internal pull-up resistor.

### 3.1.4 Power-On Sequence

The MxL86280C powers on when the power is applied and the HRSTN pin is high. See **Figure 25**.

The steps executed at power on are:

1. Lock the internal PLL.
2. Read the pin strap information, see **Section 3.1.5** for more information.
3. Boot the microprocessor from the internal ROM.
4. Authenticate the firmware image in the flash memory device.
5. Auto-negotiate the link speeds for the Ethernet TPI interfaces.
6. Train and link up each interface in accordance with the IEEE 802.3 **[2]** standards.

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### 3.1.5 Configuration by Pin Strapping

The MxL86280C is configurable by means of pin strapping on a number of the GPIO pins. The pin strapping configurations are captured during the chip power-on sequence until the reset initialization is complete.

The pin strap values are set to logical high or low by connecting the corresponding pin via an external 1 kΩ resistor to either ground or the pin supply voltage.

Table 14 and Table 15 describe the pin strap mapping.

**Table 14 Pin Names Used for Pin Strapping**

| Ball Name | Ball Number | Configuration Item Description |
|---|---|---|
| GPC1 | J18 | PS_PHY_MADDR(4) |
| GPC2 | J16 | PS_PHY_MADDR(3) |
| GPC3 | H17 | PS_CLK_SEL |
| GPIO1 | D5 | PS_CLK_SEL1 |
| GPIO2 | P4 | PS_RJ45_TAB |
| MDINT | G16 | PS_MDINT_POLARITY |
| GPIO3 | K4 | PS_MDIO_VOLTAGE |
| GPC0 | J17 | PS_SUPER_ISOLATE |

**Table 15 Pin Strapping Configuration Description**

| Pin Strapping Signals | Description |
|---|---|
| PS_PHY_MADDR(4:3) | **MDIO Address**<br>Specifies the most significant two bits of the MDIO address. The lowest three bits of the switch MDIO address are hard-coded to 0. |
| PS_MDINT_POLARITY | **MDIO Interrupt Polarity**<br>Specifies the polarity of the MDIO interrupt.<br>$0_B$ **HIGH** MDIO interrupt is active high.<br>$1_B$ **LOW** MDIO interrupt is active low. |
| PS_RJ45_TAB | **RJ45 Tab Configuration**<br>Specifies the tab-up or tab-down configuration of the RJ45. Each BASE-T port has the same configuration.<br>$1_B$ **DOWN** Tab-down<br>$0_B$ **UP** Tab-up |
| PS_MDIO_VOLTAGE | **MDIO Voltage**<br>Specifies whether the maximum voltage level used by the MDIO signals is 3.3 V or 1.8 V.<br>$0_H$ **LOW** MDIO_S, MDC_S, MDINT, GPIO7, GPIO8, and GPIO0 signal pins are supplied with 1.8 V. In this configuration, $V_{DDP}$ must be supplied with 1.8 V.<br>$1_H$ **NORMAL** MDIO_S, MDC_S, MDINT, GPIO7, GPIO8, and GPIO0 signal pins are supplied with 3.3 V. In this configuration, $V_{DDP}$ must be supplied with 3.3 V. |

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**Table 15 Pin Strapping Configuration Description** (cont'd)

| Pin Strapping Signals | Description |
|---|---|
| PS_CLK_SEL<br>PS_CLK_SEL1 | **Input Clock Selection**<br>Specifies the input clock frequency used. MSB is PS_CLK_SEL1. LSB is PS_CLK_SEL.<br>$11_B$ **25** 25 MHz<br>$10_B$ **50** 50 MHz<br>$01_B$ **RES** Reserved<br>$00_B$ **RES** Reserved |
| PS_SUPER_ISOLATE | **Super Isolate**<br>Specifies whether the PHY is immediately active after a reset or is halted until it is manually activated.<br>$0_H$ **HALT** The PHYs are inactive after reset.<br>$1_H$ **NORMAL** The PHYs are active after reset. |

Alternative ways to configure the MxL86280C after the boot process are to use the MDIO interface [1] and write into various control registers, as detailed in Section 3.3, or to use the FCA [1].

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## 3.2 MDIO Slave Interface

The SMDIO module and the MDIO Device 30 module are directly attached to the MDIO slave interface as shown in the **Figure 4**. The MDIO Device 30 is the vendor specific 1 device for MMD=30, which supports both IEEE 802.3 clause 22 and clause 45 protocol. It allows access to the switch and the PHY configurations using the correct MDIO PHY address. The MDIO address used for this access is configurable through pin-strapping, as described in **Section 3.1.5**. A switch driver executed by the micro-controller in the figure allows configuration of the MxL86280C. The switch driver is part of the host SoC API software documented in the MxL86280C API.

The SMDIO module provides access to the external flash memory device via the QSPI interface. The MxL86280C supports downloading of firmware to the flash memory device via the SMDIO module attached to the MDIO bus. The MDIO address used for this access is the same MDIO address as defined by the pin strapping. The MxL86280C user guide **[1]** describes the driver software executed on the external processor which must be followed to perform this feature. The SMDIO module supports only IEEE 802.3 clause 22 protocol.

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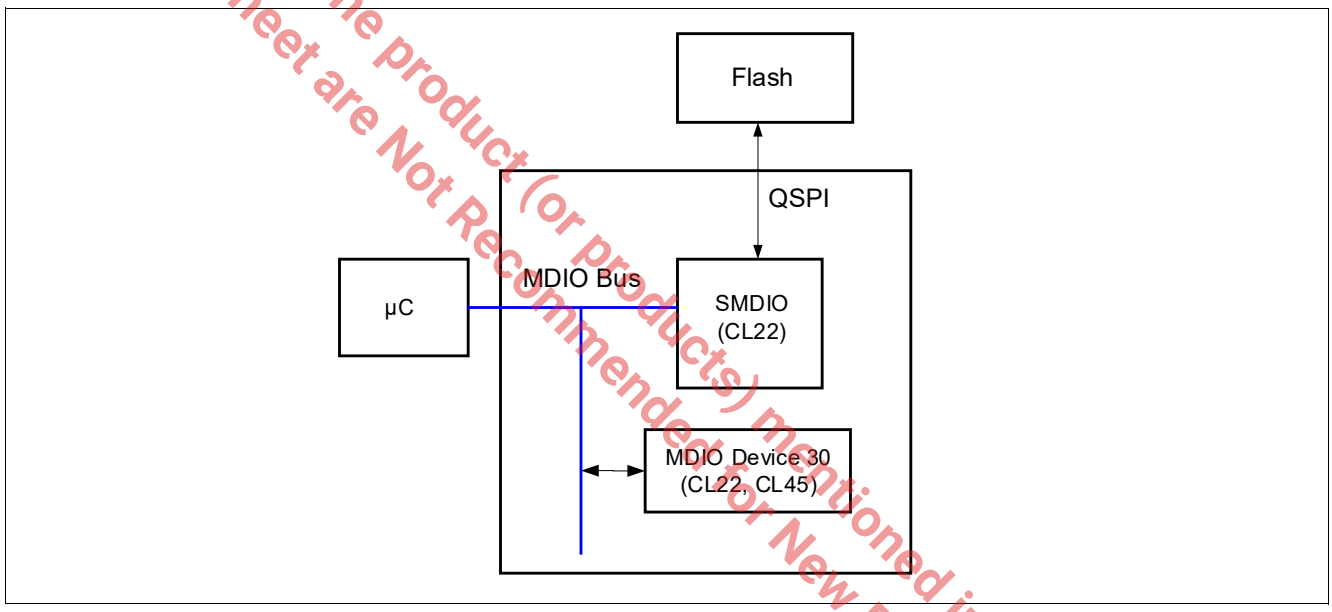



**Figure 4 MDIO Slave**

When other devices in the system need to be configured through MDIO, they must be connected to the MDIO slave interface and configured such that no addressing conflict arises.

The standard MDIO protocol requires a 32-bit preamble at the beginning of each read or write access. To speed up the data exchange, reduce the preamble down to 1 bit for the second and subsequent accesses.

The standard MDIO protocol uses a clock rate of 2.5 MHz on MDC. To speed up the data exchange, increase the clock applied on MDC_S to the maximum 25 MHz. **Section 7.7.4** contains more details on AC characteristics.

## 3.3 Configuration via MDIO Management Interface

It is possible to connect an external controller's STA to the chip's slave MDIO interface. This allows access to the MDIO and MMD registers standardized in IEEE 802.3, enabling the STA to control the chip configuration and retrieve status information. The MDIO transactions are any of the three types described in IEEE 802.3 Clause 22, Clause 22 Extended, and Clause 45 [2].

Figure 5 and Table 16 show the minimum time required for the MDIO to be available for access.

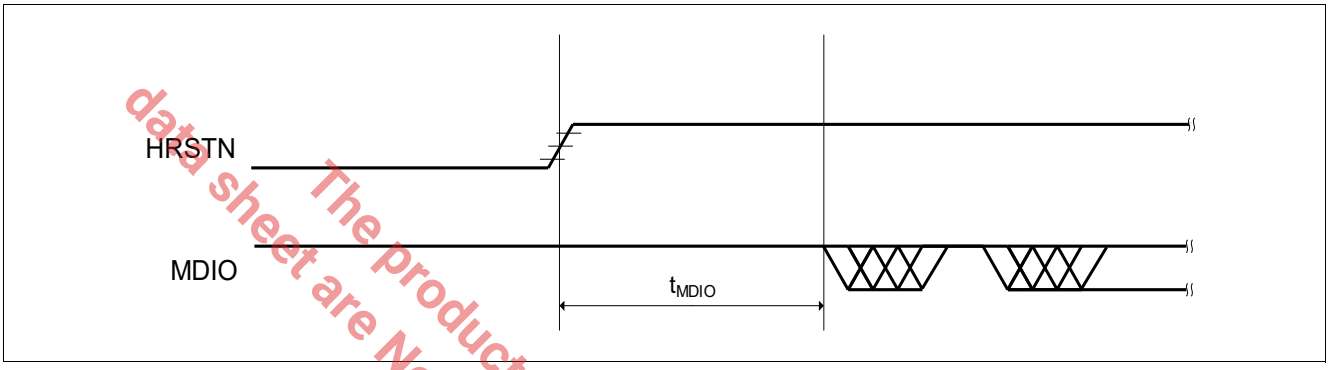



**Figure 5 MDIO Access Timing**

**Table 16 MDIO Ready Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| MDIO Ready Time | $T_{MDIO}$ | 750 | – | | ms | |

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## 3.4 Quad Serial Peripheral Interface

A Quad Serial Peripheral Interface (QSPI) is equipped to provide access to external Quad-SPI flash memory devices. The MxL86280C requires an external Quad-SPI flash memory to operate.

The QSPI supports:

- Up to 101.5625 MHz for single/double data rate
- eXecution In Place (XIP), fully memory mapped access for CPU
- Addressing up to 512 MB range

### 3.4.1 Supported Flash Memory Devices

Table 17 lists the qualified flash memory devices. However, it is possible for the user to select a device not present in the list after consideration of command compatibility and timing compatibility as listed in Table 18. The flash memory device must support 101.5625 MHz single data rate.

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**Table 17 Supported Flash Memory Devices**

| Vendor | Model |
|---|---|
| Macronix | MX25L6433F |
| Winbond | W25Q64JV-DTR |

**Table 18 Flash Command and Timing**

| Instruction | Abbreviation | Command | Command Cycles | Address Cycles | Dummy Cycles | Data Cycles |
|---|---|---|---|---|---|---|
| Write Enable | WREN | $06_H$ | 8 | 0 | 0 | 0 |
| Write Disable | WRDI | $04_H$ | 8 | 0 | 0 | 0 |
| Read ID | RDID | $9F_H$ | 8 | 0 | 0 | 24 |
| Read Status Register | RDSR | $05_H$ | 8 | 0 | 0 | 8 |
| Write Status Register | WRSR | $01_H$ | 8 | 0 | 0 | 8 |
| Read Configuration Register | RDCR | $15_H$ | 8 | 0 | 0 | 8 |
| Read Data Bytes | READ | $03_H$ | 8 | 24 | 0 | 8 |
| Fast Read | FREAD | $0B_H$ | 8 | 24 | 8 | 8 |
| Quad Read | 4READ | $EB_H$ | 8 | 6 | 10 | 2 |
| XIP | XIP | $EB_H$ | 8 | 6 | 10 | 2 x n[1)] |
| Chip Erase | CE | $C7_H$ | 8 | 0 | 0 | 0 |
| Block Erase | BE | $D8_H$ | 8 | 24 | 0 | 0 |
| Sector Erase | SE | $20_H$ | 8 | 24 | 0 | 0 |
| Page Program | PP | $02_H$ | 8 | 24 | 0 | 8 x n[1)] |
| Reset Enable | RSTEN | $66_H$ | 8 | 0 | 0 | 0 |
| Reset | RST | $99_H$ | 8 | 0 | 0 | 0 |

1) n is the number of bytes

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## 3.5 GPIO Mapping

Other than the GPIO functionality, the GPIO pins are also shared with other alternative functions. The GPIO pins are configurable to alternative functions, which are based on the pinmux settings as shown in Table 19.

**Table 19 GPIO Mapping**

| Pinmux Mode 0 (Default) | Pinmux Mode 1 | Pinmux Mode 2 | Pinmux Mode 3 |
|---|---|---|---|
| GPIO0 | GPIO0 | EXTINT0 | — |
| GPIO1 | GPIO1 | EXTINT1 | WSP_URXD |
| GPIO2 | GPIO2 | — | — |
| GPIO3 | GPIO3 | — | — |
| MDINT | GPIO4 | — | — |
| MDC_S | GPIO5 | — | — |
| MDIO_S | GPIO6 | — | — |
| — | GPIO7 | — | — |
| — | GPIO8 | — | — |
| QSPI_D0 | GPIO9 | — | — |
| QSPI_D1 | GPIO10 | — | — |
| QSPI_D2 | GPIO11 | — | — |
| QSPI_D3 | GPIO12 | — | — |
| QSPI_CLK | GPIO13 | — | — |
| QSPI_CS | GPIO14 | — | — |
| QSPI_RST | GPIO15 | — | — |
| — | GPIO16 | — | — |
| — | GPIO17 | — | — |
| — | GPIO18 | — | — |
| — | GPIO19 | — | — |
| PHYLED1_0 | GPIO20 | — | FW_UTXD |
| PHYLED2_0 | GPIO21 | — | FW_URXD |
| PHYLED3_0 | GPIO22 | — | — |
| PHYLED1_1 | GPIO23 | — | — |
| PHYLED2_1 | GPIO24 | — | — |
| PHYLED3_1 | GPIO25 | — | — |
| PHYLED1_2 | GPIO26 | — | TDI |
| PHYLED2_2 | GPIO27 | — | TMS |
| PHYLED3_2 | GPIO28 | — | — |
| PHYLED1_3 | GPIO29 | — | TCK |
| PHYLED2_3 | GPIO30 | — | TDO |
| PHYLED3_3 | GPIO31 | — | — |
| PHYLED1_4 | GPIO32 | — | — |
| PHYLED2_4 | GPIO33 | — | — |
| PHYLED3_4 | GPIO34 | — | — |

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**Table 19 GPIO Mapping** (cont'd)

| Pinmux Mode 0 (Default) | Pinmux Mode 1 | Pinmux Mode 2 | Pinmux Mode 3 |
|---|---|---|---|
| PHYLED1_5 | GPIO35 | — | — |
| PHYLED2_5 | GPIO36 | — | — |
| PHYLED3_5 | GPIO37 | — | — |
| PHYLED1_6 | GPIO38 | — | — |
| PHYLED2_6 | GPIO39 | — | — |
| PHYLED3_6 | GPIO40 | — | — |
| PHYLED1_7 | GPIO41 | — | — |
| PHYLED2_7 | GPIO42 | — | — |
| PHYLED3_7 | GPIO43 | — | — |
| GPC0 | GPIO44 | WSP_UTXD | — |
| GPC1 | GPIO45 | — | WSP_UTXD |
| GPC2 | GPIO46 | — | WSP_URXD |
| GPC3 | GPIO47 | — | — |

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## 3.6 Ethernet PHY Interface

The Ethernet PHY implements the physical layer of the Ethernet standard. It supports Digital Signal Processing (DSP) and Analog Signal Processing (ASP) functions in transmitting data over the twisted pair cable.

### 3.6.1 Twisted Pair Interface

The Twisted Pair Interface (TPI) of the MxL86280C is fully compliant with IEEE 802.3. The MxL86280C integrates series resistors required to terminate the TPI links with a 100 Ω nominal impedance to facilitate a low-power implementation and reduce PCB costs. As a consequence, it is possible to connect the TPI pins directly via a transformer to the RJ45 connector. Additional external circuitry is required for common-mode termination and rejection as described in **Section 7.8.1**.

**Figure 6** shows a schematic of the TPI circuitry taking these components into account.

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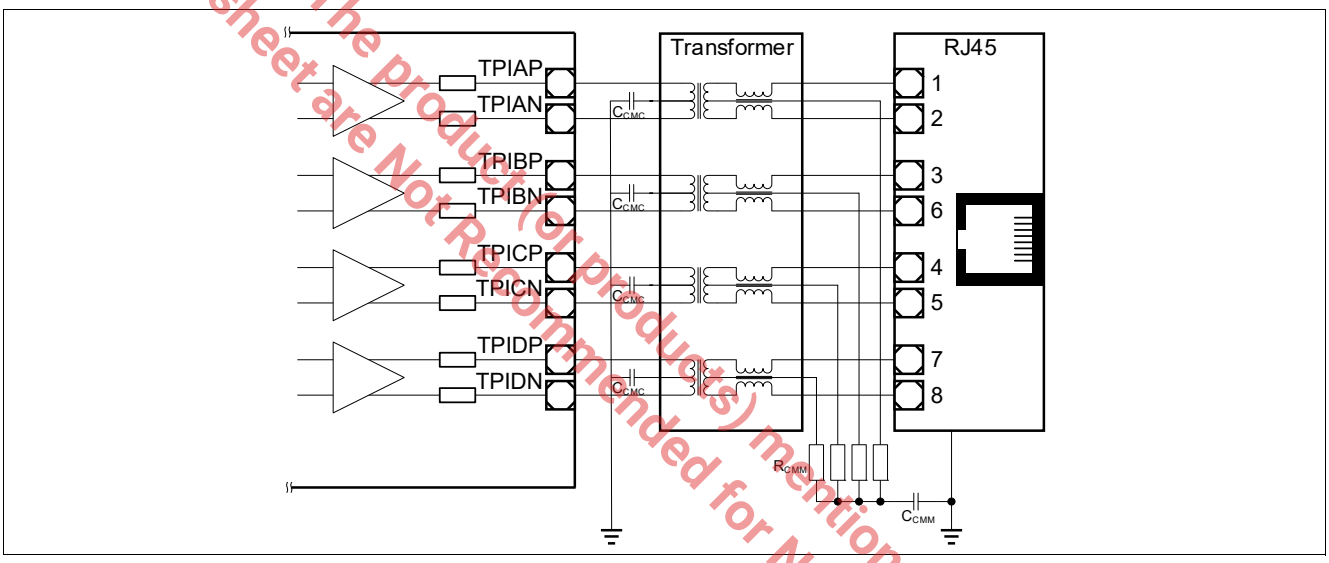



**Figure 6 Twisted-Pair Interface of MxL86280C Including Transformer and RJ45 Plug**

### 3.6.2 Transformerless Ethernet

Transformerless Ethernet (TLE) is required for backplane applications where the use of a transformer is not always required to fulfill the galvanic decoupling requirements of the isolation specifications. In such applications, removing the transformer reduces both the external bill of material and the space requirements on the PCB.
As the MxL86280C incorporates a voltage-mode line driver, the only stringent requirement is to use AC coupling, which is achievable using simple SMD type series capacitors. The value of the capacitors is selected such that the high-pass characteristics correspond to an equivalent standard transformer based application. The recommended value is $C_{coupling}$ = 100 nF. **Figure 7** shows the external circuitry for TLE.

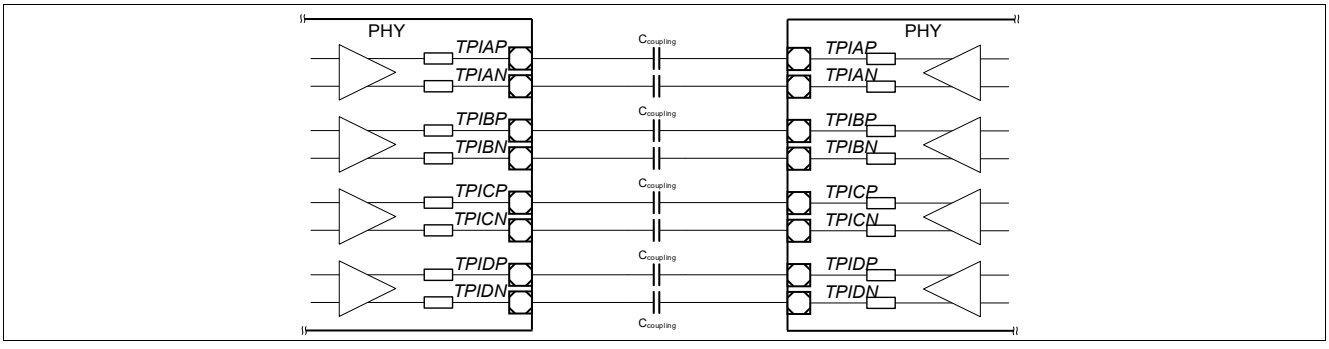



**Figure 7 External Circuitry for the Transformerless Ethernet Application**

### 3.6.3 Auto-Negotiation

The MxL86280C supports auto-negotiation (ANEG) as part of the startup procedure to exchange capability information with the link partner. ANEG is enabled at the MxL86280C initialization and its 2.5 Gbps speed capability is advertised. The ANEG procedure is executed according to IEEE 802.3 Clause 28, Clause 40, and IEEE 802.3 Clause 126 [2]. When the link partner does not support ANEG, the MxL86280C determines the link speed configuration using parallel detection as described in Clause 28.

With MDIO commands, it is possible to disable ANEG and change the advertised link rates. The STA is also able to disable ANEG. In this situation, the system configuration must ensure compatibility between link partners to allow link up in a compatible mode.

***Attention:** STD_CTRL.DPLX only takes effect when the ANEG process is disabled and the GPHY TPI is not operating in loopback mode, that is, bits STD_CTRL.ANEN and STD_CTRL.LB are set to zero. Forced half-duplex mode (STD_CTRL.DPLX = 0b0) is only supported in 10BASE-T and 100BASE-TX speed modes.*
*This field is ignored for higher speeds.*

### 3.6.4 Auto-Downspeed

The auto-downspeed (ADS) feature implements a process to renegotiate the link with a lower speed when the link quality is insufficient. The feature ensures maximum interoperability even in harsh, or inadequate, cable infrastructure environments. In particular, ADS is applied during the 2.5GBASE-T/1000BASE-T training phase. ADS is also required when the quality or characteristics of the cable in use cannot support the advertised speed.

For example, it is possible to advertise 2.5GBASE-T/1000BASE-T during ANEG when both link partners are connected via a cable that does not support the 4-pair Gigabit Ethernet mode. The MxL86280C detects such a configuration to avoid repeating link up failures and clears the 2.5GBASE-T/1000BASE-T capability in the ANEG advertisement registers. After the resulting link down, the next ANEG procedure no longer advertises 1000BASE-T/2.5GBASE-T. The next link up is done at the next advertised speed below 1000 Mbps.

The MxL86280C also executes an ADS procedure when the signal quality is not suited to a 1000BASE-T/2.5GBASE-T link up due to increased alien noise or a loop length that significantly exceeds the standard specification.

When the MxL86280C is configured not to advertise a speed capability below 1000 Mbps, the ADS feature is automatically disabled.

### 3.6.5 Polarity Reversal Correction

For each of the 4 pairs, the MxL86280C automatically detects and corrects any inversion of the signal polarity on the P and N signals. The detection is done during the auto-negotiation phase. The detected polarity is frozen when the link is established, and remains unchanged until the link is dropped.

The polarity corrections applied are indicated in the register: `PMA_MGBT_POLARITY` (register 1.130); and are valid after auto-negotiation is complete.

### 3.6.6 Auto-Crossover Correction

To maximize interoperability, even in inadequate wiring environments, the MxL86280C automatically performs cable crossover (MDI-X) correction. **Table 20** lists the supported pair-mappings detectable and correctable by the device.

The MxL86280C automatically detects and corrects crossed cable configuration, where the transmit-receive pairing between partners does not match. The auto-crossover function is fully compliant with IEEE 802.3, Clause 40.4.4 [2], in 1000BASE-T and 2.5GBASE-T mode.

The corrections applied are indicated in the register: `PMA_MGBT_POLARITY` (register 1.130) and are valid when auto-negotiation is complete.

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**Table 20 Supported Twisted Pair Mappings on a Cat 5 or Better Cable**

| Crossover Modes on RJ45[1)] | | RJ45 Pinning | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Mode** | **Description** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** |
| 11 | Straight cable, standard compliant | TPIAP **(A+)** | TPIAN **(A-)** | TPIBP **(B+)** | TPICP **(C+)** | TPICN **(C-)** | TPIBN **(B-)** | TPIDP **(D+)** | TPIDN **(D-)** |
| 00 | Full Gigabit Ethernet MDI-X This is standard-compliant MDI-X with pair A/B swapped and pair C/D swapped. | TPIBP **(B+)** | TPIBN **(B-)** | TPIAP **(A+)** | TPIDP **(D+)** | TPIDN **(D-)** | TPIAN **(A-)** | TPICP **(C+)** | TPICN **(C-)** |

1) This pin assignment is according to TIA/EIA-568-A/B.

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### 3.6.7 RJ45 Tab Up or Tab Down Configuration

**Figure 8** shows that the RJ45 plug on the system PCB is solderable with the tab either up or down.

The difference between tab up and tab down is a swap in position between A and D, and a swap in position between B and C. The pin strap `PS_RJ45_TAB` allows the system designer to perform this configuration. As a result, a PCB layout does not need to be modified when a RJ45 tab up or down socket needs to be mounted. The single pin strap is applicable to all ports, which are either all tab down or all tab up.

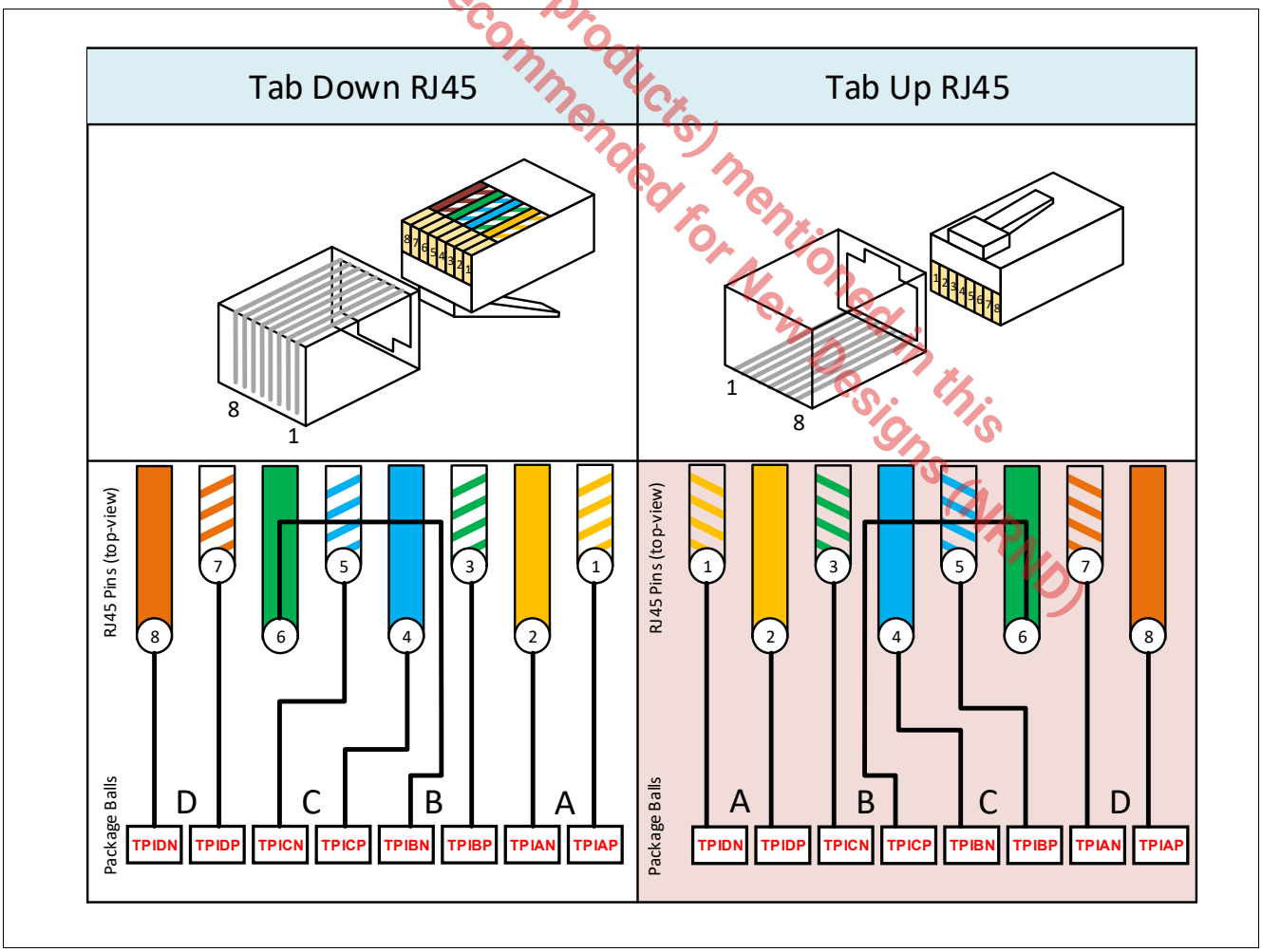



**Figure 8 RJ45 Tab Up or Tab Down Configuration**

### 3.6.8 Wake-on-LAN

The MxL86280C supports WoL. The MxL86280C generates an interrupt to an external controller or to an internal controller when it detects special WoL Ethernet packets. This allows the controller to enter sleep mode when there is no Ethernet traffic to process, and be woken up when traffic starts. WoL packets are detected at all link speeds. **Figure 9** shows the scenario when connected to an external device.

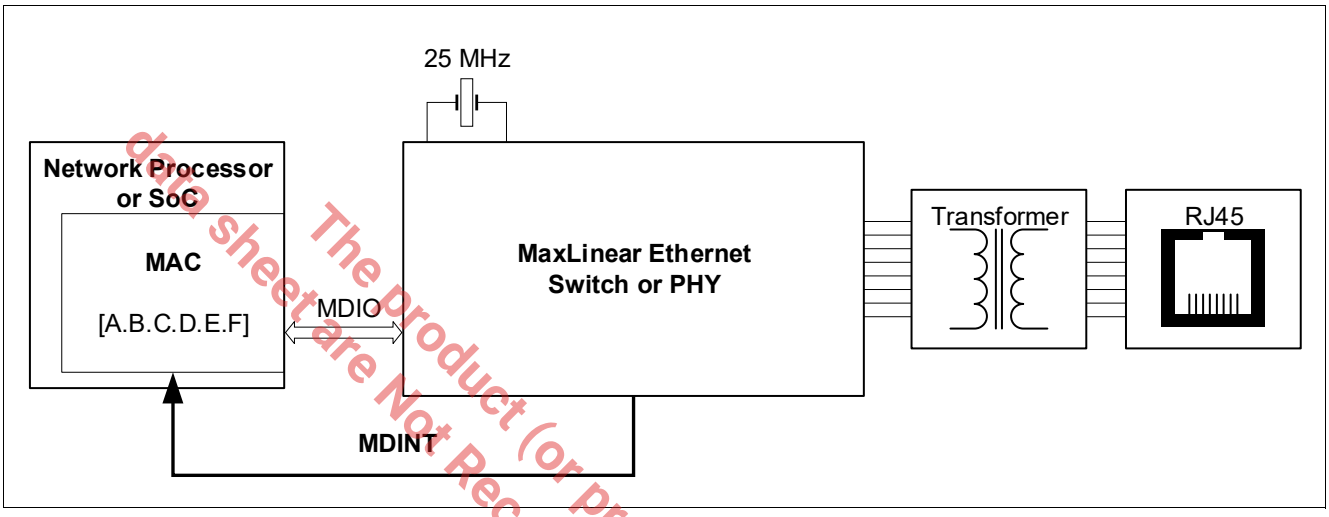



**Figure 9 WoL Application Block Diagram**

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The most commonly used WoL packet is called a magic packet, which contains the MAC address of the device to be woken up, and an optional password called SecureON. The MAC address and the optional SecureON password relevant for the WoL logic inside the MxL86280C are configurable in the WoL MDIO registers in the Vendor Specific 2, VSPEC2 MMD, device described in **Chapter 4**. When such a configured magic packet is received, an interrupt is issued.

**Table 21** gives an example programming sequence for these configuration registers.

**Table 21 Programming Sequence for the Wake-on-LAN Functionality**

| Step | Register Access | Remark |
|---|---|---|
| 1 | `MDIO.MMD.WOLAD01` = $EEFF_H$ | Programs the fifth and sixth MAC address bytes. |
| 2 | `MDIO.MMD.WOLAD23` = $CCDD_H$ | Programs the third and fourth MAC address bytes. |
| 3 | `MDIO.MMD.WOLAD45` = $AABB_H$ | Programs the first and second MAC address bytes. |
| 4 | `MDIO.MMD.WOLPW01` = $4455_H$ | Programs the fifth and sixth SecureON password bytes. |
| 5 | `MDIO.MMD.WOLPW23` = $2233_H$ | Programs the third and fourth SecureON password bytes. |
| 6 | `MDIO.MMD.WOLPW45` = $0011_H$ | Programs the first and second SecureON password bytes. |
| 7 | `MDIO.PHY.IMASK.WOL` = $1_B$ | Enables the wake-on-LAN interrupt mask. |
| 8 | `MDIO.MMD.WOLCTRL.WOL.EN` = $1_B$ | Enables wake-on-LAN functionality. |

## 3.7 LED Interface

This section describes the LED interface.

### 3.7.1 LED

The MxL86280C allows 24 synchronized LEDs to be used for visual status indication. Each LED pin drives either a single color LED or dual color LED.

### 3.7.2 LED Configuration

The MxL86280C API describing the driver software executed on the Host SoC must be followed to configure this interface. When there is no Host SoC attached, it is possible for the configurations to be done in the FCA [1].

**Figure 10** shows the external LED connected to either ground or the power rail in single color mode.

**Figure 11** and **Figure 12** show the connection of single and dual color LEDs when the pin is also used for pin strapping.

*Note: These figures do not show the full recommended circuits with all the necessary components. Refer to the relevant HDK/EVK PCB design documentation for more details.*

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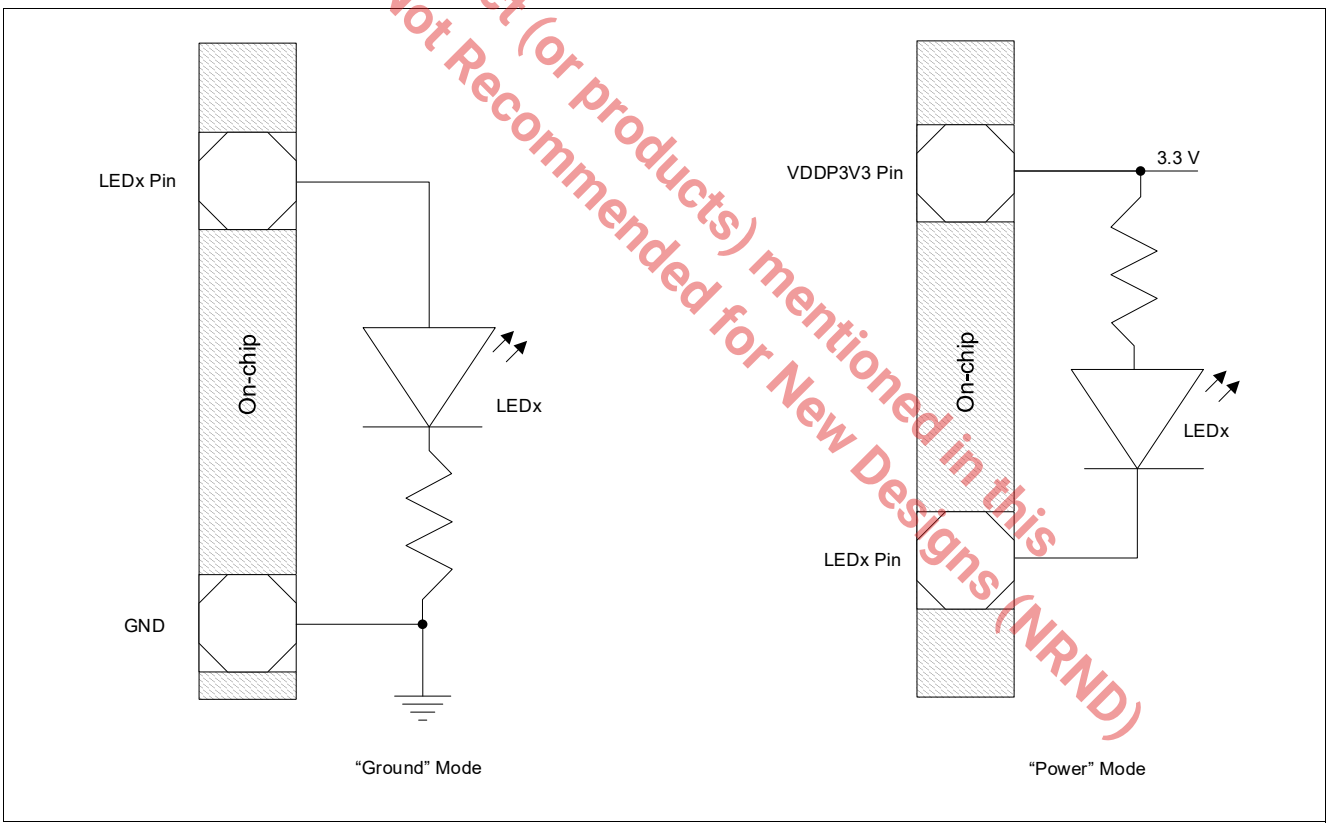



**Figure 10 LED Connection Options to Ground or Power Supply**

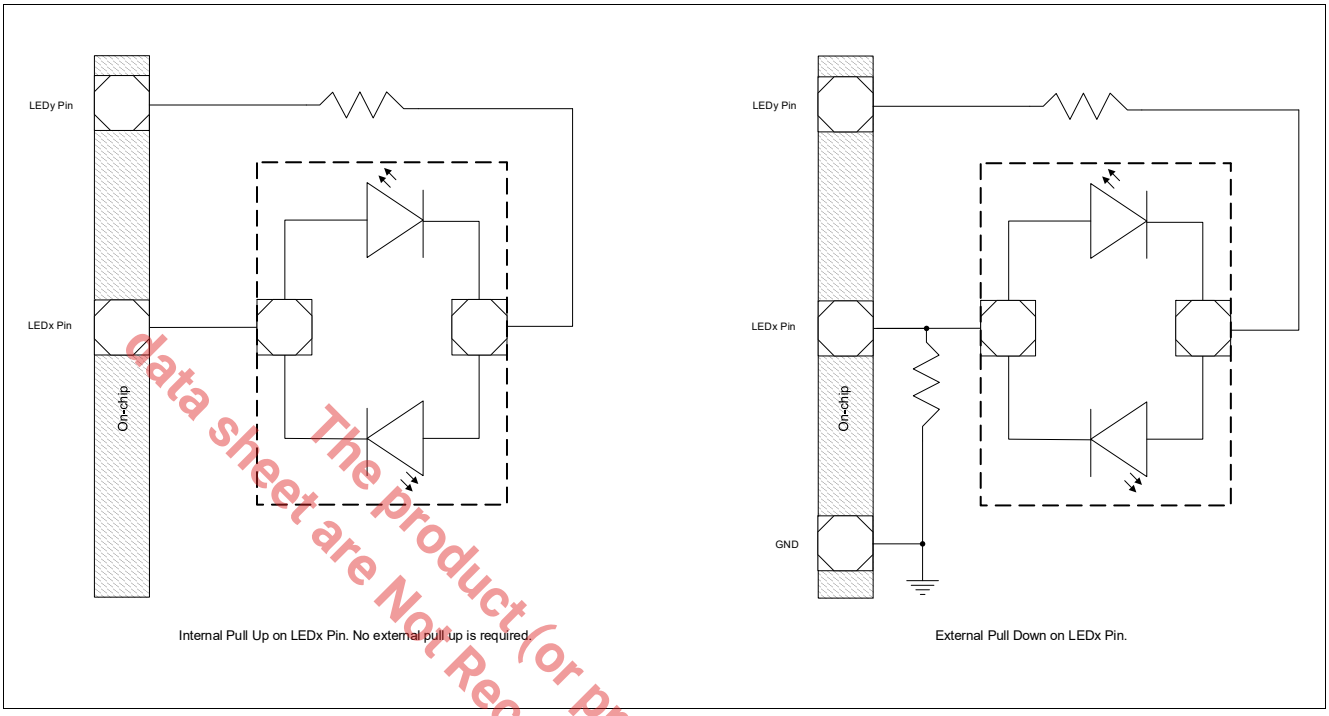



**Figure 11 Connection of a Dual Color LED and Configuring Pin Strap Value**

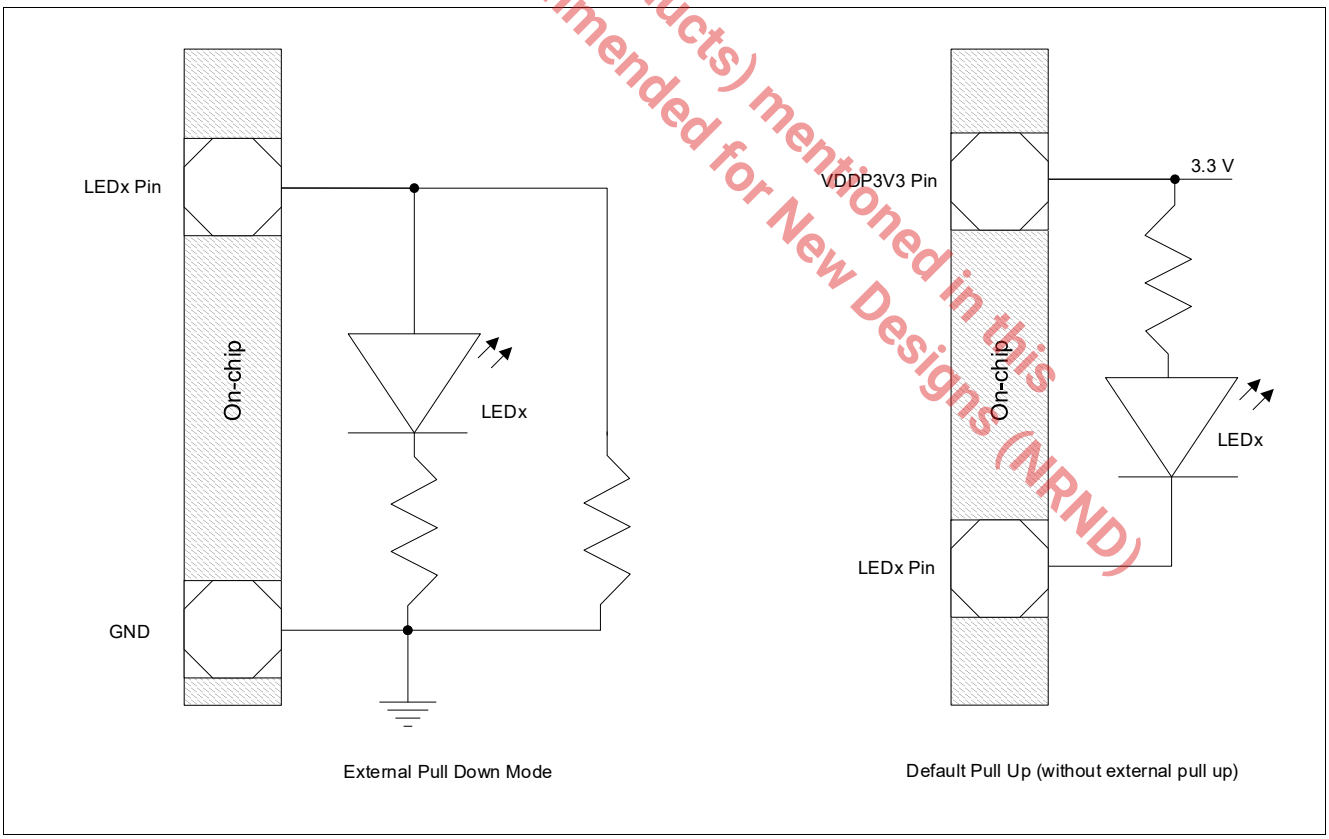



**Figure 12 Connection of a Single Color LED and Configuring Pin Strap Value**

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### 3.7.3 LED Brightness Control

There are two LED brightness modes configurable by the API for the MDIO-managed mode, or FCA [1] for the unmanaged mode, based on the system requirement.

- LED Brightness Level Maximum Mode
  Fixed level signal (no pulses) for maximum brightness, also available as a control signal for other purposes.
- LED Brightness Level Control Mode (Constant Mode)
  Allows the configuration of 16 levels of LED brightness. See **Brightness Control**.

#### Brightness Control

This block controls the brightness of the LED by controlling the time duration for which the LED is on/off. The persistence characteristic of the eye causes it to perceive this as LED brightness. When LED is off, the output is disabled. When the LED is on, the output is enabled. The brightness control affects the LED output enable directly.

Figure 13 shows the brightness control frequency is 81.25 Hz, where each period is divided into 64 slots.

In the LED brightness level maximum mode, the LED is enabled in all 64 slots, as shown in brightness level 0 which is the maximum brightness.

In the LED brightness level control mode, the LED is enabled for n consecutive slots, where n is determined by the configured brightness level. Figure 13 shows the brightness level in active low mode, whereby brightness level 15 is the minimum brightness.

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**Figure 13 LED Brightness Control by Controlling LED Output Enable/Disable**

## 3.8 Power Management

This section describes the power management functions of the MxL86280C integrated Ethernet PHY.

### 3.8.1 Power States

**Figure 14** illustrates the power states and transitions of each integrated Ethernet PHY.

In this state diagram, the (0.11) syntax corresponds to the value of bit 11 from register 0 in device 0, which is `STD_CTRL.PD`. This is the Power Down (PD) bit in `MDIO STD_CTRL`, described in **Chapter 4**. The STA is able to use this `STD_CTRL.PD` field to bring the physical interface into the **POWER DOWN State**.

The other states are automatically entered by the MxL86280C depending on the context, and following the EEE protocol. This is done without any intervention from the STA.

The Normal Link Pulse (NLP) and Fast Link Pulse (FLP) are received on the TPI from a link partner and used to wake up the MxL86280C and enter auto-negotiation.

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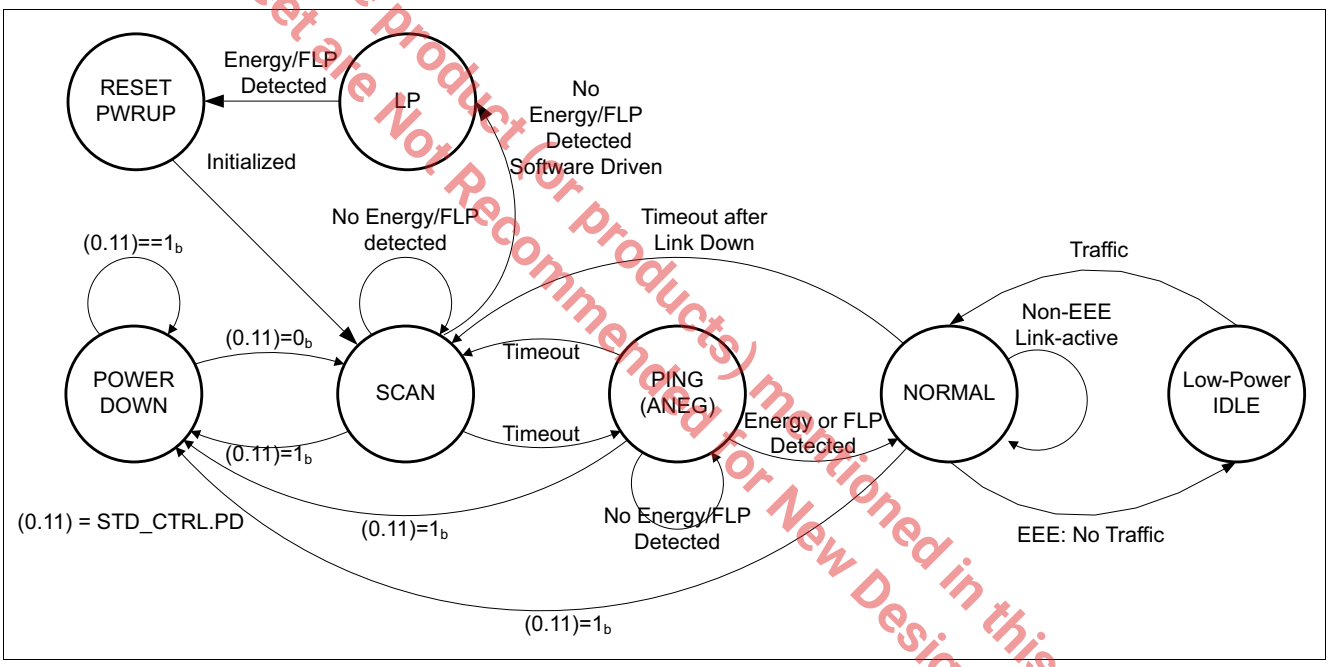



**Figure 14 State Diagram for Power Down State Management**

### 3.8.2 RESET PWRUP

The MxL86280C starts up in the RESET Power Up (PWRUP) state after either a hardware reset or power up.

After initialization, the PHYs always transition to the **SCAN (ANEG) State**.

### 3.8.3 POWER DOWN State

The **POWER DOWN State** is entered by setting the PD bit (0.11) of the MDIO standard register `STD_CTRL` to 1, regardless of the current state of the device. The **POWER DOWN State** corresponds to power down as specified in IEEE 802.3, Clause 22.2.4.1.5. Some signal processing blocks are stopped to save energy, but the MxL86280C still responds to MDIO messages.

Exiting the **POWER DOWN State** is triggered by setting the PD bit (0.11) of `STD_CTRL` to 0, which initiates a transition to the **SCAN (ANEG) State**.

### 3.8.4 SCAN (ANEG) State

The SCAN state differs from the **POWER DOWN State** in that the receiver periodically scans for signal energy or FLP bursts on the TPI. There is no transmission in this state. When an FLP burst is received, the MxL86280C enters the auto-negotiation protocol to exchange capabilities with the link partner and establish a data link in the **NORMAL State**.

### 3.8.5 PING (ANEG) State

The PING state is similar to the **SCAN (ANEG) State** except that the transceiver transmits an FLP burst onto the TPI for a programmable amount of time. This is used to wake potential link partners from the **POWER DOWN State**. This state corresponds to the state of ANEG described in Clause 28 of the IEEE standard **[2]**.

### 3.8.6 Low-Power State

The MxL86280C's Low-Power (LP) state is enabled by configuring the MDIO register `PHY_CTL2.LP`. The LP state is entered automatically when there is no Ethernet cable connected to the MxL86280C. The MxL86280C firmware detects this condition when no energy or Link Pulse is present on the TPI and enters the LP state. It is intended to set the MxL86280C into its maximum power saving state. In this state, most digital domains are in reset. Only a minimal amount of circuitry (analog/digital) operates to detect signal energy on the receiver of a TPI and trigger a wake-up.

When the port is in the LP state, the STAs do not have access to the corresponding MDIO/MMD registers.

The LP state is exited upon detection of signal energy on the twisted pair (either NLP or FLP). The port transitions to the **RESET PWRUP** state automatically. The STA host is also able to trigger an LP state exit by applying an API to wake up the specific port that entered the LP state.

It is possible for the STA host to be informed of the LP entry condition. By setting the `PHY_IMASK.LP` bit to ACTIVE, the STA requests the MDINT interrupt from the port when the entry conditions are met. **Figure 15** shows all the LP related control bits and communication mechanism between the STA and the MxL86280C.

It is possible for the STA host to be informed of the LP exit condition. By setting the `VSPEC1_IMASK.CDET` bit to ACTIVE, the STA requests the MDINT interrupt from the port when energy on the link is detected during auto-negotiation. Even when none of the ports are in the LP state, this interrupt is triggered whenever energy is first detected on the link. When the STA triggers the LP state exit via a wake-up request, and there is no energy on the link after the LP state exit, no interrupt is asserted.

***Attention: An active-high MDINT in push-pull mode (default is tristate mode) is not supported in the LP mode.***

***Attention: VSPEC1_IMASK.CDET is not supported in forced speed 10BASE-T/100BASE-TX mode. Auto-negotiation is required to support this feature.***

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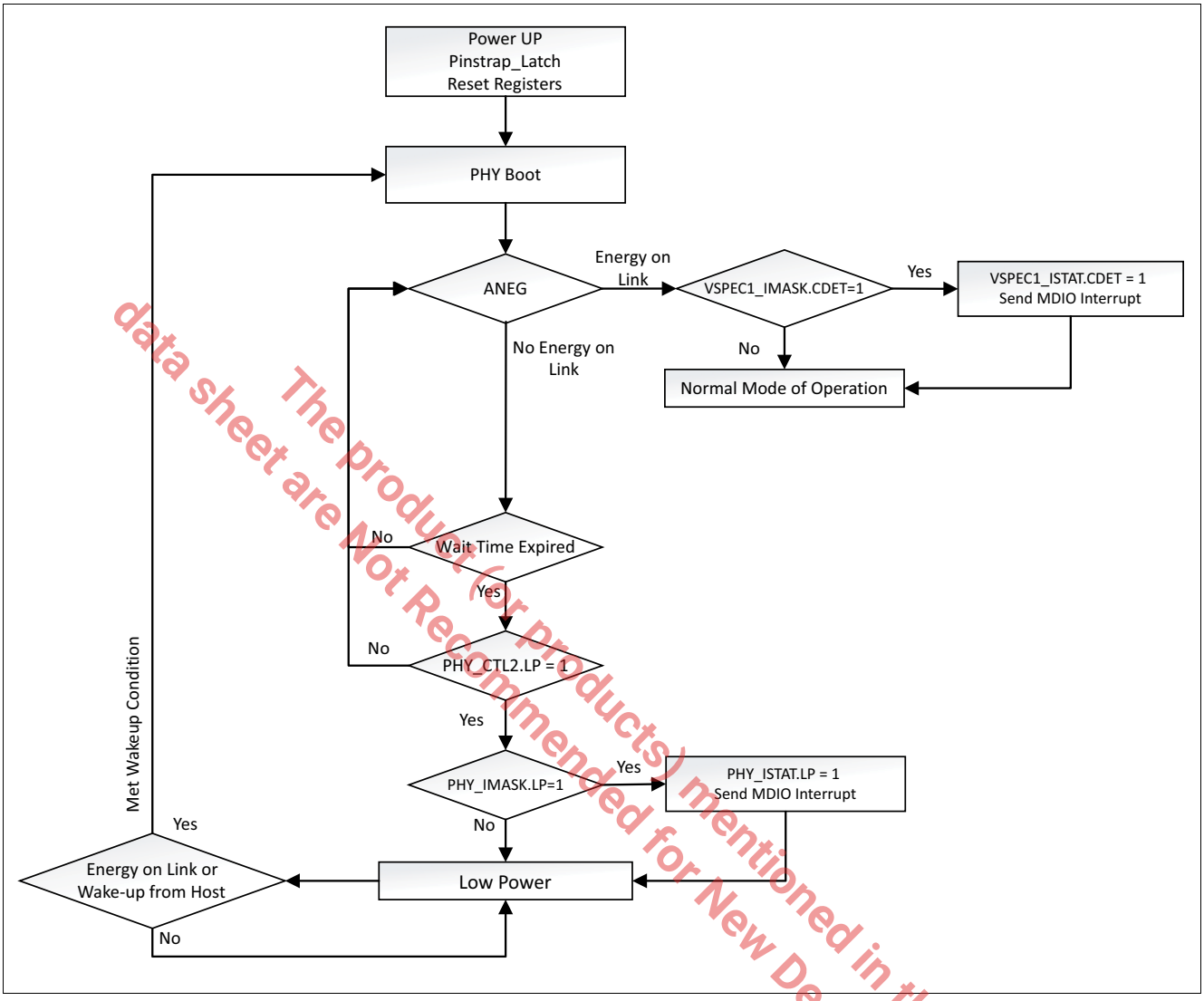



**Figure 15 Low Power Sequence**

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**Table 22 Low Power State Entry and Exit Sequence**

| Step | State | Remark |
|---|---|---|
| 1 | ACTIVE<br>The LP feature is enabled by setting `PHY_CTL2.LP` = 1 | Use the MDIO register PHY_CTL2.LP to enable or disable the LP feature. |
| 2 | ANEG, Ability Detect | The firmware detects no energy on the cable when no FLP is received for a long period of time. When the LP feature is not enabled, this time is fixed to between 6.4 and 9.6 seconds. When the LP feature is enabled, this time is configured using the `VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM` register.<br>Time in seconds = 4 x value programmed.<br>Default time is 4 seconds.<br>(`VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM` = 1). There is an initial time of between 2.4 and 5.6 seconds, which adds on to the programmed time. |
| 3 | LP Entry Timer | This time is configured with the `VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM` register.<br>The value is set in steps of 4 seconds. The default time is 4 seconds. |
| 4 | LP Entry | The MxL86280C saves MDIO LP persistent registers.<br>An interrupt is sent to indicate entry into the LP state. |
| 5 | LP State | Power consumption is saved in this state.<br>The MxL86280C listens to energy pulses from the link partner ANEG as a condition to trigger an exit from the LP state. Only a minimal amount of circuitry operates to detect signal energy on TPI and trigger a wake-up.<br>The port LEDs and MDIO interface are disabled. |
| 6 | LP Exit (Option 1)<br>Based on energy detected on the cable | The MxL86280C restores the configurations in the MDIO registers. An interrupt is sent to indicate an exit from the LP state. |
| 7 | LP Exit (Option 2)<br>Based on a wake-up request from the STA | The STA is able to request an LP exit by using a provided API. The MxL86280C restores the configurations in the MDIO registers. No interrupt is sent to notify LP exit. Not applicable if MxL86280C is not managed via MDIO. |
| 8 | ANEG, LINK-UP, and ACTIVE | The MxL86280C operates in normal power modes. |

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These are persistent MDIO registers saved and restored during LP entry-exit.

1. STD_CTRL.SSM
2. STD_CTRL.DPLX
3. STD_CTRL.ANEN
4. STD_CTRL.SSL
5. STD_AN_ADV.TAF
6. STD_AN_ADV.XNP
7. STD_GCTRL.MBTHD
8. STD_GCTRL.MBTFD
9. STD_GCTRL.MSPT
10. STD_GCTRL.MS
11. STD_GCTRL.MSEN
12. PHY_IMASK
13. PHY_CTL1.AMDIX
14. PHY_CTL1.MDIAB
15. PHY_CTL1.MDICD
16. PHY_CTL1.POLA
17. PHY_CTL1.POLB
18. PHY_CTL1.POLC
19. PHY_CTL1.POLD
20. PHY_CTL2.LPI
21. PHY_CTL2.ANPD
22. PHY_CTL2.PSCL
23. PHY_CTL2.LP
24. PHY_CTL2.STICKY
25. PHY_CTL2.SDETP
26. PHY_LED
27. ANEG_CTRL.ANEG_ENAB
28. ANEG_MGBT_AN_CTRL.LDL
29. ANEG_MGBT_AN_CTRL.FR
30. ANEG_MGBT_AN_CTRL.FR2G5BT
31. ANEG_MGBT_AN_CTRL.AB2G5BT
32. ANEG_MGBT_AN_CTRL.PT
33. ANEG_MGBT_AN_CTRL.MS_MAN_EN
34. ANEG_MGBT_AN_CTRL.MSCV
35. ANEG_EEE_AN_ADV1.EEE_100BTX
36. ANEG_EEE_AN_ADV1.EEE_1000BT
37. ANEG_EEE_AN_ADV2.EEE2G5
38. ANEG_MGBT_AN_CTRL2.THPBYP2G5
39. VSPEC1_NBT_DS_CTRL.NO_NRG_RST
40. VSPEC1_NBT_DS_CTRL.DOWNSHIFTEN
41. VSPEC1_NBT_DS_CTRL.DOWNSHIFT_THR
42. VSPEC1_NBT_DS_CTRL.NRG_RST_CNT
43. VSPEC1_NBT_DS_CTRL.FORCE_RST
44. VSPEC1_LED0
45. VSPEC1_LED1
46. VSPEC1_LED2
47. VSPEC1_PM_CTRL
48. VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM
49. VSPEC1_IMASK
50. VSPEC1_FRCTL.CAP_EXT

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51. VSPEC1_FRCTL.CAP_TXDIS
52. VSPEC1_FRCTL.CAP_THPBYP
53. VSPEC1_FRCTL.CAP_CISCO
54. VSPEC1_FRCTL.CAP_IEEE
55. VSPEC1_FRCTL.MAX_FR_RETRY
56. VSPEC2_WOL_CTRL
57. VPSPEC2_WOL_AD01
58. VPSPEC2_WOL_AD23
59. VPSPEC2_WOL_AD45
60. VPSPEC2_WOL_PW01
61. VPSPEC2_WOL_PW23
62. VPSPEC2_WOL_PW45

### 3.8.7 NORMAL State

The NORMAL state is used to establish and maintain a link connection. When a connection is dropped, the MxL86280C moves back into the **SCAN (ANEG) State**.

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### 3.8.8 Low Power IDLE State - Energy-Efficient Ethernet

The IEEE 802.3 standard [2] describes the EEE operation supported by the MxL86280C in the various speeds of 100BASE-TX, 1000BASE-T, and 2.5GBASE-T. The general idea of EEE is to save power during periods of low link utilization. Instead of sending active idle data, the transmitters are switched off for a short period of time. This is called the quiet period. The link is kept active by means of a frequent refresh cycle initiated by the PHY itself while in the low power state. This sequence is repeated until a wake request is generated by one of the link partner MACs. The MxL86280C follows the IEEE 802.3 standard regarding EEE. Figure 16 illustrates the principle. This state is entered automatically when the low power idle conditions are met.

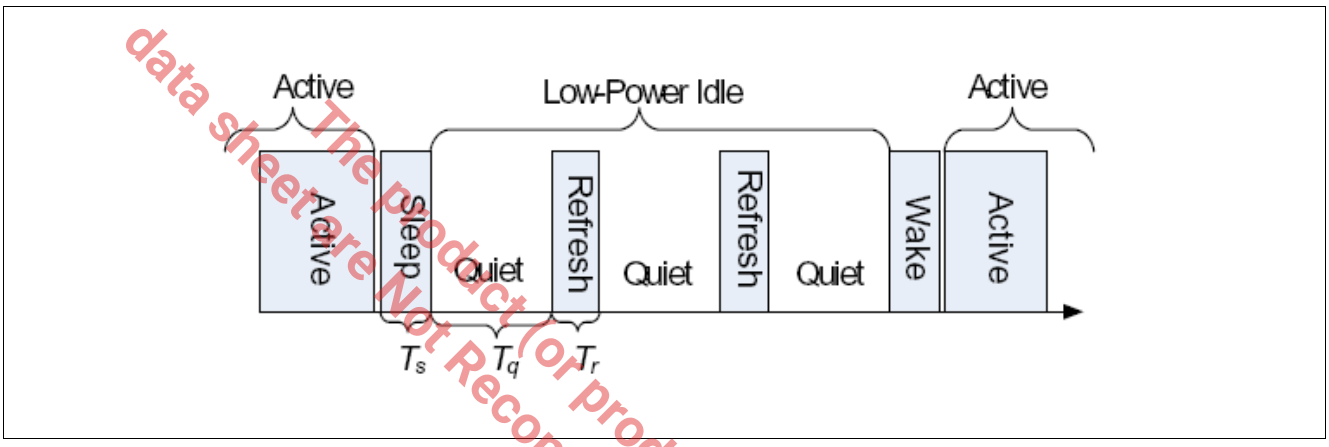



**Figure 16 EEE Low Power Idle Sequence**

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## 3.9 Firmware Upgrade

The MxL86280C provides a Firmware Upgrade feature that allows feature and functional enhancements of the MxL86280C in the field.
It is possible to download a new firmware image via the MxL86280C's **MDIO Slave Interface** to a serial flash memory device connected to the MxL86280C's QSPI. The MxL86280C is then able to fetch the upgraded firmware from the flash memory after a reboot.

For Security Development Lifecycle (SDL) **[5]** reasons, the MxL86280C only accepts firmware images electronically signed by MaxLinear. When authentication of the flash image by the MxL86280C fails, or the download of the image is aborted or fails, the MxL86280C resets and wait for a new image to be downloaded.

The supported options for upgrading the firmware image are:

- The firmware is upgradeable over the MDIO slave interface to the flash memory device for MDIO-managed mode.
- In addition firmware download into "empty" flash is supported over MDIO slave interface.

***Attention: The MDIO slave interface for firmware download or upgrade supports IEEE 802.3 Clause 22 only.***

***Attention: The MDIO address for firmware download or upgrade to flash is defined by the pin strapping in Table 15 with the lowest three bits equal to 0.***

***Attention: After the firmware upgrade to the flash memory is completed, the MxL86280C must be rebooted such that the new image is authenticated. The same requirement also applies to flash memory devices that are programmed directly by customers, which do not use the firmware upgrade procedure provided in this section.***

The procedure to download firmware over the MDIO slave interface is documented in **[1]**. It provides information on the update/download process and which actions are required in the external processor application.

Security feature to prevent flash memory wear-out due to frequent updates (flash anti-wear out) is not supported within the MxL86280C. When the system to which the MxL86280C is attached mandates such features, they must be supported by the system itself. Flash memory components typically support a minimum of 100,000 erase/program cycles, so flash wear-out is unlikely. However, ensuring a minimum interval between flash updates decreases the likelihood of wear-out. An interval of one hour sets the minimum time before wear-out to longer than 11 years. The system is also expected to ensures that the firmware is only installed when a new firmware is available and does not attempt to install a new firmware after every reboot.

Security feature to prevent rollback of the image to a previous version (anti-rollback) is supported within the MxL86280C. The MxL86280C verifies that the new firmware has a higher or same security version number (SVN) than the previously installed firmware before executing it. If this step fails due to the firmware SVN being a lower version, the MxL86280C resets itself and waits for the host SoC to download a new image to the flash memory over the MDIO slave interface. If the system does not desire to have this anti-rollback feature, MaxLinear will deliver firmware images with fixed SVN, such that the security check will always pass.

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## 3.10 Switch Fabric Functional Description

This section provides a detailed functional description of the Switch Fabric.

### 3.10.1 Overview

The Switch Fabric is responsible for classifying, storing, and forwarding multiple data packets. It consists of storage buffer, packet queuing, and packet classification units. Ingress data received on one of the interfaces is classified and placed in the appropriate QoS queue in the shared storage buffer. Ingress policing and access control rules are applied to the received traffic and packets not compliant to the rules are discarded. Before a packet is fetched from the shared memory and transmitted on one or several of the egress interfaces, it is subjected to egress scheduling, rate shaping, and modification.

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#### 3.10.1.1 Packet Flow

Figure 17 describes a packet data flow through various stages of the switch. The flow starts on the top right corner.

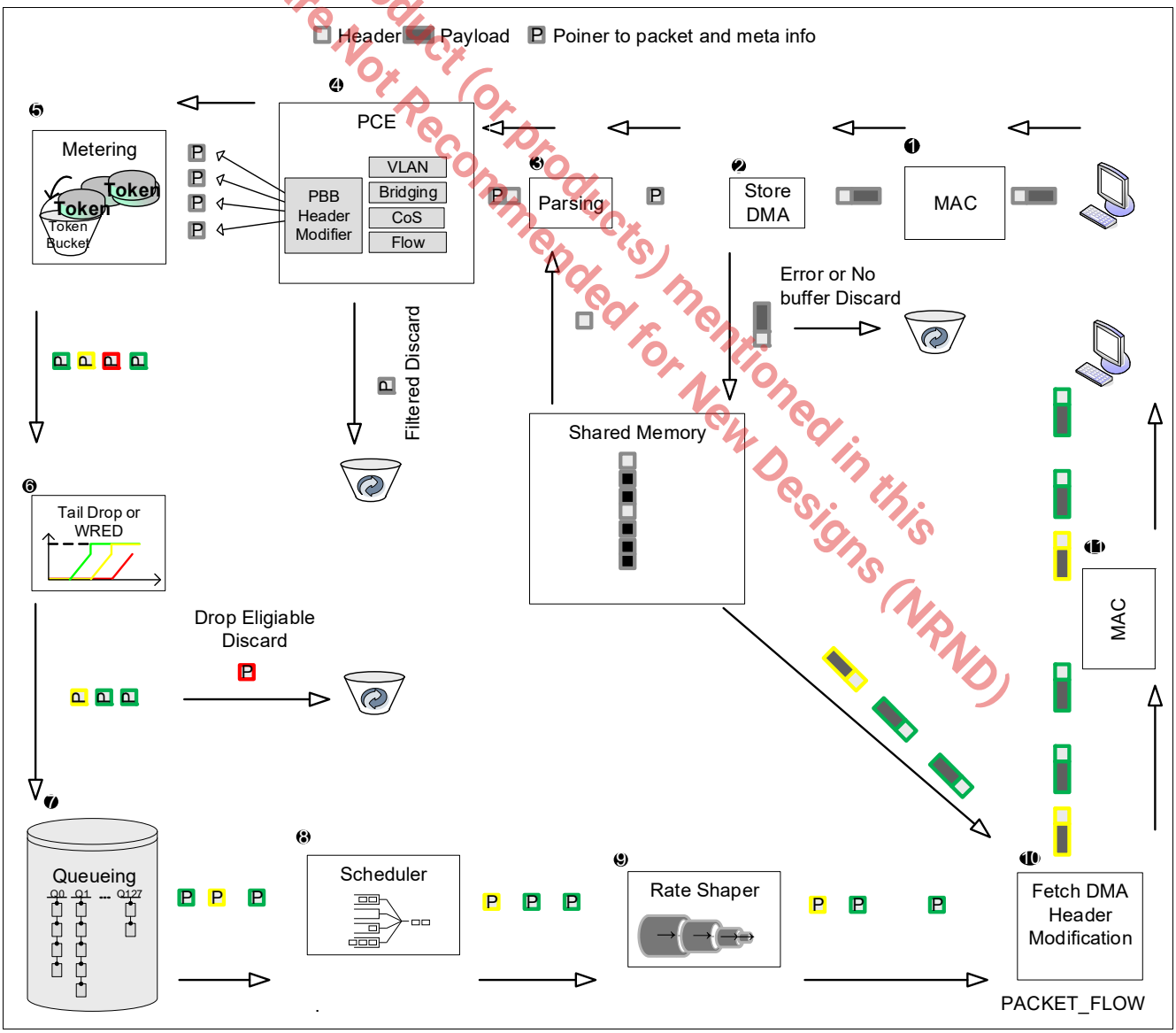



**Figure 17 Packet Flow Diagram**

The packet received on the ingress interface is first stripped from the Ethernet Preamble and checked for correct CRC. The behavior when a reception error occurs is programmable. This determines whether the packet is discarded or not.

The received packet is classified in the Packet Classification Engine (PCE). The packet is assigned to one or several appropriate QoS queues, such as broadcast or multicast. The packet classification filtering determines whether the received packet is discarded.

Prior to accepting it to a certain queue, the packet is subject to metering and Weighted Random Early Detection (WRED) functions. Packets marked as non-conforming by the metering engine might be discarded by the WRED algorithm based on the configurable drop precedence.

The scheduling function, Strict Priority (SP) and/or Deficit Weighted Round Robin (DWRR), determines which queue is allowed to emit a packet. Prior to transmission on the egress side, the packet is subject to Rate Shaping.

Packets scheduled for transmission are subject to egress specific header modification, such as, MAC address swap, special tag modification, OAM timer stamp modification, OAM packet counter field modification, DSCP and IP checksum modification, or VLAN tag modification.

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### 3.10.1.2 Switch Fabric Control

For applications with MDIO-managed mode of operation, the switch fabric on the MxL86280C is controlled by a switch driver executed on the Host SoC. The control interface is the slave MDIO interface. The same interface is used to configure the PHY MDIO and MMD registers using the switch driver. The switch driver is part of the Host SoC API software documented in the MxL86280C API.

In unmanaged mode, the switch fabric is pre-configured using the FCA, documented in [1].

### 3.10.2 Ethernet Bridging

Ethernet bridging, or switching, is the primary task of the switch macro. The frames received on one of the ingress ports must be forwarded to the appropriate destination port. The destination port is determined by a lookup in the MAC bridging table. The MAC bridging table can be populated by software, using static entries, or entries can automatically be learned by the hardware learning function. The entries learned by the hardware can age out after a configurable time and are deleted from the MAC bridging table.

#### 3.10.2.1 Parsing

The switch macro features a parser realized as a microcoded engine. This allows a flexible adaptation to any future protocol changes. The parser microcode evaluates the frame header and is capable of extracting all relevant information up to the layer 4 protocol from the frame. The microcode must be loaded otherwise only the MAC destination and MAC source address is extracted from the frame.

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#### 3.10.2.2 MAC Bridging Table

The MAC bridging table is realized as a hash table with four collision buckets and holds these components.

- Lookup key
  - MAC address
  - Forwarding identifier (FID)
  - VLAN tag
- Control information
  - Static indication
  - Aging timer
  - Changed indication
- Result
  - Port or port map
  - Sub-interface ID
  - Associated MAC address

A port map is a bitmap where each bit represents a single port. The port map allows to send the frame to multiple destination ports and is available for static entries only.

The switch macro supports learning, either Shared VLAN Learning (SVL), or Independent VLAN Learning (IVL). It is achieved by mapping the default customer VLAN ID or a flow to an FID used as part of the lookup key, together with the MAC address, for the MAC bridging table lookup. By default, the FID value is zero and all entries belong to SVL.

Entries are entered automatically by hardware using dynamic MAC address learning, or entered by software via manual learning. The software writes static entries into the MAC bridge table, but it is also possible to write dynamic entries which are subject to aging.

The MAC bridge table is able to hold unicast, multicast, or broadcast addresses. The table entries containing multiple egress ports as a destination are entered only as static entries by appropriate management action.

#### 3.10.2.3 Layer 2 Security

The supported layer 2 security features comprise:

- IEEE 802.1X
- MAC learning limitation, allows only a limited number of MAC addresses to be learned on a port.
- MAC port locking and MAC spoofing detection, allows only frames with a previously learned MAC and PortID association.
- MAC table freeze, allows only frames with previously learned MAC addresses.
- Source MAC address filtering and destination MAC address filtering, filters user defined MAC addresses.

### 3.10.2.4 Spanning Tree Protocol Support

The switch macro supports the port states required for the Spanning Tree Protocol (STP) functionality. 16 spanning tree instances per port are supported. Each spanning tree instance is associated with least significant 4 bits of the FID and a port. The port state programmed for one FID does not have effect on the behavior of another FID of the same port.

These states are supported per STP instance:

- **Disabled**
  When disabled, all ingress frames are dropped, the source MAC address is not learned. All egress frames are discarded.
- **Blocking/Listening**
  In this state, all regular ingress and egress traffic is discarded. It is possible for Bridge Protocol Data Unit (BPDU) frames to ignore the port state and be forwarded to the STP managing entity. The source MAC address is not learned in this state.
- **Learning**
  In this state, all regular ingress and egress traffic is discarded. The source MAC address is learned in this state. It is possible for BPDU frames to ignore the port state and be forwarded to the STP managing entity.
- **Forwarding**
  Normal operation. Ingress and egress traffic is enabled for all frames.

### 3.10.2.5 Flow Control Function

To prevent buffer congestion and packet drop, the switch macro supports a flow control mechanism. In full duplex operation the sender is notified to start or stop the transmission via a PAUSE frame based on the IEEE 802.3x standard or a priority pause frame based on the IEEE 802.1Qbb standard. The switch macro is able to transmit or receive and react accordingly to 802.3x/802.1Qbb flow control frames. In half duplex operation, the switch macro supports a back pressure mechanism, specifically, a jam pattern is transmitted on the port forcing a collision. It is possible to enable or disable flow control on a per-port basis. When enabled, it depends on the auto-negotiation result of the attached PHY.

This list shows how flow control is applied:

- **Global Flow Control**
  Flow control is activated when the global buffer congestion level exceeds a programmable global threshold and is deactivated when the global buffer congestion level is below a programmable global threshold. Flow control applies to all enabled ports.
- **Ingress Port Congestion-Based Flow Control**
  Flow control is activated when the ingress port local buffer congestion level exceeds a programmable local threshold and deactivated when the local buffer congestion level drops below a programmable local threshold. Flow control applies to each port individually.
- **Ingress Port Metering-Based Flow Control**
  When the global buffer filling level exceeds a programmable global threshold, flow control is activated on the port that exceed the configured ingress rate. When the global buffer filling level drops below a programmable threshold or the traffic rate is reduced below the configured rate, flow control is deactivated on the port. See Section 3.10.5.4 for details regarding the metering based flow control and metering assignment.

### 3.10.2.6 Port Trunking Functions

The switch macro supports link aggregation according to IEEE 802.3ad. Link aggregation (LAG), also called port trunking, allows to combine multiple physical ports to a trunk for high bandwidth inter-switch links. It is possible to combine 64 physical ports to from a trunk, which is also known as a LAG group. There is no restriction on the port sequence or combination which are used for the trunk. When one link is broken or disabled for any reason, such as being powered off, the software or firmware detects and automatically reconfigures the mapping. It is not

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possible for hardware to automatically switch to other working links. Up to 32 LAG groups are supported. The number of physical ports in a LAG group is not required to be a power of 2.

**Figure 18** shows how packets received from all ports in a trunk are aggregated and how the packets are distributed to all ports in a trunk.

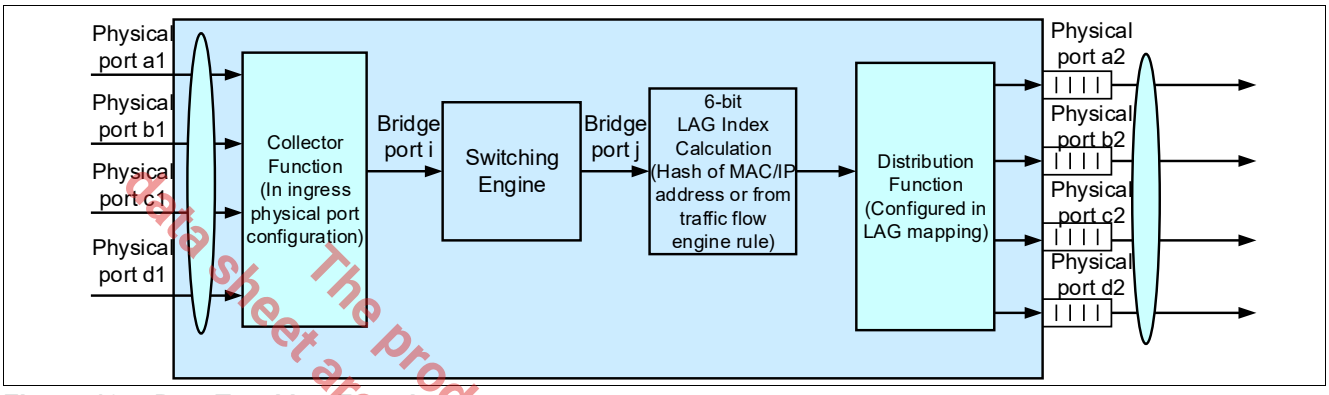



**Figure 18 Port Trunking Function**

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### 3.10.3 VLAN Functions

This section describes Virtual Local Area Network (VLAN) bridging functionality.

A VLAN is a grouping of network devices logically segmented by functions or applications without regard to the physical location of the devices. Ports in a VLAN share broadcast traffic and belong to the same broadcast domain. Any traffic in one VLAN is by definition not transmitted outside of that VLAN. However, there are exceptions to this general rule which are configurable to cover certain system requirements.

This section provides more details regarding VLAN functionality.

#### 3.10.3.1 VLAN Association

The VLAN classification function associates each packet received on the ingress side with a specific VLAN group. VLAN association is performed in one of two ways:

- **Implicit VLAN Association**
  The VLAN group is based on packet attributes. When the association is based on the ingress port it is called port-based VLAN. When the association is based on the MAC address, it is referred to as a MAC-based VLAN. When the association is based on selected packet header fields, such as Ethernet type, IP protocol, IP address subnet, or MAC address, it is referred to as a protocol-based VLAN.
- **Explicit VLAN Association**
  The VLAN group information is carried in a VLAN tag in the Ethernet header of the received packet. This association is referred to as a tag-based VLAN.

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#### 3.10.3.2 VLAN QinQ

IEEE 802.1QinQ is an Ethernet networking standard formally known as IEEE 802.1ad and is defined in the amendment IEEE 802.1Q-1998. It is for Ethernet frame formats. The technique is also known as provider bridging, stacked VLANs, QinQ, or Q-in-Q. The idea is to provide, for example, the possibility for customers to run their own VLANs inside service provider's provided VLAN. This allows a service provider to configure a single VLAN for a customer and allowing each customer to treat that VLAN as if it were a trunk.

The original 802.1Q specification allows a single VLAN header to be inserted into an Ethernet frame. QinQ allows multiple VLAN headers to be inserted into a single frame.

In this context, a QinQ frame is a frame that has two VLAN 802.1Q headers, and is referred to as a being double-tagged. A tag stack creates a mechanism for internet service providers to encapsulate customer-tagged 802.1Q traffic with service provider’s tag. The final frame is a QinQ frame.

A Service VLAN Tag (STAG) frame is identified by a Tag Protocol ID (TPID), which is typically $88A8_H$, but is programmable, and is followed by two bytes of the Tag Control Information (TCI) field. The TCI field consists of a 3-bit Priority Code Point (PCP) field, a 1-bit Drop Eligible Indicator (DEI) field, and a 12-bit VLAN Identifier (VID) field.

A Customer VLAN Tag (CTAG) frame is identified by a TPID, typically $8100_H$, but is programmable, and is followed by two bytes of the TCI field. The TCI field consists of a 3-bit PCP field, a 1-bit DEI field, and a 12-bit VID field.

VLAN QinQ is supported with the extended VLAN tagging operation.

#### 3.10.3.3 Extended VLAN Tagging Operation

Extended VLAN tagging operation is supported with a 1K entry table. Both symmetrical and asymmetrical ingress and egress tagging is supported, whereby the start and the end entry index are programmable per ingress port and per egress port independently. It is possible to cascade the ingress and egress extended VLAN tagging operation.

There are two parts in each entry: the filtering pattern and the action. The filtering pattern includes VLAN priority, VLAN ID, TPID/DEI of both STAG and CTAG and the Ethertype. It is configurable to base on the intermediate

VLAN tags, after modification in the previous processing stage, or the original ingress VLAN tags, before any modification, per entry.

The actions of the tagging operation corresponding to each matched rule includes the discard/forwarding action, STAG and CTAG removal/insertion/replacement, DSCP remarking, traffic class assignment, bridge port reassignment, metering assignment, mirroring enable/disable, loop-back enable with DA/SA swap.

It is only possible to insert, remove, or replace two VLAN tags. If both an ingress extended VLAN tagging operation and an egress extended VLAN tagging operation are enabled, any configuration which requires the insertion/removal/replace of more than two VLAN tags is illegal.

Discarded packets by ingress extended VLAN tagging operation are trappable by traffic flow classification engine for forwarding. When cross-VLAN is enabled, discard actions by the extended VLAN tagging operation are ignored.

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### 3.10.3.4 VLAN Filtering

It is possible to forward or discard a received frame based on the VLAN group configuration and configured port attributes. VLAN filtering is based on the STAG VLAN TCI, after it has been modified in a previous processing stage. The filtering is applicable to all ingress ports, after the ingress extended VLAN tagging operation, and egress ports, before egress extended VLAN tagging operation. Both symmetrical and asymmetrical VLAN filtering are supported.

The VLAN TCI field comprises the VLAN ID, PCP and DEI field. These VLAN filtering mask options are supported in ingress and egress port configuration:

- **VID-Only Mode**
  In VID-only mode, the VLAN ID field is used for VLAN filtering lookup.
- **PCP-Only Mode**
  In PCP-only mode, the PCP field is used for VLAN filtering lookup.
- **TCI Mode**
  In TCI mode, all 16-bit TCI is used for VLAN filtering lookup.

It is possible to configure the VLAN rules to discard or forward VLAN-tagged traffic which does not match any of the three filtering rules. For VLAN untagged traffic, it can be configured to be discarded or forwarded.

It is possible to configure each ingress port to filter according to a list of different TCI or mask patterns. Each egress port supports up to 2 such lists. These lists are sharable between ports and contain up to 1,000 TCI or mask patterns.

### 3.10.3.5 VLAN Transparent Mode

VLAN transparent mode is configurable per ingress port.

If VLAN transparent mode is enabled, VLAN tags at ingress are treated as part of the payload and the packets are considered as untagged.

Several exceptions apply to VLAN transparent mode, they are:

- **Traffic Flow Classification - Ingress VLAN ID**
  Transparent mode is ignored when the pattern field of a VLAN is based on the ingress VLAN ID. The ingress-tagged packets are still considered as tagged packets regardless of transparent mode setting.
- **Traffic Flow Classification - STAG PCP+DEI and CTAG PCP+DEI**
  Transparent mode is ignored when STAG PCP+DEI and CTAG PCP+DEI is based on ingress packets. The ingress-tagged packets are still considered as tagged packets regardless of the transparent mode setting.
- **Traffic Class Mapping**
  PCP+DEI in ingress STAG and PCP in ingress CTAG are used for traffic class mapping regardless of transparent mode setting.

### 3.10.3.6 Cross-VLAN Functionality

Ethernet frames that are classified as cross-VLAN cross the VLAN boundaries. They ignore any of the VLAN filtering modes for the ingress or egress ports, and any discard action in the extended VLAN tagging operation for the ingress or egress ports.

Cross-VLAN classification is performed as part of the traffic flow classification function.

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### 3.10.4 Multicast Forwarding Functions

Multicast forwarding is a method of forwarding Ethernet frames or IP datagrams to a group of receivers. A basic Ethernet switch floods all received multicast frames to all output ports even when no host on a port is interested in that particular multicast stream. This waste of bandwidth is avoided by the sophisticated multicast handling of the switch macro which allows the forwarding of multicast frames based on layer 2 or layer 3 addresses to dedicated ports. In addition, the switch macro is able to learn layer 3 multicast group addresses via IGMPv1/2/3 and MLDv1/2 snooping.

#### 3.10.4.1 Layer 2 Multicast Forwarding

The layer 2 multicast forwarding function deals with multicast frame forwarding based on the Ethernet MAC address. The destination port map is looked up in the bridging table. The multicast addresses are not added to the bridging table by automatic learning function and must be configured manually, by an appropriate management action. The associated port map contains all the relevant port members. When the destination MAC address of the received frame matches the entry in the bridging table and the forwarding mode is layer 2 only or there was no match in the layer 3 multicast table, or the packet is non-IP multicast, the frame is delivered to all the destinations specified in the associated port map.

#### 3.10.4.2 Layer 3 Multicast Forwarding

The layer 3 multicast function deals with multicast frame forwarding based on the IPv4 or IPv6 network address. The destination port map is looked up in the layer 3 multicast table.

The lookup in the multicast table is performed using the destination IPv4/IPv6 address, the source IPv4/IPv6 address, and FID. The addresses in the table are added by an appropriate management action.

#### 3.10.4.3 IGMP and MLD Snooping

The switch macro supports Internet Group Management Protocol (IGMP) and Multicast Listener Discovery (MLD) snooping. IGMP/MLD snooping is designed to prevent hosts on a local network from receiving traffic for a multicast group they have not explicitly joined. It provides a mechanism to prune multicast traffic from links that do not contain a multicast listener, which is an IGMP/MLD group member. IGMP/MLD snooping requires the switch macro to examine, or snoop, some layer 3 information in the IGMP/MLD packets sent between the hosts and the router. In addition, adjacent routers also use these protocols to communicate and share routing information. It is also possible to snoop the exchange information to identify the multicast router port.

The switch macro supports software-based IGMP/MLD snooping mode for the IGMPv1/2/3 or MLDv1/2 protocols. In this mode, specific IGMP/MLD reports can be intercepted by the switch and delivered to the CPU or network processor port. The reports are analyzed by the CPU and the layer 3 multicast table is populated by the software with appropriate source or destination addresses.

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### 3.10.5 Quality of Service Functions

The switch macro provides extensive support for Quality of Service functionality. Traffic class assignment based on multiple flow parameters, ingress traffic policing, multiple egress queues per port with strict or WFQ scheduling, traffic shaping, and Weighted Random Early Detection (WRED) functions are supported.

This section describes the QoS functions supported by the switch.

#### 3.10.5.1 Class of Service Assignment

The switch macro supports classification of the incoming traffic into traffic classes or classes of service (CoS). It is possible to manage each traffic class differently, be it remarked, policed, or shaped, ensuring preferential treatment for higher-priority traffic on the network. Supported RFCs include RFC2474 and RFC2597.

Up to 16 different traffic classes are supported and mapped individually to appropriate QoS queue. See **Section 3.10.5.3** for more details regarding queue mapping.

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#### 3.10.5.2 Remarking Function

The switch macro supports the remarking of the Differentiated Services Code Point (DSCP), the (re)generation of the STAG PCP&DEI, and the (re)generation of the CTAG PCP&DEI in the egress frame. The modification of the code points in the outgoing packets is based on both traffic class and egress port. The switch macro provides a dedicated mapping table to assign the new DSCP, CTAG PCP&DEI, and STAG PCP&DEI according to traffic class, as well as the egress port. **Figure 19** shows how to remark DSCP, including drop precedence, CTAG PCP, CTAG DEI, STAG PCP, and STAG DEI based on any of the class of service assignment parameters.

Remarking is enabled on a per ingress port basis. It is also possible to disable remarking on a per egress port and per code point basis. In addition, the traffic flow table allows disabling remarking explicitly for certain flows.

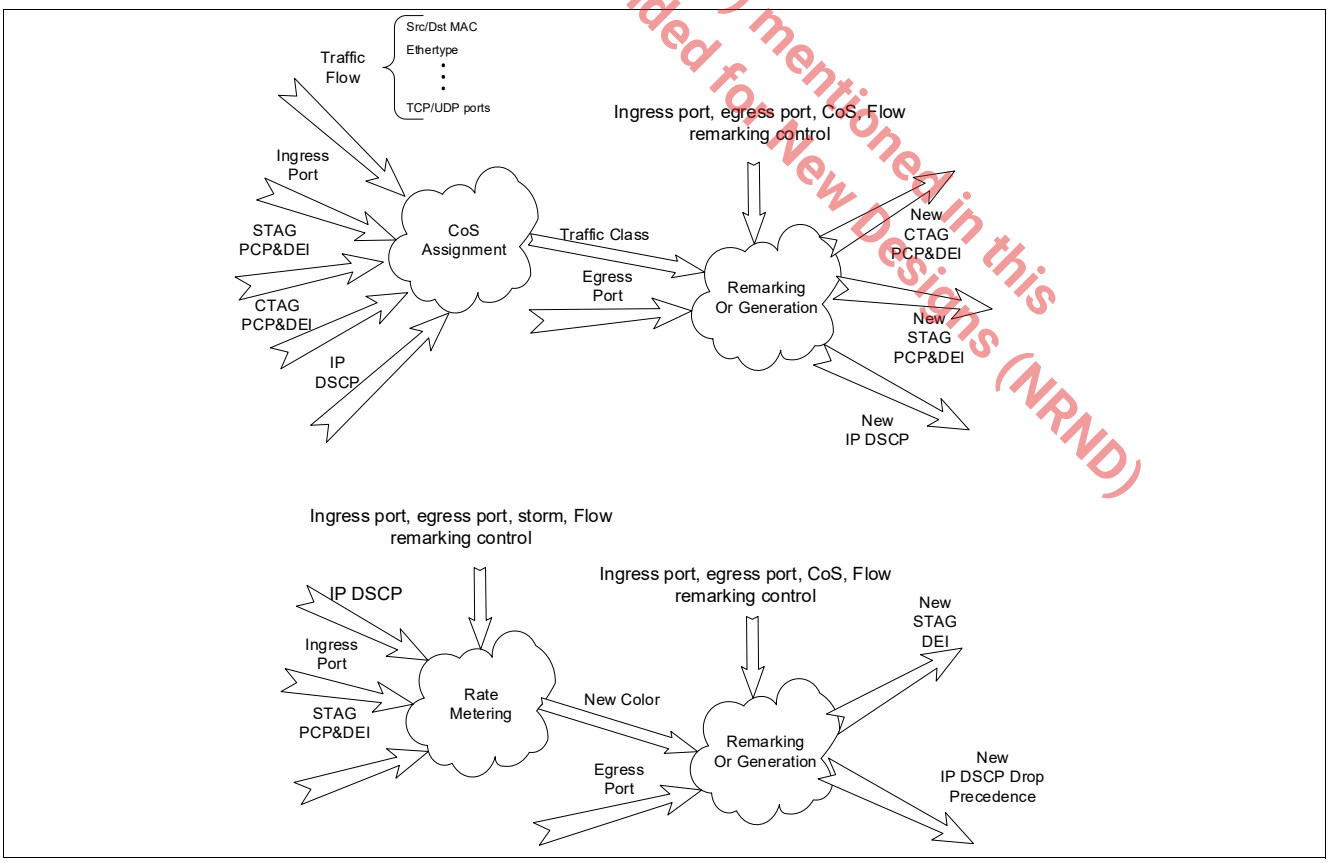



**Figure 19 PCP/DSCP/DEI Remarking**

### 3.10.5.3 Queue Mapping

The switch macro supports 128 egress QoS queues which are flexibly assignable to egress ports and traffic classes. For each egress physical port, up to 16 priority queues are assignable. This section provides more details about the queue mapping functionality.

#### Queue to Port Mapping

By default, each egress port has 8 QoS queues. Depending upon application, it might be desirable to have a different number of QoS queues on specific ports. The switch macro supports flexible queue to port mapping, assuming that the queues assigned to one egress physical port are consecutive and the total number of queues per port do not exceed 16. This way the default configuration can be changed so that one port, for example, contains 16 queues.

In addition, an active port must have at least one queue and can have maximum 16 queues assigned to it.

#### Port, Traffic Class to Queue Mapping

Incoming frames are being stored in the appropriate queues based on the egress port and the traffic class assignment. The mapping of the traffic class to queue is specified in a dedicated queue mapping table per egress port. The mapping of the traffic classes to queues is related to the number of the queues available on a certain port. For example, on one port, four traffic classes are mappable to four different queues, while on another port, all four traffic classes are mappable to one single queue.

### 3.10.5.4 Rate Metering

The switch macro supports 128 instances of a Two Rate Three Color Marker (trTCM) rate metering. Each marker or meter measures the rate of a packet stream and marks the packets as green, yellow, or red. When there is no metering instance assigned to a traffic stream, the stream is considered to be green and in color-blind mode. In color-aware mode, the stream is colored based on the drop precedence encoded in the frame.

It is possible to use the color markings later for policing in the active congestion management function, see Section 3.10.5.7 for details. In addition, the markings are usable to remark the drop precedence of the outgoing packet in the DSCP and STAG DEI.

The supported metering algorithm in Single Rate Three Color Marker (srTCM) is defined in RFC2697. The supported metering algorithm in trTCM are the non-coupling mode as defined in RFC4115 and the coupling mode as defined in the Metro Ethernet Forum (MEF). It is only possible to assign a single meter instance to measure the rate of a traffic flow.

#### Critical Frames

Frames are classified as critical based on a rule configured in the traffic flow table. Critical frames bypass the metering instance and do not trigger the active congestion management function.

#### Color-aware and Color-blind Modes

The switch macro supports color-awareness modes which are configurable per ingress port. In color-aware mode, the meter assumes that some preceding entity has pre-colored the incoming packet stream so that each packet is either green, yellow, or red. The ingress color of the incoming frame is based on either DSCP value or STAG PCP&DEI value. It is retrieved from the appropriate DSCP mapping table or STAG PCP&DEI mapping table. Non-IP and non-STAG packets are treated as pre-colored to green.

In color-blind mode, all packets are treated as green.

#### DSCP Drop Precedence Remarking

DSCP drop precedence remarking is enablable in both the ingress port configuration and the egress port configuration by replacing the lower three bits of the received DSCP field with the value of appropriate color

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decided by the metering instance for the received packet. The mapping of the color to the lower three bits of the DSCP is configurable per egress port. See **Section 3.10.5.2** for details.

#### DEI (Re)generation

DEI regeneration is enabled by both ingress port and egress port configuration to reflect the metering result by setting the STAG DEI field of the packet with the value of appropriate color decided by the metering instance for the received packet. The mapping of the color to the DEI is configured per egress port. See **Section 3.10.5.2** for details.

#### Metering-based Flow Control

When a metering instance is assigned to an ingress port, the conformance rate of the port is usable for triggering flow control. See **Section 3.10.2.5** for details.

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### 3.10.5.5 Rate Shaping

The switch macro supports 128 instances of rate shaper instances. Each rate shaper is configurable to either token bucket mode or credit rate shaper mode. Each shaper measures the rate of an egress queue and prevent the queues which exceeded the configured rate from being scheduled for the next packet transmission. Shaping is based on a Committed Information Rate (CIR) and an associated Committed Burst Size (CBS). A queue is selectable for transmission only when it does not exceed the CBS for a given CIR.

Up to two shaping instances can be assigned to measure the egress rate of a specific queue or number of queues. Two shapers are typically assigned to measure the peak and committed rate and typically have different CIR settings. It is possible for any number of queues to share the same shaping instance. In this situation, the committed rate and the burst size are shared among the assigned queues.

When there is no shaper assigned to a queue, the queue rate is not monitored. MaxLinear recommends assigning a shaper for queues with high scheduling weights or strict priority queues. See **Section 3.10.5.6** for details regarding queue scheduling.

### 3.10.5.6 Queue Scheduling

The scheduling function determines which queue is allowed to emit a packet. Queue scheduling is done after rate shaping. The switch macro supports these scheduling types for each one of the 128 egress QoS queues:

- **Weighted Fair Queueing (WFQ)**
  For a given port, packets in the WFQ queues are scheduled for transmission in accordance with their configured weight. The weight represents a ratio for transmission. The higher the weight of one queue compared to another, the more this queue is scheduled for transmission.
  For example, a queue with a weight of 4000 is served twice as often than a queue with a weight of 2000.
- **Strict High Priority**
  For a given port, packets in the strict high priority queue are scheduled for transmission before any packet in the WFQ queue. When there are multiple strict high priority queues configured for a port, the queues with a higher physical number are scheduled first.
- **Strict Low Priority**
  For a given port, packets in the strict low priority queue are scheduled for transmission after any packet in the WFQ queue. When there are multiple strict low priority queues configured for a port, the queues with a higher physical number are scheduled first.

### 3.10.5.7 Congestion Management

The switch macro provides protection for the internal buffer from congestion and overflow.

When the shared buffer is fully occupied and does not have enough resources to receive any new frame, the incoming frames on all ports are discarded, until the congestion condition is relieved. See **Section 3.10.2.5** for flow control activation.

The switch macro also provides two segment thresholds per color globally and per color per egress queue. For every incoming packet, a decision is made whether to enqueue it or not, which is based on the configured thresholds of the respective packet color, and the global, port or queue segment filling level. This protection mechanism is called Active Congestion Management (ACM).

The color of the packets is decided based on the conformance rate in the metering instance. See **Section 3.10.5.4** for details. The thresholds are checked with accordance to the incoming packet color. For example, red thresholds apply to red-colored packets, yellow for yellow-colored packets, and green for green-colored packets.

The switch macro is able to reserve a buffer per egress queue. This allows the protection of queues against congestion caused by other queues and ports. It provides a minimum buffer guarantee for each queue. A green frame is permitted to bypass ACM and is always accepted by the queue when the reserved buffer threshold of the queue is not exceeded.

Critical frames bypass the ACM and are enqueued regardless of the filling level. Critical frames are not enqueued only in case of a buffer full event or a packet pointer full event.

The ACM function discards the frames early, before the buffer full event, with a certain drop probability. ACM thresholds provide three functionalities:

- **Minimum (MIN) Threshold**
  When the filling level of the queue is below this threshold, excluding the threshold value, the packet with the appropriate color is not discarded and is enqueued.
- **Maximum (MAX) Threshold**
  When the filling level of the queue is above this threshold, excluding the threshold value, the packet with the appropriate color is discarded.
- **½(Maximum-Minimum) ½(MAX-MIN) Threshold**
  When the filling level of the queue is between the MIN and MAX thresholds, the packet is discarded with certain probability. The drop probability profile is selectable globally between 25%, 50% and 75%. When the filling level is below half the distance between the minimum and maximum thresholds, the packet is discarded with a lower probability ($P_{min}$), when the filling level is above half the distance between the minimum and maximum thresholds, the packet is discarded with a higher probability ($P_{max}$).

### 3.10.5.8 Egress Queue Congestion Notification

802.1Qau operates in the link layer to provide a means for a bridge to notify a source of congestion allowing the source to reduce the flow rate.

In switch macro, the congestion level of each egress queue is monitored. If the congestion level is greater than 1/4 of green maximum threshold, congestion status of the egress queue is set to `1`. If the congestion level is lower than 1/4 of green minimum threshold, congestion status of the egress queue is cleared to `0`.

### 3.10.5.9 Storm Control

The switch macro supports a broadcast storm control function. A broadcast storm is defined as an excessive amount of broadcast, multicast, or unknown unicast Ethernet frames received on a switch port. Due to the massive replication of data frames, broadcast storms significantly degrade the system performance. Intentional broadcast storms are a form of Denial-of-Service (DoS) attack.

The storm control function effectively polices specific traffic type and protect the resources from being flooded by broadcast traffic.

The selected metering instance is configured to the required policed rate of the broadcast storm. Several traffic types are selectable for the storm control function:

- Broadcast frames

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- Unknown multicast frames
- Unknown unicast frames

When the rate of the selected frame types exceeds the rate configured in the meter instance, the frames are marked as either yellow or red. When the active congestion management thresholds are configured appropriately, the storm frames are discarded.

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### 3.10.6 Flow Classification Function

The switch macro includes a powerful packet classification engine which performs multi-field classifications based on up to 512 programmable rules.

#### Traffic Flow Table

The traffic flow table contains up to 512 programmable rules. Rules are configurable per ingress port, but are also sharable between ports. Each rule consists of a pattern section and an action section. A pattern specifies certain combination of packet header fields. The parser extracts the packet header fields from the received packet and provides them to the traffic flow table. When a pattern matches, the enabled actions apply. The pattern search continues until all actions are satisfied. This allows the definition of multiple pattern for different actions. It is possible to enable or disable an action for a given pattern.

The location of a rule in the table defines its priority. A rule with a lower index number has higher priority. The traffic flow table is searched using pattern matching and action matching.

- **Pattern Match:**
  A pattern row is considered matched when all of the fields in the pattern have been matched, not matched, or configured to be ignored. When a pattern row matches, the appropriate action row is checked for that pattern.
  *Note: It is possible for multiple pattern rows in a table to match the search, but only the first pattern in the table matched for certain action is applied.*
  The supported patterns include the source port information, packet length, and multiple L2/L3/L4/L4+ packet fields.
- **Action Match:**
  Each action in the action row can be enabled or disabled for certain pattern row match. When the action is enabled and the pattern row matched, this action is applied for the classified packet. The search in the table terminates only when all the actions in the action section have been found. When not, the search continues for the next pattern match and the corresponding action match. An additional option is to enable the action and to select a default behavior for that action, in other words, the search for another enabled action is terminated.
  *Note: For a given packet classification only one pattern may match one specific action, however, multiple patterns may match multiple different actions, in other words, the action section is searched independently for each action type.*
  The supported actions include destination port(s) assignment (including discard option), port filtering, traffic class assignment, traffic meter assignment, extended VLAN tagging operation assignment, flow counter assignment, OAM handling assignment, cross VLAN policy, cross state policy, color assignment, Link Aggregation Group (LAG) assignment, L2 MAC address learning policy, and interrupt policy.

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### 3.10.7 Operation, Administration, and Management Functions

This section summarizes the functions provided to control and monitor the data traffic through the switch.

#### 3.10.7.1 Monitoring Counters

Multiple counters are provided per port to monitor incoming and outgoing data traffic as well as errors or special events. Each port provides the same set of counters. The groups of counters are:

- A set of standard Ethernet counters, also known as RMON counters in RFC2819.
- A group of counters assigned to programmable traffic flows.
- A group of counters for metering.
- A group of counters for MAC learning discard events.

#### 3.10.7.2 Port Mirroring

The switch macro supports port monitoring and port redirection to assist in system debugging or to enable a software-controlled functionality. The data received on a selected port may be mirrored or redirected to another selected port (the monitoring port).

**Mirroring Function**

Ingress mirroring means the received frame is processed and forwarded as normal, but a copy of that frame is in addition sent to the monitoring port.

Egress mirroring means that the transmitted frame is forwarded as normal, but a copy of that egress frame (with modification) is in addition sent to the monitoring port.

The options given by the port mirroring function are:

- Copy data received on a selected port to the monitoring port.
- Copy data received on a selected group of ports to the monitoring port.
- Copy data transmitted on a selected port to the monitoring port.
- Copy data transmitted on a selected group of ports to the monitoring port.
- Copy data received or transmitted on a selected port to the monitoring port.
- Copy data received or transmitted on a selected group of ports to the monitoring port.

**Figure 20** and **Figure 21** provide illustrations on the ingress and egress monitoring.

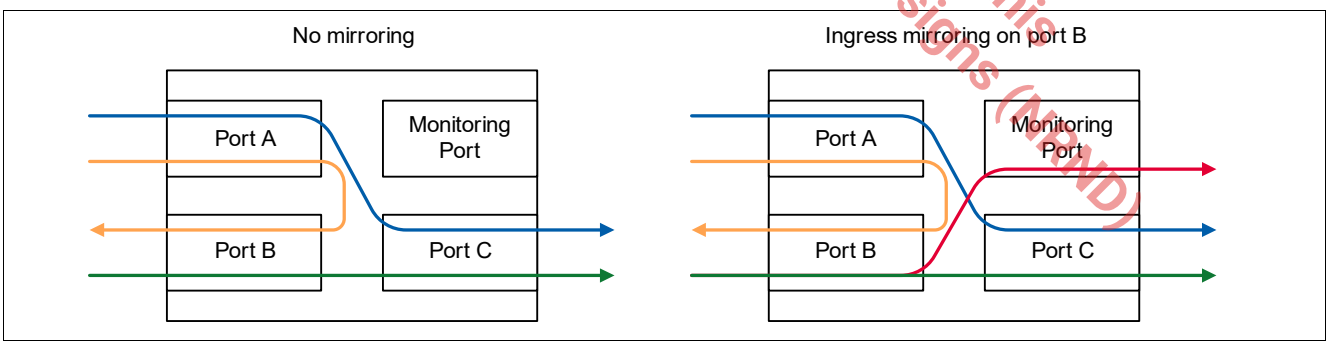



**Figure 20 Port Mirroring Examples – Ingress Monitoring**

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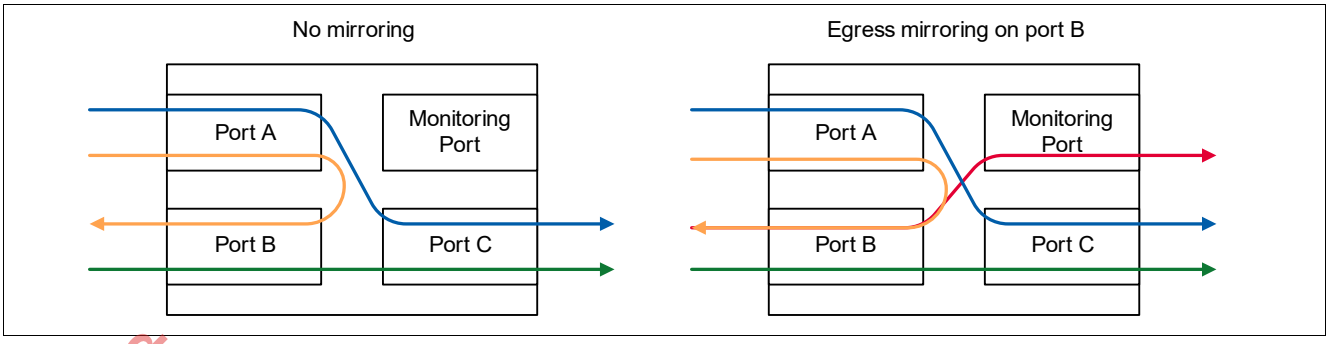



**Figure 21 Port Mirroring Examples – Egress Monitoring**

Mirroring is also usable to create diagnostic loopbacks, when the ingress port is identical to the monitoring port.

#### Error Monitoring

The mirroring function is used to monitor frames otherwise dropped due to reception errors, packet filtering, or violation of certain classification rules. In this case, the received frame is only delivered to the monitoring port and not to the target egress port defined in the egress port map.

It is possible to explicitly enable error monitoring for frames which contain MAC errors or when the MTU has been exceeded.

#### Egress Redirection Function

Egress redirection means that the received frame is processed but not forwarded as normal. Instead, that frame is sent to another MAC. **Figure 22** provides an illustration. The figure shows an egress traffic port B, which is the destination port, redirected to port D, the redirection port. Egress traffic is counted in port B's transmit counters. Egress packets are treated according to the configuration for port B.

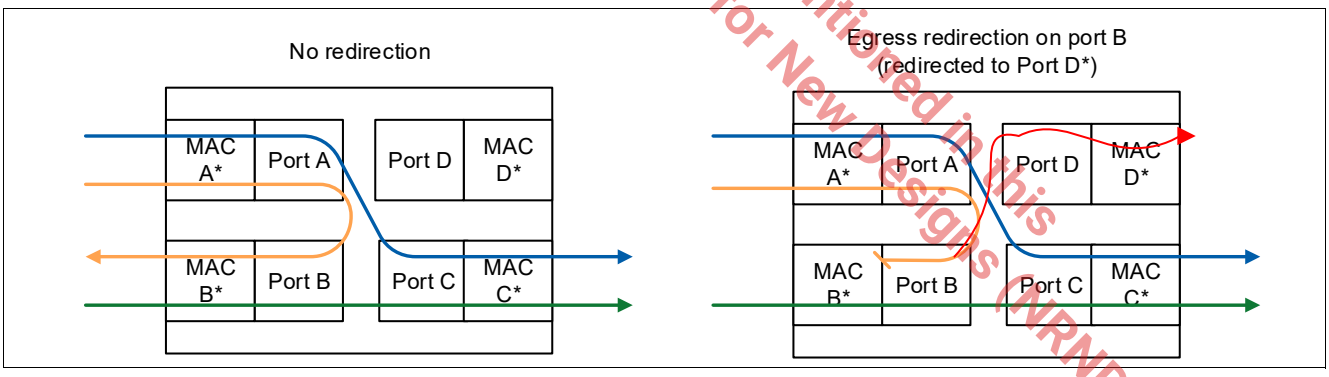



**Figure 22 Port Redirection Examples – Egress Redirection**

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### 3.10.7.3 Special Tag Functionality

The special tag is used to override the forwarding and QoS functionality of the switch on the ingress side and to provide additional frame-status information on the egress side.

The special tag is identified by the special Ethertype field located after the source MAC address in the Ethernet frame. This allows the transmission of the frame via an Ethernet network to a remote receiver. The special tag content has a fixed length of 6 bytes. For internal communication or point-to-point communication it can be configured per egress port when the frame contains additional content in place of the Ethertype. This option is only available at egress direction, in ingress direction always an Ethertype is expected. See **Figure 23**.

The pause frames generated by the MAC do not contain a special tag. This may result in a mix of frames with and without a special tag on one egress port. Frames with a special tag which do not use the special Ethertype are

distinguishable from pause frames because pause frames have an Ethertype of 0x8808 while the first nibble after the MAC addresses is 0 for frames with a special tag.

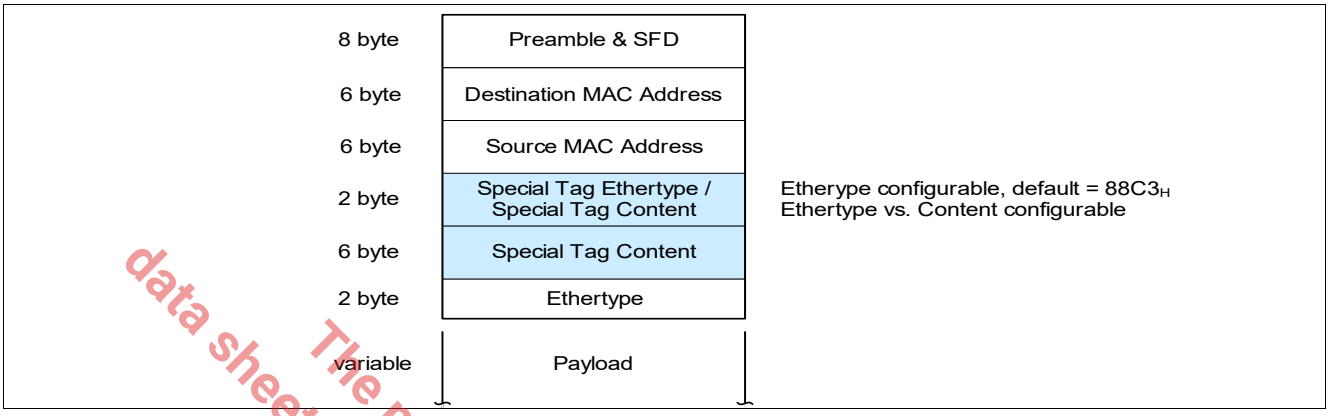



**Figure 23 Special Tag Location in the Frame**

*Note: The special tag is used on the CPU port of the switch.*

The content format of the special tag is different for the ingress and the egress.

### Ingress Special Tag

The ingress special tag is used to override the classification function and the default frame forwarding of the switch. Special tag detection on ingress is enabled or disabled per port. When the detection is disabled, the frame containing a special tag is treated as regular frame and the content of the frame is ignored.

When the ingress special tag detection is enabled, the content of the tag is used for the frame forwarding decision. The ingress special tag must always have a special tag Ethertype. See **Table 23** for details.

**Table 23 Special Tag Ingress Format**

| Byte | Bit | Description |
|---|---|---|
| 0 | [7:0] | **Ethertype MSB**<br>Byte 1<br>Configurable. Default $88_H$. |
| 1 | [7:0] | **Ethertype LSB**<br>Byte 2<br>Configurable. Default $C3_H$. |
| 2 | [7] | **Reserved**<br>Reserved. This field is not used internally by the switch. |
| 2 | [6:4] | **Sub-interface ID [14:12]**<br>See the Sub-interface ID portions of this table for a description. |
| 2 | [3:0] | **Traffic Class**<br>Target traffic class. This field is valid only when traffic class enable is set |
| 3 | [7] | **Pre-L2: Bit 1**<br>See below for description of Pre-L2 size. |
| 3 | [6] | **OAM Flag (OAM)**<br>This is OAM packet (Delay measurement and loss measurement packet)<br>$0_B$ **Disable** Not OAM packet<br>$1_B$ **Enable** OAM packet |

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**Table 23 Special Tag Ingress Format** (cont'd)

| Byte | Bit | Description |
|---|---|---|
| 3 | [5] | **Forced Learning Disable (LNMD)**<br>Forced leaning disable control<br>$0_B$ **Ignore** Leaning enable or disable is determined by the switch configurations<br>$1_B$ **Disable** Learning is forced to be disabled regardless of the switch configurations. |
| 3 | [4] | **Traffic Class Enable (TC_EN)**<br>Traffic class enable<br>$0_B$ **Ignore** traffic class is determined by the switch configurations.<br>$1_B$ **Enable** traffic class is determined in special tag traffic class field. |
| 3 | [3] | **Insertion Flag (INS)**<br>This is special packet (For example, Ethernet OAM or IGMP packets) and is inserted by CPU to the data path<br>$0_B$ **Disable** Not insertion packet<br>$1_B$ **Enable** insertion packet. |
| 3 | [2] | **Extraction Flag (EXT)**<br>This is special packet (For example, Ethernet OAM or IGMP packets) and is extracted to CPU from the data path<br>$0_B$ **Disable** Not extracted packet<br>$1_B$ **Enable** Extracted packet. |
| 3 | [1:0] | **Packet Type (PKT_TYPE)**<br>$00_B$ **Ether** Ethernet packet<br>$10_B$ **802.11** 802.11 format<br>$X1_B$ **Reserved** Reserved. |
| 4 | [7] | **Pre-L2: Bit 0**<br>Pre-L2 size in special tag does not include PMAC header and special tag.<br>Pre-L2 size in packet descriptor includes PMAC header.<br>$00_B$ **NIL** No Pre-L2 header<br>$01_B$ **16B** 16B Pre-L2 header<br>$10_B$ **32B** 32B Pre-L2 header<br>$11_B$ **48** 48B Pre-L2 header |
| 4 | [6] | **Reserved** |
| 4 | [5] | **Reserved** |
| 4 | [4] | **Sub-interface ID [15]**<br>See below for description of sub-interface ID. |
| 4 | [3:0] | **Sub-interface ID [11:8]**<br>See below for description of sub-interface ID. |
| 5 | [7:0] | **Sub-Interface ID [7:0]**<br>For ingress special tag<br>For packet with "Egress= 0" & "INS=1", it carries source sub-interface ID.<br>For packet with "Egress = 0" & "INS=0", it caries source sub-interface ID.<br>For packet with "Egress = 1" & "EXT=0", it carries destination sub-interface ID.<br>For packet with "Egress = 1" & "EXT=1", it carries source sub-interface ID.<br>For egress special tag:<br>For "EXT=0", it carries destination sub-interface ID.<br>For "EXT=1", it carries source sub-interface ID. |
| 6 | [7:0] | **Record ID [11:4]**<br>It is used for logging information for PTP and OAM packets |

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**Table 23 Special Tag Ingress Format** (cont'd)

| Byte | Bit | Description |
|---|---|---|
| 7 | [7:4] | **Record ID [3:0]**<br>It is used for logging information for PTP and OAM packets |
| 7 | [3:0] | **Source or Destination Logical Port ID (IGP/EGP)**<br>For ingress special tag:<br>For packet with "Egress= 0" & "INS=1", it carries source LPID.<br>For packet with "Egress = 0" & "INS=0", it caries source LPID.<br>For packet with "Egress = 1" & "EXT=0", it carries destination LPID.<br>For packet with "Egress = 1" & "EXT=0", it carries source LPID.<br>For egress special tag<br>For "EXT=0", it carries destination LPID.<br>For "EXT=1", it carries source LPID. |

*Note: Bytes are defined as MSB = bit 7 and LSB = bit 0.*

Table 24 describes the encoding of the traffic class enable fields of the special tag content.

**Table 24 Traffic Class Map Coding**

| Traffic Class Enable | Resulting Traffic Class |
|---|---|
| 0 | The traffic class is based on the classification result in switch. |
| 1 | The traffic class is taken from the special tag (classified traffic class ignored). |

An additional *Force No Learning* action flag is available in the ingress special tag. This action disables the learning of the source MAC address of the received frame in the MAC bridging table

The special tag detected on the ingress side is not delivered to the egress side. The tag is removed prior to transmission.

### Egress Special Tag

The egress special tag contains the status and debug information of the switch. Special tag transmission on egress is enabled or disabled per egress port. When egress special tag is disabled, no special tag is inserted in the egress frame. When egress special tag function is enabled, each egress frame transmitted on that port contains the special tag.

See Table 25 for more details regarding the egress special tag format.

*Note: Bytes are defined as MSB = bit 7 and LSB = bit 0.*

**Table 25 Special Tag Egress Format**

| Byte | Bit | Description |
|---|---|---|
| 0 | [7:0] | **Ethertype**<br>Byte 1<br>Configurable. Default $88_H$ |
| 1 | [7:0] | **Ethertype**<br>Byte 2<br>Configurable. Default: $C3_H$ |
| 2 | [7] | **Reserved**<br>Reserved. This field is not used internally by the switch. |
| 2 | [6:4] | **Sub-interface ID [14:12]**<br>See below for description of sub-interface ID. |

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**Table 25 Special Tag Egress Format**

| Byte | Bit | Description |
|---|---|---|
| 2 | [3:0] | **Traffic Class**<br>Traffic class of the packet determined by the switch QoS classification. |
| 3 | [7] | **Pre-L2: Bit 1**<br>See below for description of Pre-L2 size. |
| 3 | [6] | **OAM Flag (OAM)**<br>This is OAM packet (Delay measurement and loss measurement packet)<br>$0_B$ **Disable** Not OAM packet<br>$1_B$ **Enable** OAM packet |
| 3 | [5] | **Reserved**<br>This field is fixed to 0. |
| 3 | [4] | **Reserved**<br>This field is fixed to 0. |
| 3 | [3] | **Insertion Flag (INS)**<br>This is special packet (For example, Ethernet OAM or IGMP packets) and is inserted by CPU to the data path.<br>$0_B$ **Disable** Not insertion packet<br>$1_B$ **Enable** Insertion packet |
| 3 | [2] | **Extraction Flag (EXT)**<br>This is special packet (For example, Ethernet OAM or IGMP packets) and is extracted to CPU from the data path.<br>$0_B$ **Disable** Not extracted packet<br>$1_B$ **Enable** Extracted packet |
| 3 | [1:0] | **Packet Type (PKT_TYPE)**<br>$00_B$ **Ether** Ethernet packet<br>$10_B$ **802.11** 802.11 format<br>$X1_B$ **Reserved** Reserved. |
| 4 | [7] | **OAM Flag (OAM)**<br>This is OAM packet (Delay measurement and loss measurement packet)<br>$0_B$ **Disable** Not special OAM packet<br>$1_B$ **Enable** Special OAM packet |
| 4 | [6] | **Reserved** |
| 4 | [5] | **Reserved** |
| 4 | [4] | **Sub-interface ID [15]**<br>See below for description of sub-interface ID. |
| 4 | [3:0] | **Sub-interface ID [11:8]**<br>See below for description of sub-interface ID. |
| 5 | [7:0] | **Sub-Interface ID [7:0]**<br>For “EXT=0”, it carries destination sub-interface ID.<br>For “EXT=1”, it carries source sub-interface ID. |
| 6 | [7:0] | **Record ID MSB bit 11 to 4.**<br>It is used for logging information for PTP and OAM packets |

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**Table 25 Special Tag Egress Format**

| Byte | Bit | Description |
|---|---|---|
| 7 | [7:4] | **Record ID MSB bit 3 to 0.**<br>It is used for logging information for PTP and OAM packets |
| 7 | [3:0] | **Source or Destination Logical Port ID (IGP/EGP)**<br>For “EXT=0”, it carries destination logical port ID.<br>For “EXT=1”, it carries source logical port ID. |

### 3.10.7.4 Loop Detection

The loop detection feature detects a loop in the network and triggers an alarm, which is usually indicated by an LED. It does not prevent the loop like STP, so a network administrator must be able to clearly see the alarm and resolve the loop by manual means. The violating ports are not disabled by means of any protocol.

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# 4 MDIO and MMD Register Interface Description

This chapter describes the MDIO and MMD registers available to support the MxL86280C feature set. These registers are accessible by an external management entity (called STA in IEEE) to control, configure, or read the status of the MxL86280C. After power-on, the MxL86280C resets the MDIO and MMD registers to default values sufficient to operate without specific programing.

All the register definitions, behaviors, and fields are strictly compliant with IEEE 802.3. Refer to IEEE 802.3 [2] for more information about the registers. The only registers not referenced in IEEE 802.3 are two register groups that are vendor-specific: VSPEC1 and VSPEC2. These allow custom functions related to MxL86280C.

In the register descriptions, the section or table references refer to the IEEE 802.3 [2].

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## 4.1 MDIO-specific Terminology

This list describes how the common IEEE 802.3 terms relate to MDIO and MMD register concepts discussed in this chapter.

- **STA**: Station Management. A host connected to the MDIO interface. STAs are generally Media Access Controllers (MACs). The STA drives the MDIO bus as a clock master and the MxL86280C is an MDIO slave.
- **Host**: Used as a synonym of STA in this document.
- **PHY**: Physical Layer. In the MxL86280C, this encompasses Analog Signal Processing, Digital Signal Processing, and Physical Coding Sublayer (PCS). The PHY contains several sublayers that are individually manageable entities known as MDIO manageable devices (MMDs).
- **MMD**: MDIO Manageable Device. The list of MMDs available in the MxL86280C is in Section 4.3.
- **Device**: In the context of the MDIO/MMD registers, a device is a register bank grouped by logical sublayers of the PHY layer.
- **Clause**: Refers to a particular section of the IEEE 802.3 standard [2]. In particular, Clause 22 describes MDIO device 0 and Clause 45 describes the other MMDs.
- **MII**: Media Independent Interface. This encompasses the MDIO and the (G)MII as described in Clause 22. STD registers in device 0 are also called MII registers.

## 4.2 Register Naming and Numbering

The register numbering convention in this document is similar to that of IEEE 802.3.

The numbering syntax uses three numbers, a.b.c, as specified in IEEE 802.3, paragraph 45.1 [2], and the notation is generalized to Clause 22 registers in device 0 STD. The alphanumeric syntax also uses the same structure and uses the names of the MMD devices, registers, and register fields separated by underscores and dots.

### 4.2.1 Register Numbering

The syntax is as follows, with a, b, and c written as decimal numbers:

a.b.c = <DEVICE_NUMBER>.<REGISTER_NUMBER>.<FIELD_NUMBER>

When the last indicator (c) is omitted, the register numbering refers to the full register.

When a field is more than a single bit, the bit range is indicated using a colon (for example, 1:3 is the field of bits 1 to 3). In an MDIO register, the least significant bit is bit 0 and most significant bit is bit 15. All MDIO registers are 16-bit wide.

### 4.2.2 Register Naming

The syntax is as follows, with AA, BB, and CC written as alphanumeric strings:

AA_BB.CC = <DEVICE_NAME>_<REGISTER_NAME>.<FIELD_NAME>

When the last indicator (CC) is omitted, the register naming refers to the full register.

The fields named RES, RES1, and RES2 refer to reserved fields as per IEEE 802.3.

### 4.2.3 Examples

`STD_STAT.ANOK` is the name of the field 0.1.5, which indicates that auto-negotiation is complete.

`ANEG_CTRL.ANEG_RESTART` is the name of the field 7.0.9, which allows the STA to restart the Ethernet ANEG procedure.

`ANEG_PHYID1` is the complete 16-bit register number 7.2, for the PHY identifier 1 number.

`VSPEC1_LED1.BLINKS` is the 4-bit wide field number 30.2.15:12, which contains LED1 slow blinking configuration.

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## 4.3 MMD Devices Present in MxL86280C

The MMD devices implement groups of standardized registers under the management of the STA.

**Table 26 MDIO/MMD Devices Present in MxL86280C**

| MDIO/MMD Name | Device Number (decimal) | Description |
|---|---|---|
| STD | 0 | MDIO Standard Device as described in Clause 22. This also contains a number of MxL86280C-specific PHY registers. |
| PMAPMD | 1 | Control and status registers related to the PMA/PMD signal processing modules |
| PCS | 3 | Control and status registers related to the PCS encoding/decoding device |
| ANEG | 7 | Control and status registers related to the auto-negotiation device |
| VSPEC1 | 30 | MxL86280C-specific LED control and other MxL86280C-specific control |
| VSPEC2 | 31 | MxL86280C-specific WoL control |

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## 4.4 Responsibilities of the STA

The MxL86280C responds to all published register addresses for the device and returns a value of zero for undefined and unsupported registers.

In accordance with IEEE 802.3 guidelines, it is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs of the MxL86280C.

The MxL86280C ignores writes to the PMA/PMD speed selection bits that select speeds not advertised in the PMA/PMD speed ability register. The PMA/PMD speed selection defaults to a supported ability.

API is provided to access the PHY MDIO and MMD registers, which cannot be accessed directly.

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## 4.5 MDIO Access Protocols to Read / Write Registers

All the MDIO/MMD registers are accessible from an external chip connected to the MDIO bus on the MDIO_S and MDC_S pins. The MxL86280C supports several MDIO frame protocols:

- Clause 22: To access Device 0
- Clause 22 Extended: To access other devices using the indirection scheme specified by IEEE 802.3
  Dev 1: PMAPMD
  Dev 3: PCS
  Dev 7: ANEG
  Dev 30: VSPEC1
  Dev 31: VSPEC2
- Clause 45: to access all devices

Both Clause 22 Extended and Clause 45 are used to access MMD devices. However, the mechanism implemented in the MxL86280C provides faster speeds using Clause 45. It creates differences in latencies in the MDIO reply:

- The Clause 22 Extended protocol involves an indirect mechanism.
- The Clause 45 protocol provides faster replies.

The Clause 22 registers are accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. Refer to IEEE 802.3 section 45 [2].

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# 5 PHY MDIO Registers Detailed Description

**Table 27 Register Access Type**

| Mode | Symbol |
|---|---|
| Read-Only Register (Status or Ability Register) | RO |
| Read-Write Register (MDIO Register) | RW |
| Read-Write Self-Clearing Register (bit cleared after read from MDIO) | RWSC |
| Read-Only Self-Clearing Register (bit cleared after read from MDIO) | ROSC |
| Read-Only Latching Low Register | ROLL |
| Read-Only Latching High Register | ROLH |

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## 5.1 Standard Management Registers

This section describes the IEEE 802.3 standard management registers corresponding to Clause 22.

**Table 28 Registers Overview- Standard Management Registers**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| STD_CTRL | STD Control (Register 0.0) | $3040_H$ |
| STD_STAT | Status Register (Register 0.1) | $7949_H$ |
| STD_PHYID1 | PHY Identifier 1 (Register 0.2) | $C133_H$ |
| STD_PHYID2 | PHY Identifier 2 (Register 0.3) | $5400_H$ 1) |
| STD_AN_ADV | Auto-Negotiation Advertisement (Register 0.4) | $9DE1_H$ |
| STD_AN_LPA | Auto-Negotiation Link Partner Ability (Register 0.5) | $1DE0_H$ |
| STD_AN_EXP | Auto-Negotiation Expansion (Register 0.6) | $0064_H$ |
| STD_AN_NPTX | Auto-Negotiation Next Page Transmit Register (Register 0.7) | $2001_H$ |
| STD_AN_NPRX | Auto-Negotiation Link Partner Received Next Page Register (Register 0.8) | $0000_H$ |
| STD_GCTRL | Gigabit Control Register (Register 0.9) | $0200_H$ |
| STD_GSTAT | Gigabit Status Register (Register 0.10) | $0000_H$ |
| STD_MMDCTRL | MMD Access Control Register (Register 0.13) | $0000_H$ |
| STD_MMDDATA | MMD Access Data Register (Register 0.14) | $0000_H$ |
| STD_XSTAT | Extended Status Register (Register 0.15) | $2000_H$ |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

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### 5.1.1 Standard Management Register Descriptions

This section describes all the STD registers in detail.

**STD Control (Register 0.0)**

This register controls the main functions of the PHY.

IEEE Standard Register=0.0

**STD_CTRL** **Reset Value**

**STD Control (Register 0.0)** **$3040_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 … 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| **RST** | **LB** | **SSL** | **ANEN** | **PD** | **ISOL** | **ANRS** | **DPLX** | **COL** | **SSM** | **RES** |
| rwsc | rw | rw | rw | rw | rw | rwsc | rw | rw | rw | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RWSC | **Reset**<br>Resets the PHY to its default state. Active links are terminated. This is a self-clearing bit, which is set to zero by the hardware after a reset is performed.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **RESET** Resets the device. |
| LB | 14 | RW | **Loopback on GMII**<br>This mode enables looping back of MII data from the transmit to the receive direction. No data is transmitted to the Ethernet PHY.<br>The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **ENABLE** Closes the loopback from Tx to Rx at xMII. |
| SSL | 13 | RW | **Forced Speed Selection LSB**<br>This bit only takes effect when bit ANEN is set to zero, which disables the auto-negotiation process. This is the lower bit (LSB) of the forced speed selection and is used in conjunction with the higher bit (MSB).<br>The standard procedure to force 2500 Mbps operation (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0].<br>The GPHY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13.<br>This is the MSB LSB bit value encoding:<br>$00_B$ 10 Mbps<br>$01_B$ 100 Mbps<br>$10_B$ 1000 Mbps<br>$11_B$ Reserved, defaults to 2500 Mbps operation when the PMA_CTRL register 1.0.5:2 equals [0 1 1 0]. |

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| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ANEN | 12 | RW | **Auto-Negotiation Enable**<br>Allows enabling and disabling of the auto-negotiation process capability of the PHY. When enabled, the force bits for duplex mode (CTRL.DPLX) and the speed selection (CTRL.SSM, CTRL.SSL) become inactive; otherwise, the force bits define the PHY operation.<br>$0_B$ **DISABLE** Disables the auto-negotiation protocol.<br>$1_B$ **ENABLE** Enables the auto-negotiation protocol. |
| PD | 11 | RW | **Power Down**<br>Forces the device into a power down state (SLEEP) in which power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **POWERDOWN** Forces the device into power down mode. |
| ISOL | 10 | RW | **Isolate**<br>The isolation mode isolates the PHY from the MAC. The MAC interface inputs are ignored, whereas the MAC interface outputs are set to tristate (high-impedance).<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **ISOLATE** Isolates the PHY from the MAC. |
| ANRS | 9 | RWSC | **Restart Auto-Negotiation**<br>Restarts the auto-negotiation process on the MDI. This bit does not have any effect when auto-negotiation is disabled using CTRL.ANEN. This bit is self-clearing after the auto-negotiation process is initiated.<br>$0_B$ **NORMAL** Stays in current mode.<br>$1_B$ **RESTART** Restarts auto-negotiation. |
| DPLX | 8 | RW | **Forced Duplex Mode**<br>This bit only takes effect when bit CTRL.ANEN is set to zero, which disables the auto-negotiation process. This bit controls the forced duplex mode. It allows forcing of the PHY into full-duplex or half-duplex mode. This bit does not take effect in loopback mode, when bit CTRL.LB is set to $1_B$.<br>It is only possible to force the duplex mode to half-duplex in 10BASE-T and 100BASE-TX speed modes. This field is ignored for higher speeds.<br>$0_B$ **HD** Half-duplex<br>$1_B$ **FD** Full-duplex |
| COL | 7 | RW | **Collision Test**<br>Allows testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency.<br>$0_B$ **DISABLE** Normal operational mode<br>$1_B$ **ENABLE** Activates the collision test. |

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| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SSM | 6 | RW | **Forced Speed Selection MSB**<br>This bit only takes effect when bit ANEN is set to zero, which disables the auto-negotiation process. This is the higher bit (MSB) of the forced speed selection and is used in conjunction with the lower bit (LSB).<br>The preferred way to force 2500 Mbps operation (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0].<br>The GPHY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13.<br>This is the MSB LSB bit value encoding:<br>$00_B$ 10 Mbps<br>$01_B$ 100 Mbps<br>$10_B$ 1000 Mbps<br>$11_B$ Reserved, defaults to 2500 Mbps operation when the PMA_CTRL register 1.0.5:2 equals [0 1 1 0]. |
| RES | 5:0 | RO | **Reserved**<br>Write as zero, ignore on read. |

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### Status Register (Register 0.1)

This register contains status and capability information about the device. All the bits are read-only. A write access by the MAC does not have any effect. Refer to IEEE 802.3 22.2.4.2.

IEEE Standard Register=0.1

**STD_STAT** **Reset Value**

**Status Register (Register 0.1)** **$7949_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CBT4** | **CBTXF** | **CBTXH** | **XBTF** | **XBTH** | **CBT2F** | **CBT2H** | **EXT** | **RES** | **MFPS** | **ANOK** | **RF** | **ANAB** | **LS** | **JD** | **XCAP** |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | rolh | ro | roll | rolh | ro |

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| Field | Bits | Type | Description |
|---|---|---|---|
| CBT4 | 15 | RO | **IEEE 100BASE-T4**<br>Specifies the 100BASE-T4 ability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| CBTXF | 14 | RO | **IEEE 100BASE-TX Full Duplex**<br>Specifies the 100BASE-TX full duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| CBTXH | 13 | RO | **IEEE 100BASE-TX Half-Duplex**<br>Specifies the 100BASE-TX half-duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| XBTF | 12 | RO | **IEEE 10BASE-T Full-Duplex**<br>Specifies the 10BASE-T full-duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| XBTH | 11 | RO | **IEEE 10BASE-T Half-Duplex**<br>Specifies the 10BASE-T half-duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| CBT2F | 10 | RO | **IEEE 100BASE-T2 Full-Duplex**<br>Specifies the 100BASE-T2 full-duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| CBT2H | 9 | RO | **IEEE 100BASE-T2 Half-Duplex**<br>Specifies the 100BASE-T2 half-duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| EXT | 8 | RO | **Extended Status**<br>The extended status registers are used to specify 1000 Mbps speed capabilities in the register XSTAT.<br>$0_B$ **DISABLED** No extended status information available in register 15<br>$1_B$ **ENABLED** Extended status information available in register 15 |
| RES | 7 | RO | **Reserved**<br>Ignore when read. |
| MFPS | 6 | RO | **Management Preamble Suppression**<br>Specifies the Management Frame (MF) preamble suppression ability.<br>$0_B$ **DISABLED** PHY requires management frames with preamble.<br>$1_B$ **ENABLED** PHY accepts management frames without preamble. |
| ANOK | 5 | RO | **Auto-Negotiation Completed**<br>Indicates whether the auto-negotiation process is completed or in progress.<br>$0_B$ **RUNNING** Auto-negotiation process is in progress.<br>$1_B$ **COMPLETED** Auto-negotiation process is completed. |
| RF | 4 | ROLH | **Remote Fault**<br>Indicates the detection of a remote fault event. GPHY does not indicate RF.<br>$0_B$ **INACTIVE** No remote fault condition detected<br>$1_B$ **ACTIVE** Remote fault condition detected |
| ANAB | 3 | RO | **Auto-Negotiation Ability**<br>Specifies the auto-negotiation ability.<br>$0_B$ **DISABLED** PHY is not able to perform auto-negotiation.<br>$1_B$ **ENABLED** PHY is able to perform auto-negotiation. |
| LS | 2 | ROLL | **Link Status**<br>Indicates the link status of the PHY to the link partner.<br>$0_B$ **INACTIVE** The link is down. No communication with link partner possible.<br>$1_B$ **ACTIVE** The link is up. Data communication with link partner is possible. |
| JD | 1 | ROLH | **Jabber Detect**<br>Indicates that a jabber event was detected.<br>$0_B$ **NONE** No jabber condition detected<br>$1_B$ **DETECTED** Jabber condition detected |
| XCAP | 0 | RO | **Extended Capability**<br>Indicates the availability and support of extended capability registers.<br>$0_B$ **DISABLED** Only base registers are supported.<br>$1_B$ **ENABLED** Extended capability registers are supported. |

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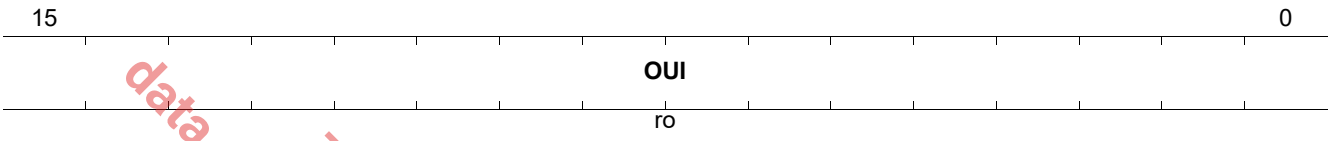
**PHY Identifier 1 (Register 0.2)**

This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number.

IEEE Standard Register=0.2

**STD_PHYID1** **Reset Value**

**PHY Identifier 1 (Register 0.2)** **$C133_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier Bits 3:18** |

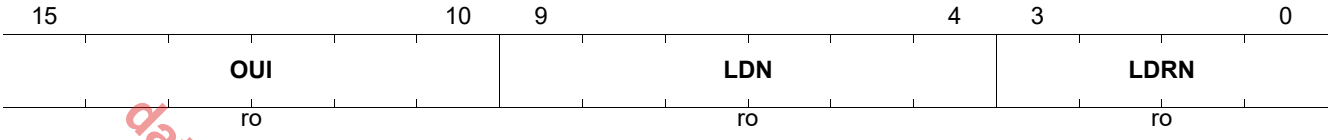
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**PHY Identifier 2 (Register 0.3)**

IEEE Standard Register=0.3

**STD_PHYID2** **Reset Value**

**PHY Identifier 2 (Register 0.3)** **$5400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several different products. |
| LDRN | 3:0 | RO | **Device Revision Number**<br>Specifies the device revision number[1)] to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

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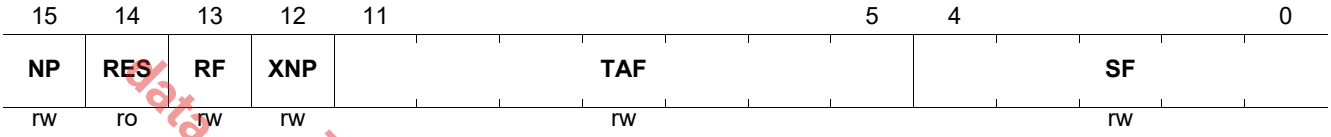
### Auto-Negotiation Advertisement (Register 0.4)

This register contains the advertised abilities of the PHY during auto-negotiation.

IEEE Standard Register=0.4

**STD_AN_ADV** **Reset Value**

**Auto-Negotiation Advertisement (Register 0.4)** **$9DE1_H$**




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| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page**<br>The next page indication is encoded in bit AN_ADV.NP regardless of the selector field value or link code word encoding. The PHY always advertises NP when a 1000BASE-T mode is advertised during auto-negotiation.<br>$0_B$ **INACTIVE** No next page to follow<br>$1_B$ **ACTIVE** Additional next page(s) to follow |
| RES | 14 | RO | **Reserved**<br>Write as zero, ignore on read. |
| RF | 13 | RW | **Remote Fault**<br>This bit allows indication of a fault to the link partner.<br>$0_B$ **NONE** No remote fault is indicated.<br>$1_B$ **FAULT** A remote fault is indicated. |
| XNP | 12 | RW | **Extended Next Page**<br>Indicates the GPHY supports transmission of extended next pages (XNP).<br>$0_B$ **UNABLE** GPHY is XNP unable.<br>$1_B$ **ABLE** GPHY is XNP able. |
| TAF | 11:5 | RW | **Technology Ability Field**<br>This is an 8-bit wide field containing information indicating supported technologies. The GPHY supports half-duplex and full-duplex 10BASE-T and 100BASE-TX and also both symmetric and asymmetric PAUSE.<br>$40_H$ **PS_ASYM** Advertises asymmetric pause<br>$20_H$ **PS_SYM** Advertises symmetric pause<br>$10_H$ **DBT4** Advertises 100BASE-T4<br>$08_H$ **DBT_FDX** Advertises 100BASE-TX full-duplex<br>$04_H$ **DBT_HDX** Advertises 100BASE-TX half-duplex<br>$02_H$ **XBT_FDX** Advertises 10BASE-T full-duplex<br>$01_H$ **XBT_HDX** Advertises 10BASE-T half-duplex |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SF | 4:0 | RW | **Selector Field**<br>This field is a 5-bit wide field for encoding 32 possible messages. The encodings are defined in IEEE 802.3-2008 Annex 28A. Unspecified combinations are reserved for future use. Reserved combinations of this field are not to be transmitted.<br>$00001_B$**IEEE802DOT3** Selects the IEEE 802.3 technology. |

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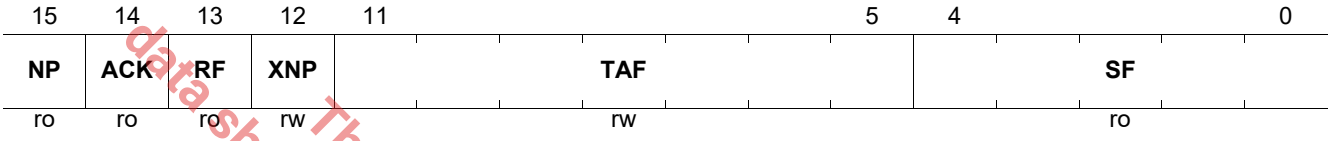
### Auto-Negotiation Link Partner Ability (Register 0.5)

IEEE Standard Register=0.5

When the auto-negotiation is complete, this register contains the advertised ability of the link partner. The bit definitions are a direct representation of the received link code word.

**STD_AN_LPA** **Reset Value**

**Auto-Negotiation Link Partner Ability (Register 0.5)** **$1DE0_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Next Page**<br>Next page request indication from the link partner.<br>$0_B$ **INACTIVE** No next page to follow<br>$1_B$ **ACTIVE** Additional next pages to follow |
| ACK | 14 | RO | **Acknowledge**<br>Acknowledgment indication from the link partner's link code word.<br>$0_B$ **INACTIVE** The device did not receive its link partner's link code word.<br>$1_B$ **ACTIVE** The device received its link partner's link code word. |
| RF | 13 | RO | **Remote Fault**<br>Remote fault indication from the link partner.<br>$0_B$ **NONE** Remote fault is not indicated by the link partner.<br>$1_B$ **FAULT** Remote fault is indicated by the link partner. |
| XNP | 12 | RW | **Extended Next Page**<br>Indicates the GPHY supports transmission of extended next pages (XNP).<br>$0_B$ **UNABLE** Link partner is XNP unable.<br>$1_B$ **ABLE** Link partner is XNP able. |
| TAF | 11:5 | RW | **Technology Ability Field**<br>$40_H$ **PS_ASYM** Advertises asymmetric pause<br>$20_H$ **PS_SYM** Advertises symmetric pause<br>$10_H$ **DBT4** Advertises 100BASE-T4<br>$08_H$ **DBT_FDX** Advertises 100BASE-TX full-duplex<br>$04_H$ **DBT_HDX** Advertises 100BASE-TX half-duplex<br>$02_H$ **XBT_FDX** Advertises 10BASE-T full-duplex<br>$01_H$ **XBT_HDX** Advertises 10BASE-T half-duplex |
| SF | 4:0 | RO | **Selector Field**<br>$00001_B$**IEEE802DOT3** Selects the IEEE 802.3 technology |

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### Auto-Negotiation Expansion (Register 0.6)

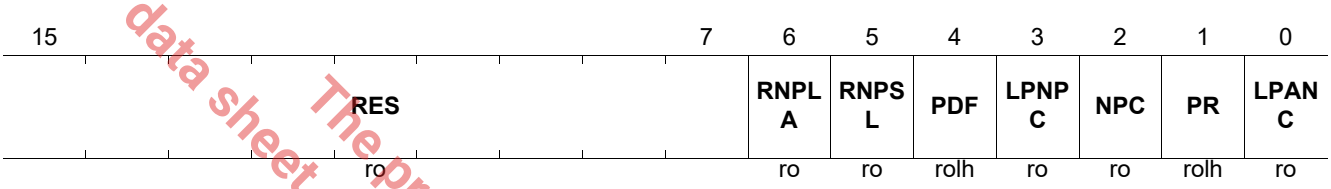
This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. This register is valid only after the auto-negotiation is completed.

Refer to IEEE 802.3 28.2.4.1.5.

IEEE Standard Register=0.6

**STD_AN_EXP** **Reset Value**

**Auto-Negotiation Expansion (Register 0.6)** **$0064_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:7 | RO | **Reserved**<br>Write as zero, ignore on read. |
| RNPLA | 6 | RO | **Receive Next Page Location Able**<br>According to 802.3-2015, indicates the Rx NP location is indicated by field RNPSL.<br>$0_B$ **UNABLE** Received Next Page Storage Location is not specified by bit (6.5).<br>$1_B$ **ABLE** Received Next Page Storage Location is specified by bit (6.5). |
| RNPSL | 5 | RO | **Receive Next Page Storage Location**<br>According to 802.3-2015, indicates the Rx NP is in register 0.8 for the GPHY.<br>$0_B$ **FIVE** Link partner next pages are stored in register 5.<br>$1_B$ **EIGHT** Link partner next pages are stored in register 8. |
| PDF | 4 | ROLH | **Parallel Detection Fault**<br>$0_B$ **NONE** A fault was not detected via the parallel detection function.<br>$1_B$ **FAULT** A fault was detected via the parallel detection function. |
| LPNPC | 3 | RO | **Link Partner Next Page Capable**<br>$0_B$ **UNABLE** Link partner is unable to exchange next pages.<br>$1_B$ **CAPABLE** Link partner is capable of exchanging next pages. |
| NPC | 2 | RO | **Next Page Capable**<br>$0_B$ **UNABLE** GPHY is unable to exchange next pages.<br>$1_B$ **CAPABLE** GPHY is capable of exchanging next pages. |
| PR | 1 | ROLH | **Page Received**<br>$0_B$ **NONE** A new page was not received.<br>$1_B$ **RECEIVED** A new page was received. |
| LPANC | 0 | RO | **Link Partner Auto-Negotiation Capable**<br>$0_B$ **UNABLE** Link partner is unable to auto-negotiate.<br>$1_B$ **CAPABLE** Link partner is auto-negotiation capable. |

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

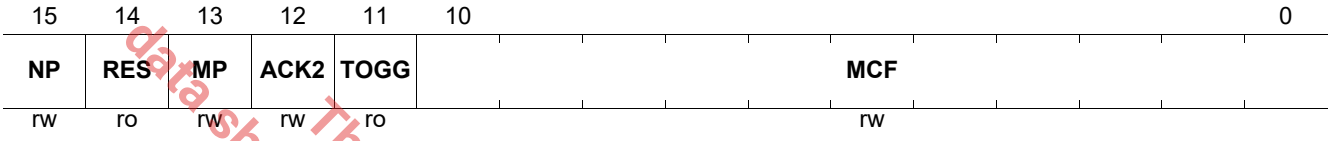
### Auto-Negotiation Next Page Transmit Register (Register 0.7)

The auto-negotiation next page transmit register contains the next page link code word to be transmitted when next page ability is supported. Refer to IEEE 802.3 28.2.4.1.6.

IEEE Standard Register=0.7

**STD_AN_NPTX** **Reset Value**

**Auto-Negotiation Next Page Transmit Register (Register 0.7)** **$2001_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page**<br>$0_B$ **INACTIVE** Last page<br>$1_B$ **ACTIVE** Additional next page(s) to follow |
| RES | 14 | RO | **Reserved**<br>Write as zeros, ignore on read. |
| MP | 13 | RW | **Message Page**<br>Indicates the content of MCF is either an unformatted page or a formatted message.<br>$0_B$ **UNFOR** Unformatted page<br>$1_B$ **MESSG** Message page |
| ACK2 | 12 | RW | **Acknowledge 2. GPHY Does Not Comply**<br>$0_B$ **INACTIVE** Device is not able to comply with message.<br>$1_B$ **ACTIVE** Device complies with message. |
| TOGG | 11 | RO | **Toggle**<br>This bit always takes the opposite value of the Toggle bit in the previously exchanged link code word.<br>$0_B$ **ZERO** Previous value of the transmitted link code word was $1_B$.<br>$1_B$ **ONE** Previous value of the transmitted link code word was $0_B$. |

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The product (or products) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MCF | 10:0 | RW | **Message or Unformatted Code Field**<br>When the Message Page bit is set to $1_B$ (0.7.13), this field is the Message Code Field of a message page used in next page exchange. The message codes are described in IEEE 802.3 Appendix 28C.<br>It is used to indicate the type of message in UCF1 and UCF2.<br>$00_H$ Reserved<br>$01_H$ Null message<br>$02_H$ One Unformatted Page (UP) with TAF follows<br>$03_H$ Two UPs with TAF follows<br>$04_H$ Remote fault details message<br>$05_H$ OUI message<br>$06_H$ PHY ID message<br>$07_H$ 100BASE-T2 message<br>$08_H$ 1000BASE-T message<br>$09_H$ MULTIGBASE-T message<br>$0A_H$ EEE technology capability follows in next UP<br>$0B_H$ OUI XNP |

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The product (or products) mentioned in this

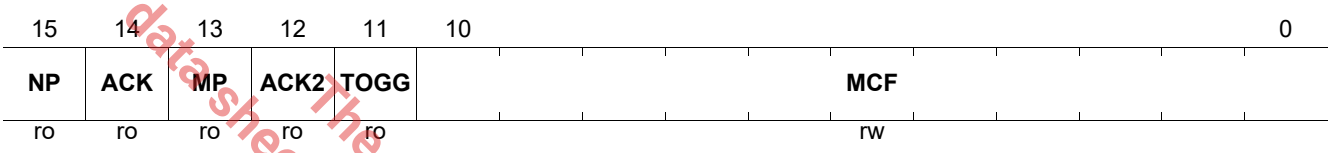
### Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)

This register contains the next page link code word received from the link partner. Refer to IEEE 802.3-2008 28.2.4.1.7.

IEEE Standard Register=0.8

**STD_AN_NPRX** **Reset Value**

**Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Next Page**<br>$0_B$ **INACTIVE** No next pages to follow<br>$1_B$ **ACTIVE** Additional next page(s) to follow |
| ACK | 14 | RO | **Acknowledge**<br>$0_B$ **INACTIVE** The device did not receive its link partner's link code word.<br>$1_B$ **ACTIVE** The device received its link partner's link code word. |
| MP | 13 | RO | **Message Page**<br>Indicates the content of MCF is either an unformatted page or a formatted message.<br>$0_B$ **UNFOR** Unformatted page<br>$1_B$ **MESSG** Message page |
| ACK2 | 12 | RO | **Acknowledge 2**<br>$0_B$ **INACTIVE** Device is not able to comply with the message.<br>$1_B$ **ACTIVE** Device complies with the message. |
| TOGG | 11 | RO | **Toggle**<br>This bit always takes the opposite value of the Toggle bit in the previously exchanged link code word.<br>$0_B$ **ZERO** Previous value of the transmitted link code word was $1_B$.<br>$1_B$ **ONE** Previous value of the transmitted link code word was $0_B$. |

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The product (or products) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MCF | 10:0 | RW | **Message or Unformatted Code Field**<br>This field is the Message Code Field of a message page used in next page exchange.<br>The message codes are described in IEEE 802.3 Appendix 28C.<br>It is used to indicate the type of message in UCF1 and UCF2.<br>$00_H$ Reserved<br>$01_H$ Null message<br>$02_H$ One Unformatted Page (UP) with TAF follows<br>$03_H$ Two UPs with TAF follows<br>$04_H$ Remote fault details message<br>$05_H$ OUI message<br>$06_H$ PHY ID message<br>$07_H$ 100BASE-T2 message<br>$08_H$ 1000BASE-T message<br>$09_H$ MULTIGBASE-T message<br>$0A_H$ EEE technology capability follows in next UP<br>$0B_H$ OUI XNP |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

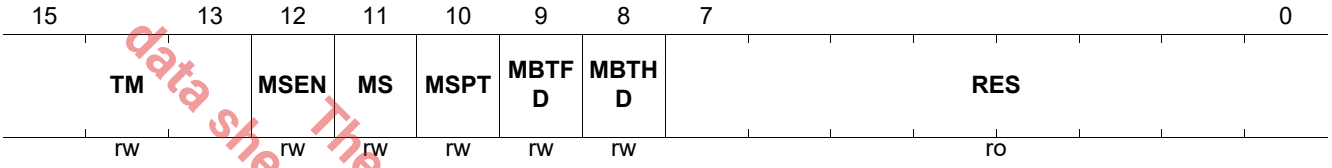
### Gigabit Control Register (Register 0.9)

This is the control register to configure the Gigabit Ethernet behavior of the PHY. Refer to IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.9

**STD_GCTRL** **Reset Value**

**Gigabit Control Register (Register 0.9)** **$0200_H$**




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| Field | Bits | Type | Description |
|---|---|---|---|
| TM | 15:13 | RW | **Transmitter Test Mode**<br>This register field allows enabling of the standard transmitter test modes.<br>$000_B$ **NOP** Normal operation<br>$001_B$ **WAV** Test mode 1 transmit waveform test<br>$010_B$ **JITM** Test mode 2 transmit jitter test in master mode<br>$011_B$ **JITS** Test mode 3 transmit jitter test in slave mode<br>$100_B$ **DIST** Test mode 4 transmitter distortion test |
| MSEN | 12 | RW | **Master/Slave Manual Configuration Enable**<br>$0_B$ **DISABLED** Disables master/slave manual configuration value.<br>$1_B$ **ENABLED** Enables master/slave manual configuration value. |
| MS | 11 | RW | **Master/Slave Configuration Value**<br>Allows forcing of master or slave mode manually when AN_GCTRL.MSEN is set to $1_B$.<br>$0_B$ **SLAVE** Configures PHY as slave during master/slave negotiation.<br>$1_B$ **MASTER** Configures PHY as master during master/slave negotiation. |
| MSPT | 10 | RW | **Master/Slave Port Type**<br>Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function.<br>$0_B$ **SPD** Single-port device<br>$1_B$ **MPD** Multi-port device |
| MBTFD | 9 | RW | **1000BASE-T Full-Duplex**<br>Advertises the 1000BASE-T full-duplex capability; always forced to 1 in converter mode.<br>$0_B$ **DISABLED** Advertises PHY as not 1000BASE-T full-duplex capable<br>$1_B$ **ENABLED** Advertises PHY as 1000BASE-T full-duplex capable |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MBTHD | 8 | RW | **1000BASE-T Half-Duplex**<br>Always advertises the 1000BASE-T half-duplex capability as disabled. The GPHY does not support 1000BASE-T half-duplex capability.<br>$0_B$ **DISABLED** Advertises PHY as not 1000BASE-T half-duplex capable<br>$1_B$ **ENABLED** Advertises PHY as 1000BASE-T half-duplex capable |
| RES | 7:0 | RO | **Reserved**<br>Write as zero, ignore on read. |

The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

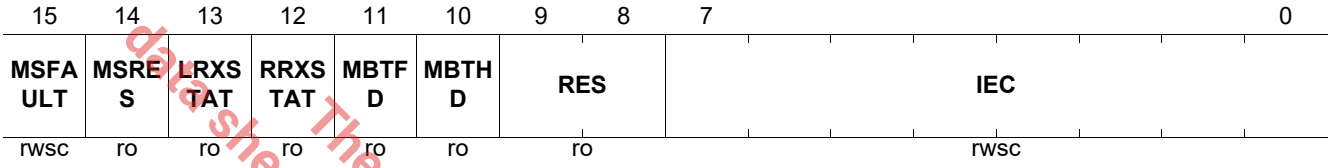
### Gigabit Status Register (Register 0.10)

This is the status register used to reflect the Gigabit Ethernet status of the PHY. Refer to IEEE 802.3-2022 40.5.1.1.

IEEE Standard Register=0.10

**STD_GSTAT** **Reset Value**

**Gigabit Status Register (Register 0.10)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| MSFAULT | 15 | RWSC | **Master/Slave Manual Configuration Fault**<br>This bit is set when the number of failed master-slave resolutions reaches 7. It is cleared upon each read of GSTAT.<br>This bit self clears on auto-negotiation enable or auto-negotiation complete.<br>$0_B$ **OK** Master/slave manual configuration resolved successfully<br>$1_B$ **NOK** Master/slave manual configuration resolved with a fault |
| MSRES | 14 | RO | **Master/Slave Configuration Resolution**<br>$0_B$ **SLAVE** Local PHY configuration resolved to SLAVE<br>$1_B$ **MASTER** Local PHY configuration resolved to MASTER |
| LRXSTAT | 13 | RO | **Local Receiver Status**<br>Indicates the status of the local receiver.<br>$0_B$ **NOK** Local receiver not OK<br>$1_B$ **OK** Local receiver OK |
| RRXSTAT | 12 | RO | **Remote Receiver Status**<br>Indicates the status of the remote receiver.<br>$0_B$ **NOK** Remote receiver not OK<br>$1_B$ **OK** Remote receiver OK |
| MBTFD | 11 | RO | **Link Partner Capable of Operating 1000BASE-T Full-Duplex**<br>$0_B$ **DISABLED** Link partner is not capable of operating 1000BASE-T full-duplex<br>$1_B$ **ENABLED** Link partner is capable of operating 1000BASE-T full-duplex |
| MBTHD | 10 | RO | **Link Partner Capable of Operating 1000BASE-T Half-Duplex**<br>$0_B$ **DISABLED** Link partner is not capable of operating 1000BASE-T half-duplex<br>$1_B$ **ENABLED** Link partner is capable of operating 1000BASE-T half-duplex |
| RES | 9:8 | RO | **Reserved**<br>Write as zero, ignore on read. |

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The product (or products) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| IEC | 7:0 | RWSC | **Idle Error Count**<br>Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver receives idles. |

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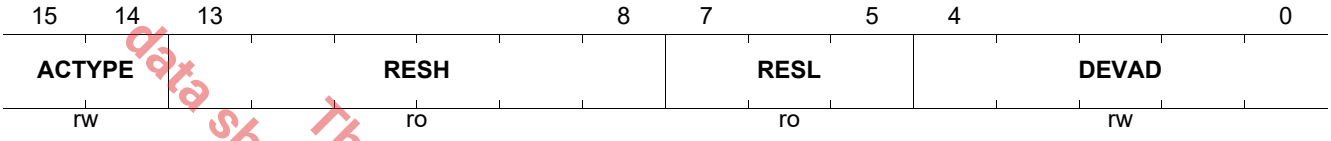
### MMD Access Control Register (Register 0.13)

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. This uses address directing as specified in IEEE 802.3 Clause 22 Extended.

IEEE Standard Register=0.13

**STD_MMDCTRL** **Reset Value**

**MMD Access Control Register (Register 0.13)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| ACTYPE | 15:14 | RW | **Access Type Function**<br>When the MMDDATA register is accessed via an address access (ACTYPE=0), the access is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD address register direct the MMDDATA register data accesses to the appropriate registers within that MMD.<br>$00_B$ **ADDRESS** Accesses to the MMDDATA register access the MMD individual address register.<br>$01_B$ **DATA** Accesses to the MMDDATA register access the register within the MMD selected.<br>$10_B$ **DATA_PI** Accesses to the MMDDATA register access the register within the MMD selected.<br>$11_B$ **DATA_PIWR** Accesses to the MMDDATA register access the register within the MMD selected. |
| RESH | 13:8 | RO | **Reserved**<br>Write as zero, ignored on read. |
| RESL | 7:5 | RO | **Reserved**<br>Write as zero, ignored on read. |
| DEVAD | 4:0 | RW | **Device Address**<br>The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 Clause 45.2. |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

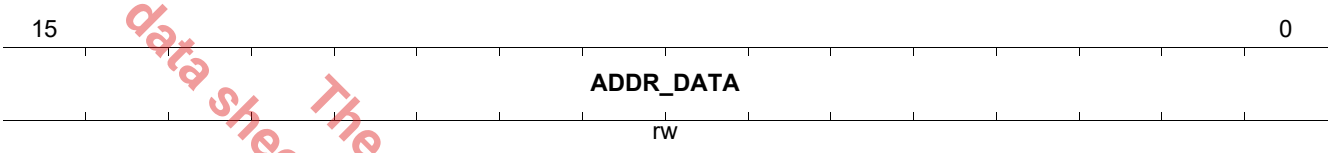
### MMD Access Data Register (Register 0.14)

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space. For more information on MMD access, refer to IEEE 802.3-2008 Clause 22.2.4.3.12, Clause 45.2, and Annex 22D.

IEEE Standard Register=0.14

**STD_MMDDATA** **Reset Value**

**MMD Access Data Register (Register 0.14)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| ADDR_DATA | 15:0 | RW | **Address or Data Register**<br>This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. The MMDCTRL register defines which function is currently valid. |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

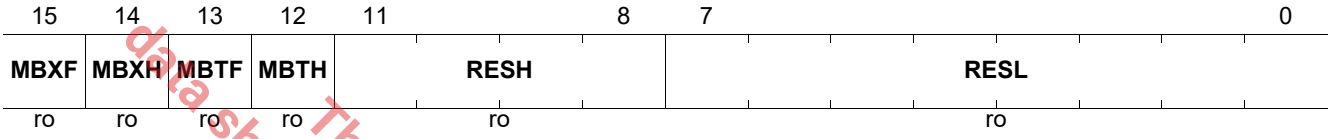
### Extended Status Register (Register 0.15)

This register contains extended status and capability information about the PHY. All the bits are read-only. A write access does not have any effect.

IEEE Standard Register=0.15

**STD_XSTAT** **Reset Value**

**Extended Status Register (Register 0.15)** **$2000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| MBXF | 15 | RO | **1000BASE-X Full-Duplex Capability**<br>Specifies whether the PHY is capable of operating 1000BASE-X full-duplex.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| MBXH | 14 | RO | **1000BASE-X Half-Duplex Capability**<br>Specifies whether the PHY is capable of operating 1000BASE-X half-duplex.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| MBTF | 13 | RO | **1000BASE-T Full-Duplex Capability**<br>Specifies whether the PHY is capable of operating 1000BASE-T full-duplex.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| MBTH | 12 | RO | **1000BASE-T Half-Duplex Capability**<br>GPHY do not support 1000BASE-T half-duplex capability.<br>$0_B$ **DISABLED** PHY does not support this mode.<br>$1_B$ **ENABLED** PHY supports this mode. |
| RESH | 11:8 | RO | **Reserved**<br>Ignore when read. |
| RESL | 7:0 | RO | **Reserved**<br>Ignore when read. |

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## 5.2 PHY-specific Management Registers

This section describes the PHY-specific management registers in device 0.

**Table 29 Registers Overview- PHY-specific Management Registers**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| PHY_STAT1 | Physical Layer Status 1 (Register 0.17) | $000C_H$ |
| PHY_CTL1 | Physical Layer Control 1 (Register 0.19) | $0001_H$ |
| PHY_CTL2 | Physical Layer Control 2 (Register 0.20) | $0006_H$ |
| PHY_ERRCNT | Error Counter (Register 0.21) | $0000_H$ |
| PHY_MIISTAT | Media-Independent Interface Status (Register 0.24) | $0000_H$ |
| PHY_IMASK | Interrupt Mask Register (Register 0.25) | $0000_H$ |
| PHY_ISTAT | Interrupt Status Register (Register 0.26) | $0000_H$ |
| PHY_LED | LED Control Register (Register 0.27) | $FF00_H$ |
| PHY_TPGCTRL | Test-Packet Generator Control (Register 0.28) | $0000_H$ |
| PHY_TPGDATA | Test-Packet Generator Data (Register 0.29) | $00AA_H$ |
| PHY_FWV | Firmware Version Register (Register 0.30) | $0000_H$ |

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### 5.2.1 PHY-specific Management Register Descriptions

This section describes all the PHY registers in detail.

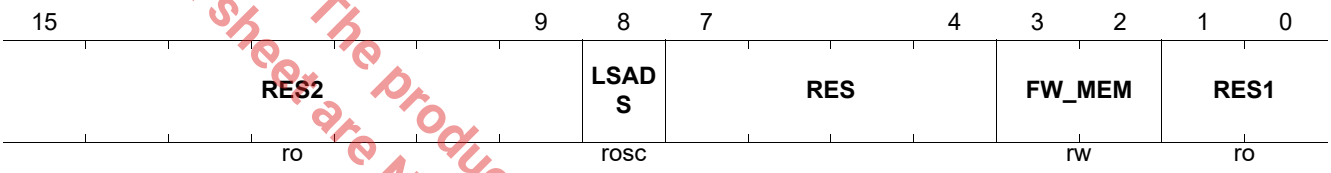
#### Physical Layer Status 1 (Register 0.17)

This register reports PHY link information, for example link-up, polarity reversals, and port mapping. The content of this register is only valid when the link is up.

IEEE Standard Register=0.17

**PHY_STAT1** **Reset Value**

**Physical Layer Status 1 (Register 0.17)** **$000C_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES2 | 15:9 | RO | **Reserved**<br>Write as zero, ignored on read. |
| LSADS | 8 | ROSC | **Link Speed Auto-Downspeed Status**<br>Monitors the status of the Auto-Downspeed (ADS).<br>$0_B$ **NORMAL** Did not perform any link speed ADS.<br>$1_B$ **DETECTED** Detected an ADS. |
| FW_MEM | 3:2 | RW | **Firmware Memory Location**<br>Indicates memory target used for firmware execution.<br>$11_B$ **RAM** Firmware is executed from SRAM.<br>Others: Reserved. |
| RES1 | 1:0 | RO | **Reserved**<br>Write as zero, ignored on read. |

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The product (or products) mentioned in this

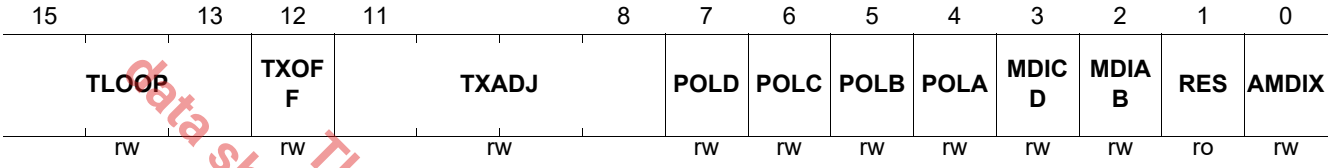
**Physical Layer Control 1 (Register 0.19)**

This register controls the PHY functions.

IEEE Standard Register=0.19

**PHY_CTL1** **Reset Value**

**Physical Layer Control 1 (Register 0.19)** **$0001_H$**




data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| TLOOP | 15:13 | RW | **Test Loop**<br>Configures predefined test loops.<br>$000_B$ **OFF** Test loops are switched off - normal operation.<br>$001_B$ **NETL** Near-end test loop<br>$010_B$ **FETL** Far-end test loop.<br>$100_B$ **RJTL** RJ45 connector test loop.<br>$101_B$ **FETLS** Standalone far-end test loop. No dependency on GMII_TX_CLK and GMII_RX_CLK.<br>Others: Reserved. |
| TXOFF | 12 | RW | **Transmitter Off**<br>This register bit turns the transmitter off.<br>This feature is used for return loss measurements.<br>$0_B$ **ON** Transmitter is on.<br>$1_B$ **OFF** Transmitter is off. |
| TXADJ | 11:8 | RW | **Transmit Level Adjustment**<br>Reserved. |
| POLD | 7 | RW | **Polarity Inversion Control on Port D**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |
| POLC | 6 | RW | **Polarity Inversion Control on Port C**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |
| POLB | 5 | RW | **Polarity Inversion Control on Port B**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |
| POLA | 4 | RW | **Polarity Inversion Control on Port A**<br>$0_B$ **NORMAL** Polarity normal<br>$1_B$ **INVERTED** Polarity inversion |
| MDICD | 3 | RW | **Mapping of MDI Ports C and D**<br>Used when Auto-MDIX is OFF to force the MDIX cable crossover configuration.<br>$0_B$ **MDI** Normal MDI mode<br>$1_B$ **MDIX** Crossover MDI-X mode |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MDIAB | 2 | RW | **Mapping of MDI Ports A and B**<br>Used when Auto-MDIX is OFF to force the MDIX cable crossover configuration.<br>$0_B$ **MDI** Normal MDI mode<br>$1_B$ **MDIX** Crossover MDI-X mode |
| RES | 1 | RO | **Reserved** |
| AMDIX | 0 | RW | **PHY Performs Auto-MDI/MDI-X or Uses Manual MDI/MDI-X**<br>$0_B$ **MANUAL** PHY uses manual MDI/MDI-X.<br>$1_B$ **AUTO** PHY performs Auto-MDI/MDI-X. |

The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

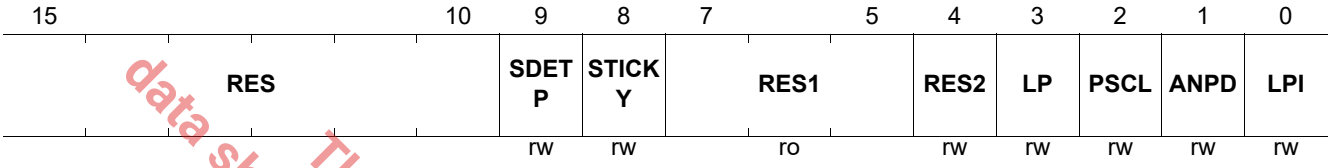
**Physical Layer Control 2 (Register 0.20)**

This register controls the PHY functions.

IEEE Standard Register=0.20

**PHY_CTL2** **Reset Value**

**Physical Layer Control 2 (Register 0.20)** **$0006_H$**




data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| SDETP | 9 | RW | **Signal Detection Polarity for the 1000BASE-X PHY**<br>This field is reserved because 1000BASE-X is not supported on this PHY port. |
| STICKY | 8 | RW | **Sticky-Bit Handling**<br>Setting this bit to $1_B$ ensures that all the vendor specific registers (of type RW) in the PHY (device 0), VSPEC1 (device 30), and VSPEC2 (device 31) are not changed during a MDIO reset or software reset of the GPHY. This allows the STA to keep the configurations chosen before reset.<br>$0_B$ **OFF** Sticky-bit handling is disabled.<br>$1_B$ **ON** Sticky-bit handling is enabled. |
| RES1 | 7:5 | RO | **Reserved**<br>Write as zero, ignored on read. |
| RES2 | 4 | RW | **Reserved** |
| LP | 3 | RW | **Low Power Mode**<br>Low Power Mode (LP) allows the GPHY to save energy by disabling most of the digital logic to reduce power consumption to its lowest level. The entry to LP is triggered when the PHY does not sense any energy on the cable and no link pulses (NLP, FLP, Beacons) are received. After spending VSPEC1_NBT_DS_CTRL.NRG_RST_CNT without energy in the ABILITY_DETECT state defined by IEEE 802.3 Clause 28, and after the timer defined VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM expired, the PHY enters LP.<br>$0_B$ **OFF** LP is disabled. The GPHY does not enter LP.<br>$1_B$ **ON** LP is enabled. The GPHY enters LP when no energy is sensed. |
| PSCL | 2 | RW | **Power Consumption Scaling Depending on Link Quality**<br>Allows enabling/disabling of the power consumption scaling depending on the link quality.<br>$0_B$ **OFF** PSCL is disabled.<br>$1_B$ **ON** PSCL is enabled. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ANPD | 1 | RW | **Auto-Negotiation Power Down**<br>Allows enabling/disabling of the power down modes during auto-negotiation looking for a link partner.<br>$0_B$ **OFF** ANPD is disabled.<br>$1_B$ **ON** ANPD is enabled. |
| LPI | 0 | RW | **Assert LPI via MDIO**<br>Controls assertion/de-assertion of the LPI by the MDIO instead of following the (X)GMII LPI.<br>Used to force the EEE on the TPI (ignoring the LPI indication from MAC).<br>$0_B$ **DE-ASSERT** LPI is de-asserted on TPI.<br>$1_B$ **ASSERT** LPI is asserted on TPI. |

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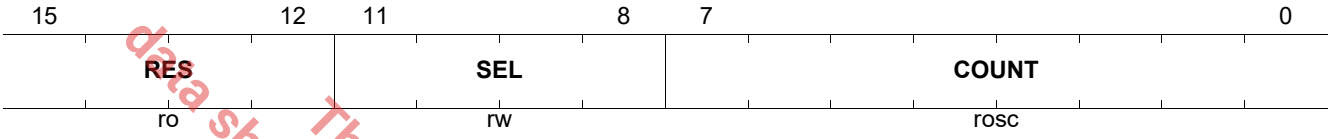
### Error Counter (Register 0.21)

This register controls the error counter. It allows the number of errors detected in the PHY to be counted for monitoring purposes.

IEEE Standard Register=0.21

**PHY_ERRCNT** **Reset Value**

**Error Counter (Register 0.21)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Write as zero, ignored on read. |
| SEL | 11:8 | RW | **Select Error Event**<br>Configures which error type the error counter counts:<br>$0000_B$**RXERR** Receive errors are counted.<br>$0001_B$**RXACT** Receive frames are counted.<br>$0010_B$**ESDERR** ESD errors are counted.<br>$0011_B$**SSDERR** SSD errors are counted.<br>$0100_B$**TXERR** Transmit errors are counted.<br>$0101_B$**TXACT** Transmit frames events are counted.<br>$0110_B$**COL** Collision events are counted.<br>$1000_B$**NLD** Number of Link Down events are counted.<br>$1001_B$**NDS** Number of ADS events are counted.<br>$1010_B$**RES** Reserved<br>$1011_B$**RES** Reserved |
| COUNT | 7:0 | ROSC | **Counter Value**<br>This counter value is updated each time the selected error event is detected. The counter value is reset every time a read operation on this register is performed or the error event is changed. The counter saturates at value $FF_H$. |

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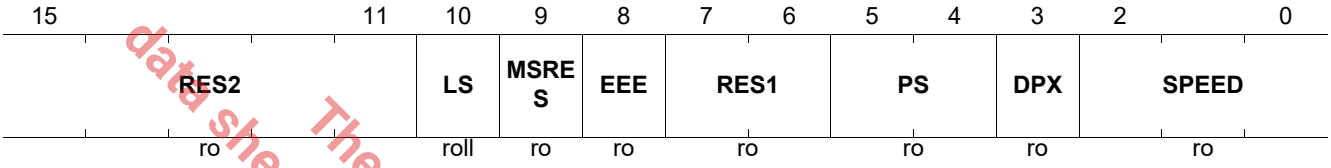
### Media-Independent Interface Status (Register 0.24)

This register contains status information on the Ethernet link, concatenated in a single register to allow concise status read by the STA in a single register.

IEEE Standard Register=0.24

**PHY_MIISTAT** **Reset Value**

**Media-Independent Interface Status (Register 0.24)** **$0000_H$**




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| Field | Bits | Type | Description |
|---|---|---|---|
| RES2 | 15:11 | RO | **Reserved**<br>Write as zero, ignored on read. |
| LS | 10 | ROLL | **Link Status of GPHY Ethernet PHY Operation**<br>Indicates the link status of the PHY.<br>$0_B$ **INACTIVE** The link is down. No communication with link partner possible.<br>$1_B$ **ACTIVE** The link is up. Data communication with link partner is possible. |
| MSRES | 9 | RO | **Master/Slave Configuration**<br>Indicates the master/slave configuration<br>$0_B$ **SLAVE** Local PHY configuration is SLAVE after ANEG.<br>$1_B$ **MASTER** Local PHY configuration is MASTER after ANEG. |
| EEE | 8 | RO | **Energy-Efficient Ethernet Mode**<br>$0_B$ **OFF** EEE is disabled after ANEG resolution.<br>$1_B$ **ON** EEE is enabled after ANEG resolution. |
| RES1 | 7:6 | RO | **Reserved** |
| PS | 5:4 | RO | **Pause Status for Flow Control**<br>$00_B$ **NONE** No PAUSE<br>$01_B$ **TX** Transmit PAUSE<br>$10_B$ **RX** Receive PAUSE<br>$11_B$ **TXRX** Both transmit and receive PAUSE |
| DPX | 3 | RO | **GPHY Ethernet PHY Duplex Mode**<br>$0_B$ **HDX** Half-duplex<br>$1_B$ **FDX** Full-duplex |
| SPEED | 2:0 | RO | **GPHY Ethernet PHY Speed**<br>$000_B$ **TEN** 10 Mbps<br>$001_B$ **FAST** 100 Mbps<br>$010_B$ **GIGA** 1000 Mbps<br>$011_B$ **ANEG** Auto-negotiation mode<br>$100_B$ **BZ2G5** 2.5 Gbps |

### Interrupt Mask Register (Register 0.25)

This register defines the mask for the Interrupt Status Register (ISTAT), which contains the event source for the MDINT interrupt sent from the GPHY to an external chip.

The information about the interrupt source is indicated in the ISTAT register.

IEEE Standard Register=0.25

**PHY_IMASK** **Reset Value**

**Interrupt Mask Register (Register 0.25)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **WOL** | **MSRE** | **NPRX** | **NPTX** | **ANE** | **ANC** | **RES** | **RES** | **LP** | **TEMP** | **ADSC** | **MDIPC** | **MDIXC** | **DXMC** | **LSPC** | **LSTC** |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

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| Field | Bits | Type | Description |
|---|---|---|---|
| WOL | 15 | RW | **Wake-on-LAN Event Mask**<br>When active and masked in IMASK, the MDINT is activated upon detection of a valid WoL event.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| MSRE | 14 | RW | **Master/Slave Resolution Error Mask**<br>When active, MDINT is activated upon detection of a master/slave resolution error (MSRE) during a 1000BASE-T ANEG.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| NPRX | 13 | RW | **Next Page Received Mask**<br>When active, MDINT is activated upon reception of a next page in STD_AN_NPRX.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| NPTX | 12 | RW | **Next Page Transmitted Mask**<br>When active, MDINT is activated upon transmission of the currently stored next page in STD_AN_NPTX.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| ANE | 11 | RW | **Auto-Negotiation Error Mask**<br>When active, MDINT is activated upon detection of an ANEG error.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| ANC | 10 | RW | **Auto-Negotiation Complete Mask**<br>When active, MDINT is activated upon completion of the ANEG process.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LP | 7 | RW | **LP Entry Indication Mask**<br>$0_B$ **INACTIVE** Interrupt is masked out. The STA does not need to be informed of the event.<br>$1_B$ **ACTIVE** Interrupt is activated. The STA receives MDINT when the PHY is about to enter LP. |
| TEMP | 6 | RW | **TEMP**<br>$0_B$ **INACTIVE** Interrupt is masked out. The STA does not need to be informed of the event.<br>$1_B$ **ACTIVE** Interrupt is activated. The interrupt is triggered when the temperature goes beyond the normal operating range. |
| ADSC | 5 | RW | **Link Speed Auto-Downspeed Detect Mask**<br>When active, MDINT is activated upon detection of a link speed ADS event.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| MDIPC | 4 | RW | **MDI Polarity Change Detect Mask**<br>When active, MDINT is activated upon detection of an MDI polarity change event.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| MDIXC | 3 | RW | **MDIX Change Detect Mask**<br>When active, MDINT is activated upon detection of an MDI/MDIX cross-over change event.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| DXMC | 2 | RW | **Duplex Mode Change Mask**<br>When active, MDINT is activated upon detection of full or half-duplex change.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| LSPC | 1 | RW | **Link Speed Change Mask**<br>When active, MDINT is activated upon detection of link speed change.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |
| LSTC | 0 | RW | **Link State Change Mask**<br>When active, MDINT is activated upon detection of link status change.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |

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**Interrupt Status Register (Register 0.26)**

This register defines the event source for the MDINT interrupt sent from the GPHY to an external chip.

PHY_ISTAT is a cleared on read by the STA.

IEEE Standard Register=0.26

**PHY_ISTAT** **Reset Value**

**Interrupt Status Register (Register 0.26)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **WOL** | **MSRE** | **NPRX** | **NPTX** | **ANE** | **ANC** | **RES** | **RES** | **LP** | **TEMP** | **ADSC** | **MDIPC** | **MDIXC** | **DXMC** | **LSPC** | **LSTC** |
| rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc | rosc |

| Field | Bits | Type | Description |
|---|---|---|---|
| WOL | 15 | ROSC | **Wake-on-LAN Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of a valid WoL event.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The WoL event is the source of the interrupt. |
| MSRE | 14 | ROSC | **Master/Slave Resolution Error Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of a MSRE during a 1000BASE-T ANEG.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The MSRE event is the source of the interrupt. |
| NPRX | 13 | ROSC | **Next Page Received Interrupt Status**<br>When this bit is set, the MDINT is activated upon reception of a next page in STD_AN_NPRX.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The NPRX event is the source of the interrupt. |
| NPTX | 12 | ROSC | **Next Page Transmitted Interrupt Status**<br>When this bit is set, the MDINT is activated upon transmission of the currently stored next page in STD_AN_NPTX.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The NPTX event is the source of the interrupt. |
| ANE | 11 | ROSC | **Auto-Negotiation Error Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of an ANEG error.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The ANEG error event is the source of the interrupt. |
| ANC | 10 | ROSC | **Auto-Negotiation Complete Interrupt Status**<br>When this bit is set, the MDINT is activated upon completion of the ANEG process.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The ANEG complete event is the source of the interrupt. |

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The product (or products) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LP | 7 | ROSC | **LP Entry Indication**<br>$0_B$ **INACTIVE** No indication of LP entry<br>$1_B$ **ACTIVE** Indication of LP entry. |
| TEMP | 6 | ROSC | **TEMP**<br>Indicates that thermal mitigation action must be taken when the temperature goes beyond the normal operating range. The GPHY implements ADS by default when this happens, but it is possible to disable ADS. When the SoC disables ADS, it is recommended that the SoC initiates a link down and changes the speed capability to cool the device back to the normal temperature range. When the temperature reaches the maximum absolute rating, the device resets for safety purposes. Thermal mitigation must ensure that the maximum absolute temperature limits are never reached.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The TEMP change event is the source of the interrupt. |
| ADSC | 5 | ROSC | **Link Speed Auto-Downspeed Detect Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of a link speed ADS event.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The ADSC change event is the source of the interrupt. |
| MDIPC | 4 | ROSC | **MDI Polarity Change Detect Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of an MDI polarity change event.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The MDIPC change event is the source of the interrupt. |
| MDIXC | 3 | ROSC | **MDIX Change Detect Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of an MDI/MDIX cross-over change event.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The MDIX change event is the source of the interrupt. |
| DXMC | 2 | ROSC | **Duplex Mode Change Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of a full or half-duplex change.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The DXMC change event is the source of the interrupt. |
| LSPC | 1 | ROSC | **Link Speed Change Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of link speed change.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The LSPC change event is the source of the interrupt. |
| LSTC | 0 | ROSC | **Link State Change Interrupt Status**<br>When this bit is set, the MDINT is activated upon detection of link status change.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The LSTC change event is the source of the interrupt. |

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### LED Control Register (Register 0.27)

This register contains the control bits for direct access to the LEDs by setting the on/off LEDxDA bits (where x is from 0 to 2).

To directly control the LED, the integrated LED functions must be disabled by the LEDxEN bit in this register.

The integrated LED functions are specified in the more sophisticated LED control registers in the MMD device VSPEC1.

IEEE Standard Register=0.27

**PHY_LED** **Reset Value**

**LED Control Register (Register 0.27)** **$FF00_H$**

| 15 | 12 | 11 | 10 | 9 | 8 | 7 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | RES | LED2EN | LED1EN | LED0EN | RES1 | | RES | LED2DA | LED1DA | LED0DA |
| rw | | rw | rw | rw | rw | ro | | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RW | **Reserved**<br>The default value must not be changed. |
| LED2EN | 10 | RW | **Enable Integrated Function of LED2**<br>Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED2DA.<br>$0_B$ **DISABLE** Disables the integrated LED function.<br>$1_B$ **ENABLE** Enables the integrated LED function. |
| LED1EN | 9 | RW | **Enable Integrated Function of LED1**<br>Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED1DA.<br>$0_B$ **DISABLE** Disables the integrated LED function.<br>$1_B$ **ENABLE** Enables the integrated LED function. |
| LED0EN | 8 | RW | **Enable Integrated Function of LED0**<br>Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED0DA.<br>$0_B$ **DISABLE** Disables the integrated LED function.<br>$1_B$ **ENABLE** Enables the integrated LED function. |
| RES1 | 7:4 | RO | **Reserved**<br>Write as zero, ignored on read. |
| LED2DA | 2 | RW | **Direct Access to LED2**<br>Write a 1 to this bit to illuminate the LED. LED2EN must be set to zero.<br>$0_B$ **OFF** Switch off the LED.<br>$1_B$ **ON** Switch on the LED. |
| LED1DA | 1 | RW | **Direct Access to LED1**<br>Write a 1 to this bit to illuminate the LED. LED1EN must be set to zero.<br>$0_B$ **OFF** Switch off the LED.<br>$1_B$ **ON** Switch on the LED. |

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| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LED0DA | 0 | RW | **Direct Access to LED0**<br>Write a 1 to this bit to illuminate the LED. LED0EN must be set to zero.<br>$0_B$ **OFF** Switch off the LED.<br>$1_B$ **ON** Switch on the LED. |

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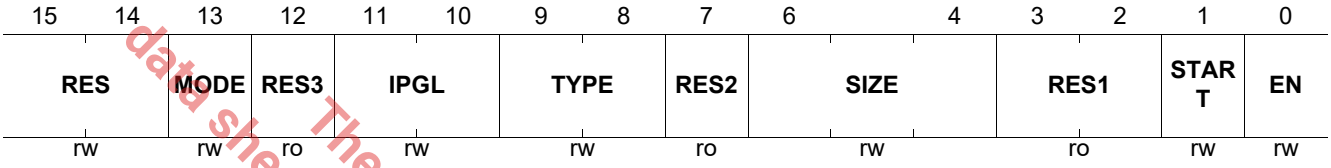
### Test-Packet Generator Control (Register 0.28)

This register controls the operation of the integrated Test-Packet Generator (TPG). This module is only used for testing purposes.

IEEE Standard Register=0.28

**PHY_TPGCTRL** **Reset Value**

**Test-Packet Generator Control (Register 0.28)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:14 | RW | **Reserved**<br>Write as zero, ignore on read. |
| MODE | 13 | RW | **TPG Mode**<br>Configures the packet generation mode.<br>$0_B$ **CONTINUOUS** Sends packets continuously.<br>$1_B$ **SINGLE** Sends a single packet. |
| RES3 | 12 | RO | **Reserved**<br>Write as zero, ignore on read. |
| IPGL | 11:10 | RW | **Inter-Packet Gap Length**<br>Configures the length of the inter-packet gap in bit times.<br>$00_B$ **RES** Reserved<br>$01_B$ **BT96** Length is 96 bit times<br>$10_B$ **BT960** Length is 960 bit times<br>$11_B$ **BT9600** Length is 9600 bit times |
| TYPE | 9:8 | RW | **Packet Data Type**<br>Configures the packet data type to be either predefined, byte increment, or random. When predefined, the content of the register TPGDATA is used.<br>$00_B$ **RANDOM** Uses random data as the packet content.<br>$01_B$ **BYTEINC** Uses byte increment as the packet content.<br>$10_B$ **PREDEF** Uses predefined content of the register TPGDATA.<br>$11_B$ **RES** Reserved. |
| RES2 | 7 | RO | **Reserved.**<br>Write as zero, ignore on read. |

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| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SIZE | 6:4 | RW | **Packet Size**<br>Configures the size of the generated Ethernet packets in bytes. The size includes DA, SA, length/type, payload, and FCS.<br>$000_B$ **B64** Packet length is 64 bytes<br>$001_B$ **B2048** Packet length is 2048 bytes<br>$010_B$ **B256** Packet length is 256 bytes<br>$011_B$ **B4096** Packet length is 4096 bytes<br>$100_B$ **B1024** Packet length is 1024 bytes<br>$101_B$ **B1518** Packet length is 1518 bytes<br>$110_B$ **B9000** Packet length is 9000 bytes |
| RES1 | 3:2 | RO | **Reserved**<br>Write as zero, ignore on read. |
| START | 1 | RW | **Start or Stop TPG Data Generation.**<br>Starts the TPG data generation. Depending on the MODE, the TPG sends only one packet or chunks of 10000 packets until stopped.<br>$0_B$ **STOP** Stops the TPG data generation.<br>$1_B$ **START** Starts the TPG data generation. |
| EN | 0 | RW | **Enable the TPG**<br>Enables the TPG for data generation.<br>$0_B$ **DISABLE** Disables the TPG<br>$1_B$ **ENABLE** Enables the TPG |

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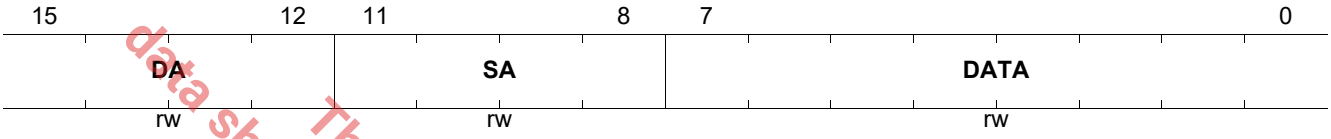
### Test-Packet Generator Data (Register 0.29)

Specifies the payload data to be used when sending a non-random data packet. All payload data bytes are sent with this value.

IEEE Standard Register=0.29

**PHY_TPGDATA** **Reset Value**

**Test-Packet Generator Data (Register 0.29)** **$00AA_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| DA | 15:12 | RW | **Destination Address**<br>Configures the destination address nibble. The destination address builds up to 00-03-19-FF-FF-F[DA]. |
| SA | 11:8 | RW | **Source Address**<br>Configures the source address nibble. The source address builds up to 00-03-19-FF-FF-F[SA]. |
| DATA | 7:0 | RW | **Data Byte to be Transmitted**<br>This is the content of the payload bytes in the frame to send constant data. The bit masks are shown here. For configuration details, refer to the corresponding chapter.<br>$80_H$ **PREC** Selects whether to take full precision (1) or reduced precision (0) at bit 7<br>$60_H$ **PREC2** For reduced precision, selects the options with bits [6:5]<br>$10_H$ **RESERVED** Reserved |

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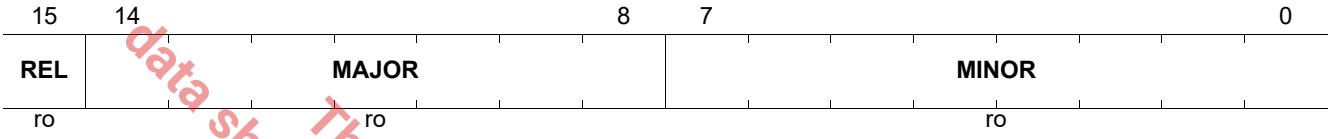
### Firmware Version Register (Register 0.30)

This register contains the version of the PHY firmware. The firmware initializes the version number at boot time with its current software version. This register is read-only by the external STA.

IEEE Standard Register=0.30

**PHY_FWV** **Reset Value**

**Firmware Version Register (Register 0.30)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| REL | 15 | RO | **Release Indication**<br>This parameter indicates either a test or a release version.<br>$0_B$ **TEST** Indicates a test version.<br>$1_B$ **RELEASE** Indicates a released version. |
| MAJOR | 14:8 | RO | **Major Version Number**<br>Specifies the main version release number of the firmware. |
| MINOR | 7:0 | RO | **Minor Version Number**<br>Specifies the sub-version release number of the firmware. |

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# 6 PHY MMD Registers Detailed Description

**Table 30 Register Access Type**

| Mode | Symbol |
|---|---|
| Status Register (Status or Ability Register) | RO |
| Read-Write Register (MDIO Register) | RW |
| Read-Write Self-Clearing Register (bit is cleared after read from MDIO) | RWSC |
| Read-Only Self-Clearing Register (bit is cleared after read from MDIO) | ROSC |

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## 6.1 Standard PMAPMD Registers for MMD=0x01

**Table 31 Registers Overview- Standard PMAPMD Registers**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| PMA_CTRL1 | PMA/PMD Control 1 (Register 1.0) | $2058_H$ |
| PMA_STAT1 | PMA/PMD Status 1 (Register 1.1) | $0000_H$ |
| PMA_DEVID1 | PHY Identifier 1 (Register 1.2) | $C133_H$ |
| PMA_DEVID2 | PHY Identifier 2 (Register 1.3) | $5400_H$ 1) |
| PMA_SPEED_ABILITY | PMA/PMD Speed Ability (Register 1.4) | $2070_H$ |
| PMA_DIP1 | Devices in Package 1 (Register 1.5) | $008B_H$ |
| PMA_DIP2 | Devices in Package 2 (Register 1.6) | $C000_H$ |
| PMA_CTL2 | PMA/PMD Control 2 (Register 1.7) | $0030_H$ |
| PMA_STAT2 | PMA/PMD Status 2 (Register 1.8) | $8200_H$ |
| PMA_EXT_ABILITY | PMA/PMD Extended Ability (Register 1.11) | $41A0_H$ |
| PMA_PACKID1 | AN Package Identifier (Register 1.14) | $C133_H$ |
| PMA_PACKID2 | AN Package Identifier (Register 1.15) | $5400_H$ 1) |
| PMA_MGBT_EXTAB | PMAPMD Extended Ability (Register 1.21) | $0001_H$ |
| PMA_MGBT_STAT | MULTIGBASE-T Status (Register 1.129) | $0000_H$ |
| PMA_MGBT_POLARITY | MULTIGBASE-T Pair Swap and Polarity (Register 1.130) | $0003_H$ |
| PMA_MGBT_TX_PBO | MULTIGBASE-T Tx Power Backoff and PHY Short Reach Setting (Register 1.131) | $0000_H$ |
| PMA_MGBT_TEST_MODE | MULTIGBASE-T Test Mode (Register 1.132) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_A | MULTIGBASE-T SNR Margin Channel A (Register 1.133) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_B | MULTIGBASE-T SNR Margin Channel B (Register 1.134) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_C | MULTIGBASE-T SNR Margin Channel C (Register 1.135) | $0000_H$ |
| PMA_MGBT_SNR_OPMARGIN_D | MULTIGBASE-T SNR Margin Channel D (Register 1.136) | $0000_H$ |
| PMA_MGBT_MINMARGIN_A | MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137) | $0000_H$ |
| PMA_MGBT_MINMARGIN_B | MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138) | $0000_H$ |
| PMA_MGBT_MINMARGIN_C | MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139) | $0000_H$ |
| PMA_MGBT_MINMARGIN_D | MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140) | $0000_H$ |
| PMA_MGBT_POWER_A | MULTIGBASE-T Rx Power Channel A (Register 1.141) | $0000_H$ |
| PMA_MGBT_POWER_B | MULTIGBASE-T Rx Power Channel B (Register 1.142) | $0000_H$ |
| PMA_MGBT_POWER_C | MULTIGBASE-T Rx Power Chan C (Register 1.143) | $0000_H$ |
| PMA_MGBT_POWER_D | MULTIGBASE-T Rx Power Chan D (Register 1.144) | $0000_H$ |
| PMA_MGBT_SKEW_DELAY_0 | MULTIGBASE-T Skew Delay 0 (Register 1.145) | $0000_H$ |
| PMA_MGBT_SKEW_DELAY_1 | MULTIGBASE-T Skew Delay 1 (Register 1.146) | $0000_H$ |

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**Table 31 Registers Overview- Standard PMAPMD Registers** (cont'd)

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| PMA_MGBT_FAST_RETRAIN_STA_CTRL | MULTIGBASE-T Skew Delay 2 (Register 1.147) | $0010_H$ |
| PMA_TIMESYNC_CAP | PMA TimeSync Capability Indication (Register 1.1800) | $0000_H$ |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

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### 6.1.1 PMAPMD Register Descriptions

This section describes all the PMAPMD registers in detail.

**PMA/PMD Control 1 (Register 1.0)**

IEEE Standard Register=1.0

**PMA_CTRL1** **Reset Value**

**PMA/PMD Control 1 (Register 1.0)** **$2058_H$**

| 15 | 14 | 13 | 12 | 11 | 10 ... 7 | 6 | 5 ... 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| **RST** | **RES** | **SSL** | **RES** | **LOW_POW*** | **RES** | **SSM** | **SPEED_SEL** | **NS1** | **NS2** |
| rw | | rw | | rw | | rw | rw | ro | ro |

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| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RW | **Reset**<br>$0_B$ Normal operation<br>$1_B$ PMA/PMD reset |
| SSL | 13 | RW | **Speed Selection (LSB)**<br>Used in conjunction with field SPEED_SEL_MSB.<br>MSB LSB:<br>$00_B$ 10 Mbps<br>$01_B$ 100 Mbps<br>$10_B$ 1000 Mbps<br>$11_B$ Bits [5:2] select the speed (SPEED_SEL field) |
| LOW_POWER | 11 | RW | **Low Power**<br>$0_B$ Normal operation<br>$1_B$ Enters low power mode. |
| SSM | 6 | RW | **Speed Selection (MSB)**<br>Used in conjunction with field SPEED_SEL_LSB.<br>MSB LSB:<br>$00_B$ 10 Mbps<br>$01_B$ 100 Mbps<br>$10_B$ 1000 Mbps<br>$11_B$ Bits [5:2] select the speed (SPEED_SEL field) |
| SPEED_SEL | 5:2 | RW | **Speed Selection**<br>Bit usage (from bit 5 to bit 2):<br>0 0 0 $0_B$ Not supported. The speed defaults to 2.5 Gbps.<br>0 0 0 $1_B$ Not supported. The speed defaults to 2.5 Gbps.<br>0 0 1 $0_B$ Not supported. The speed defaults to 2.5 Gbps.<br>0 0 1 $1_B$ Not supported. The speed defaults to 2.5 Gbps.<br>0 1 0 $0_B$ Not supported. The speed defaults to 2.5 Gbps.<br>0 1 0 $1_B$ Not supported. The speed defaults to 2.5 Gbps.<br>0 1 1 $0_B$ 2.5 Gbps<br>0 1 1 $1_B$ Not supported<br>1 x x $x_B$ Reserved |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| NS1 | 1 | RO | **Not Supported**<br>PMA remote loopback mode is not supported by the GPHY. |
| NS2 | 0 | RO | **Not Supported**<br>PMA local loopback mode is not supported by the GPHY. |

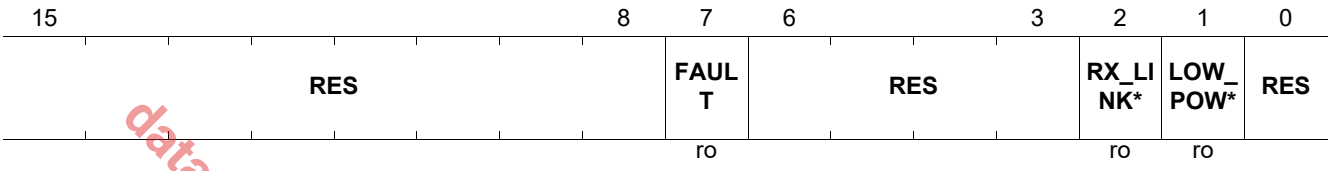
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**PMA/PMD Status 1 (Register 1.1)**

IEEE Standard Register=1.1

**PMA_STAT1** **Reset Value**

**PMA/PMD Status 1 (Register 1.1)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| FAULT | 7 | RO | **Fault**<br>$0_B$ Fault condition not detected<br>$1_B$ Fault condition detected |
| RX_LINK_STATUS | 2 | RO | **Receive Link Status**<br>$0_B$ PMA/PMD receive link down<br>$1_B$ PMA/PMD receive link up |
| LOW_POWER_ABILITY | 1 | RO | **Low Power Ability**<br>$0_B$ PMA/PMD does not support low power mode.<br>$1_B$ PMA/PMD supports low power mode. |

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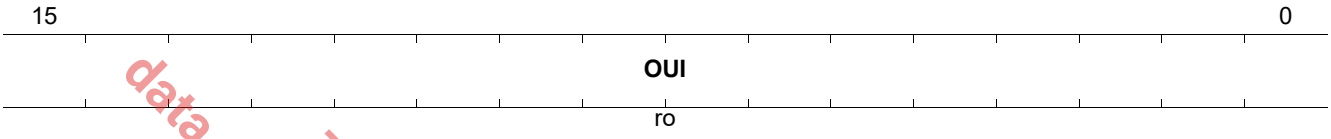
**PHY Identifier 1 (Register 1.2)**

IEEE Standard Register=1.2

Bits 31 - 16 of device ID

**PMA_DEVID1** **Reset Value**

**PHY Identifier 1 (Register 1.2)** **C133$_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier**<br>Organizationally Unique Identifier Bits 3:18 |

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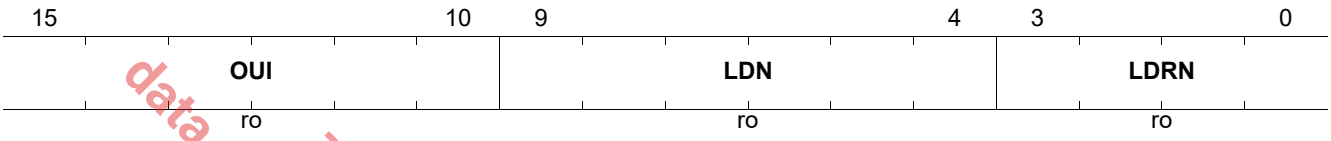
**PHY Identifier 2 (Register 1.3)**

IEEE Standard Register=1.3

Bits 15 - 0 of device ID

**PMA_DEVID2** **Reset Value**

**PHY Identifier 2 (Register 1.3)** **$5400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1] to distinguish between several different products. |
| LDRN | 3:0 | RO | **Device Revision Number**<br>Specifies the device revision number[1] to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

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The product(s) mentioned in this

### PMA/PMD Speed Ability (Register 1.4)

IEEE Standard Register=1.4

**PMA_SPEED_ABILITY** **Reset Value**

**PMA/PMD Speed Ability (Register 1.4)** **$2070_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | CAP_5G | CAP_2G5 | RES2 | RES | | CAP_100G | CAP_40G | CAP_10_* | CAP_10M | CAP_100M | CAP_100* | RES | R10PASS* | CAP_2BA* | CAP_10G* |
| | ro | ro | ro | | | ro | ro | ro | ro | ro | ro | | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| CAP_5G | 14 | RO | **Not Supported**<br>$0_B$ PMA/PMD is not capable of operating as 5 Gbps.<br>$1_B$ PMA/PMD is capable of operating at 5 Gbps. |
| CAP_2G5 | 13 | RO | **2.5 G capable**<br>$0_B$ PMA/PMD is not capable of operating as 2.5 Gbps.<br>$1_B$ PMA/PMD is capable of operating at 2.5 Gbps. |
| RES2 | 12 | RO | **Reserved**<br>Value always 0 |
| CAP_100G | 9 | RO | **Not Supported**<br>$0_B$ PMA/PMD is not capable of operating as 100 Gbps.<br>$1_B$ PMA/PMD is capable of operating at 100 Gbps. |
| CAP_40G | 8 | RO | **Not Supported**<br>$0_B$ PMA/PMD is not capable of operating as 40 Gbps.<br>$1_B$ PMA/PMD is capable of operating at 40 Gbps. |
| CAP_10_1G | 7 | RO | **Not Supported**<br>$0_B$ PMA/PMD is not capable of operating at 10 Gbps downstream and 1 Gbps upstream.<br>$1_B$ PMA/PMD is capable of operating at 10 Gbps downstream and 1 Gbps upstream. |
| CAP_10M | 6 | RO | **10M capable**<br>$0_B$ PMA/PMD is not capable of operating as 10 Mbps.<br>$1_B$ PMA/PMD is capable of operating at 10 Mbps. |
| CAP_100M | 5 | RO | **100M capable**<br>$0_B$ PMA/PMD is not capable of operating as 100 Mbps.<br>$1_B$ PMA/PMD is capable of operating at 100 Mbps. |
| CAP_1000M | 4 | RO | **1000M capable**<br>$0_B$ PMA/PMD is not capable of operating as 1000 Mbps.<br>$1_B$ PMA/PMD is capable of operating at 1000 Mbps. |
| R10PASS_TS_CAPABLE | 2 | RO | **Not Supported**<br>$0_B$ PMA/PMD is not capable of operating as 10PASS-TS.<br>$1_B$ PMA/PMD is capable of operating as 10PASS-TS. |

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| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| CAP_2BASE_TL | 1 | RO | **Not Supported**<br>$0_B$ PMA/PMD is not capable of operating as 2BASE-TL.<br>$1_B$ PMA/PMD is capable of operating as 2BASE-TL. |
| CAP_10G_CAP | 0 | RO | **Not Supported**<br>$0_B$ PMA/PMD is not capable of operating at 10 Gbps.<br>$1_B$ PMA/PMD is capable of operating at 10 Gbps. |

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**Devices in Package 1 (Register 1.5)**

IEEE Standard Register=1.5

**PMA_DIP1** **Reset Value**

**Devices in Package 1 (Register 1.5)** **$008B_H$**

| 15 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | SEP_PMA* | SEP_PMA* | SEP_PMA* | SEP_PMA* | ANEG | TC | DTE_XS | PHY_XS | PCS | WIS | PMD_PMA | CLAUSE_* |
| ro | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Ignore on read |
| SEP_PMA_4 | 11 | RO | **Separate PMA (4)**<br>$0_B$ Separate PMA (4) not present in package<br>$1_B$ Separate PMA (4) present in package |
| SEP_PMA_3 | 10 | RO | **Separate PMA (3)**<br>$0_B$ Separate PMA (3) not present in package<br>$1_B$ Separate PMA (3) present in package |
| SEP_PMA_2 | 9 | RO | **Separate PMA (2)**<br>$0_B$ Separate PMA (2) not present in package<br>$1_B$ Separate PMA (2) present in package |
| SEP_PMA_1 | 8 | RO | **Separate PMA (1)**<br>$0_B$ Separate PMA (1) not present in package<br>$1_B$ Separate PMA (1) present in package |
| ANEG | 7 | RO | **Auto-Negotiation Present**<br>This bit is always set to $1_B$ in the GPHY.<br>$0_B$ ANEG not present in package<br>$1_B$ ANEG present in package |
| TC | 6 | RO | **TC Present**<br>$0_B$ TC not present in package<br>$1_B$ TC present in package |
| DTE_XS | 5 | RO | **DTE XS Present**<br>$0_B$ DTE XS not present in package<br>$1_B$ DTE XS present in package |
| PHY_XS | 4 | RO | **PHY XS Present**<br>$0_B$ PHY XS not present in package<br>$1_B$ PHY XS present in package |
| PCS | 3 | RO | **PCS Present**<br>This bit is always set to $1_B$ in the GPHY.<br>$0_B$ PCS not present in package<br>$1_B$ PCS present in package |

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The product(s) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| WIS | 2 | RO | **WIS Present**<br>$0_B$ WIS not present in package<br>$1_B$ WIS present in package |
| PMD_PMA | 1 | RO | **PMD/PMA Present**<br>This bit is always set to $1_B$ in the GPHY.<br>$0_B$ PMA/PMD not present in package<br>$1_B$ PMA/PMD present in package |
| CLAUSE_22 | 0 | RO | **Clause 22 Registers Present**<br>This bit is always set to $1_B$ in the GPHY.<br>$0_B$ Clause 22 registers not present in package<br>$1_B$ Clause 22 registers present in package |

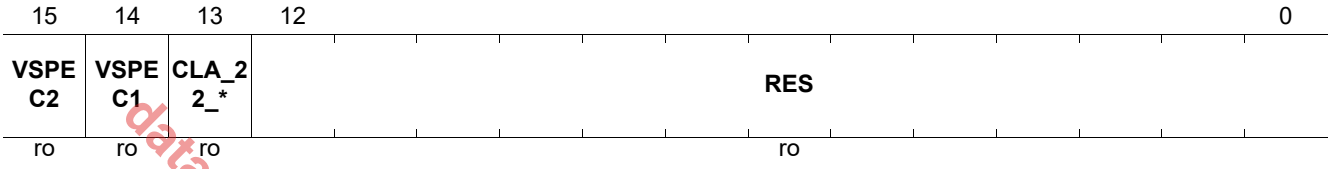
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### Devices in Package 2 (Register 1.6)

IEEE Standard Register=1.6

**PMA_DIP2** **Reset Value**

**Devices in Package 2 (Register 1.6)** **$C000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| VSPEC2 | 15 | RO | **Vendor-specific Device 2**<br>This bit is always set to $1_B$ in the GPHY.<br>$0_B$ Vendor-specific device 2 not present in package<br>$1_B$ Vendor-specific device 2 present in package |
| VSPEC1 | 14 | RO | **Vendor-specific Device 1**<br>This bit is always set to $1_B$ in the GPHY.<br>$0_B$ Vendor-specific device 1 not present in package<br>$1_B$ Vendor-specific device 1 present in package |
| CLA_22_EXT | 13 | RO | **Clause 22 Extension**<br>$0_B$ Clause 22 extension not present in package<br>$1_B$ Clause 22 extension present in package |
| RES | 12:0 | RO | **Reserved**<br>Ignore on read. |

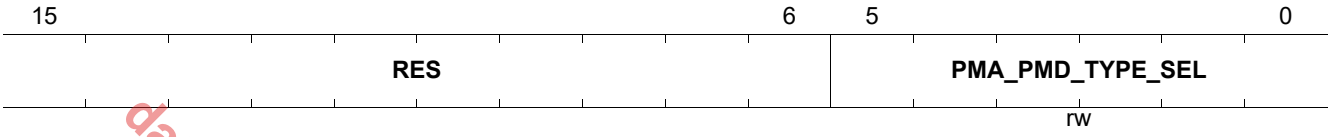
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**PMA/PMD Control 2 (Register 1.7)**

IEEE Standard Register=1.7

**PMA_CTL2** **Reset Value**

**PMA/PMD Control 2 (Register 1.7)** **$0030_H$**




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The product(or products) mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| PMA_PMD_TYPE_SEL | 5:0 | RW | **PMA/PMD Type Selection**<br>5 4 3 2 1 0<br>Others = Reserved<br>1 1 0 0 0 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 1 0 0 0 $0_B$ 2.5GBASE-T PMA<br>1 0 1 1 x $x_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 1 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 1 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 0 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 1 0 0 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 1 1 $x_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 1 0 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 1 0 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 1 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 1 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 0 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>1 0 0 0 0 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 1 x $x_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 1 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 1 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 0 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 1 0 0 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 1 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 1 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 0 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 1 0 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 1 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 1 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 0 $1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>0 1 0 0 0 $0_B$ Unsupported, defaults to 2.5GBASE-T PMA |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| PMA_PMD_TYPE_SEL | 5:0 | RW | **PMA/PMD Type Selection (cont'd)**<br>$0\ 0\ 1\ 1\ 1\ 1_B$ 10BASE-T PMA/PMD<br>$0\ 0\ 1\ 1\ 1\ 0_B$ 100BASE-TX PMA/PMD<br>$0\ 0\ 1\ 1\ 0\ 1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 1\ 1\ 0\ 0_B$ 1000BASE-T PMA/PMD<br>$0\ 0\ 1\ 0\ 1\ 1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 1\ 0\ 1\ 0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 1\ 0\ 0\ 1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 1\ 0\ 0\ 0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 1\ 1\ 1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 1\ 1\ 0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 1\ 0\ 1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 1\ 0\ 0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 0\ 1\ 1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 0\ 1\ 0_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 0\ 0\ 1_B$ Unsupported, defaults to 2.5GBASE-T PMA<br>$0\ 0\ 0\ 0\ 0\ 0_B$ Unsupported, defaults to 2.5GBASE-T PMA |

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**PMA/PMD Status 2 (Register 1.8)**

IEEE Standard Register=1.8

**PMA_STAT2** **Reset Value**

**PMA/PMD Status 2 (Register 1.8)** **$8200_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEVICE_PRESENT | | TX_FAUL* | RX_FAUL* | TX_FAULT | RX_FAULT | EXT_ABI* | PMD_TX_* | RMGBT_S* | RMGBT_L* | RMGBT_E* | RMGBT_L* | RMGBT_S* | RMGBT_L* | RMGBT_E* | PMA_LOC* |
| ro | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

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The product (or products) mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| DEVICE_PRESENT | 15:14 | RO | **Device Present**<br>$00_B$ No device responding at this address<br>$01_B$ No device responding at this address<br>$10_B$ Device responding at this address<br>$11_B$ No device responding at this address |
| TX_FAULT_ABILITY | 13 | RO | **Transmit Fault Ability**<br>$0_B$ PMA/PMD is not able to detect a fault condition on the transmit path.<br>$1_B$ PMA/PMD is able to detect a fault condition on the transmit path. |
| RX_FAULT_ABILITY | 12 | RO | **Receive Fault Ability**<br>$0_B$ PMA/PMD is not able to detect a fault condition on the receive path.<br>$1_B$ PMA/PMD is able to detect a fault condition on the receive path. |
| TX_FAULT | 11 | RO | **Transmit Fault**<br>$0_B$ No fault condition on transmit path<br>$1_B$ Fault condition on transmit path |
| RX_FAULT | 10 | RO | **Receive Fault**<br>$0_B$ No fault condition on receive path<br>$1_B$ Fault condition on receive path |
| EXT_ABILITIES | 9 | RO | **Extended Abilities**<br>$0_B$ PMA/PMD does not have extended abilities.<br>$1_B$ PMA/PMD has extended abilities listed in register 1.11. |
| PMD_TX_DISABLE | 8 | RO | **PMD Transmit Disable**<br>$0_B$ PMD is not able to disable the transmit path.<br>$1_B$ PMD is able to disable the transmit path. |
| RMGBT_SR_ABILITY | 7 | RO | **MULTIGBASE-SR Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-SR.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-SR. |
| RMGBT_LR_ABILITY | 6 | RO | **MULTIGBASE-LR Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-LR.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-LR. |
| RMGBT_ER_ABILITY | 5 | RO | **MULTIGBASE-ER Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-ER.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-ER. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| RMGBT_LX4_ ABILITY | 4 | RO | **MULTIGBASE-LX4 Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-LX4.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-LX4. |
| RMGBT_SW_ ABILITY | 3 | RO | **MULTIGBASE-SW Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-SW.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-SW. |
| RMGBT_LW_ ABILITY | 2 | RO | **MULTIGBASE-LW Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-LW.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-LW. |
| RMGBT_EW_ ABILITY | 1 | RO | **MULTIGBASE-EW Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-EW.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-EW. |
| PMA_LOCAL_ LOOPBACK | 0 | RO | **PMA Local Loopback**<br>$0_B$ PMA is not able to perform a local loopback function.<br>$1_B$ PMA is able to perform a local loopback function. |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### PMA/PMD Extended Ability (Register 1.11)

IEEE Standard Register=1.11

**PMA_EXT_ABILITY** **Reset Value**

**PMA/PMD Extended Ability (Register 1.11)** **$41A0_H$**

| 15 | 14 | 13 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | R2G5_EX* | RES | | R40G_10* | P2MP_AB* | R10BASE* | R100BAS* | R1000BA* | R1000BA* | RMGBT_K* | RMGBT_K* | RMGBT_A* | RMGBT_L* | RMGBT_C* |
| | ro | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| R2G5_EXT_ABILITIES | 14 | RO | **2.5G/5G Extended Abilities**<br>$0_B$ PMA/PMD does not have 2.5G/5G extended abilities.<br>$1_B$ PMA/PMD has 2.5G/5G extended abilities listed in register 1.21. |
| R40G_100G_EXT_ABILITIES | 10 | RO | **40G/100G Extended Abilities**<br>$0_B$ PMA/PMD does not have 40G/100G extended abilities.<br>$1_B$ PMA/PMD has 40G/100G extended abilities listed in register 1.13. |
| P2MP_ABILITY | 9 | RO | **P2MP Ability**<br>$0_B$ PMA/PMD does not have P2MP extended abilities.<br>$1_B$ PMA/PMD has P2MP abilities listed in register 1.12. |
| R10BASE_T_ABILITY | 8 | RO | **10BASE-T Ability**<br>$0_B$ PMA/PMD is not able to perform 10BASE-T.<br>$1_B$ PMA/PMD is able to perform 10BASE-T. |
| R100BASE_TX_ABILITY | 7 | RO | **100BASE-TX Ability**<br>$0_B$ PMA/PMD is not able to perform 100BASE-TX.<br>$1_B$ PMA/PMD is able to perform 100BASE-TX. |
| R1000BASE_KX_ABILITY | 6 | RO | **1000BASE-KX Ability**<br>$0_B$ PMA/PMD is not able to perform 1000BASE-KX.<br>$1_B$ PMA/PMD is able to perform 1000BASE-KX. |
| R1000BASE_T_ABILITY | 5 | RO | **1000BASE-T Ability**<br>$0_B$ PMA/PMD is not able to perform 1000BASE-T.<br>$1_B$ PMA/PMD is able to perform 1000BASE-T. |
| RMGBT_KR_ABILITY | 4 | RO | **MULTIGBASE-KR Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-KR.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-KR. |
| RMGBT_KX4_ABILITY | 3 | RO | **MULTIGBASE-KX4 Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-KX4.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-KX4. |
| RMGBT_ABILITY | 2 | RO | **10GBASE-T Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-T.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-T. |
| RMGBT_LRM_ABILITY | 1 | RO | **MULTIGBASE-LRM Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-LRM.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-LRM. |

data sheet are Not Recommended for New Designs (NRND)
The product (or product(s) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| RMGBT_CX4_ ABILITY | 0 | RO | **MULTIGBASE-CX4 Ability**<br>$0_B$ PMA/PMD is not able to perform MULTIGBASE-CX4.<br>$1_B$ PMA/PMD is able to perform MULTIGBASE-CX4. |

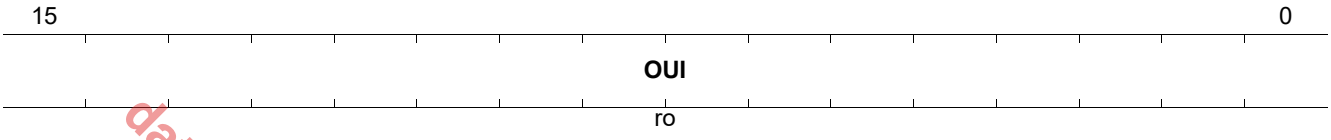
The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

### AN Package Identifier (Register 1.14)

IEEE Standard Register=1.14

**PMA_PACKID1** **Reset Value**

**AN Package Identifier (Register 1.14)** **C133$_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier**<br>Organizationally Unique Identifier Bits 3:18 |

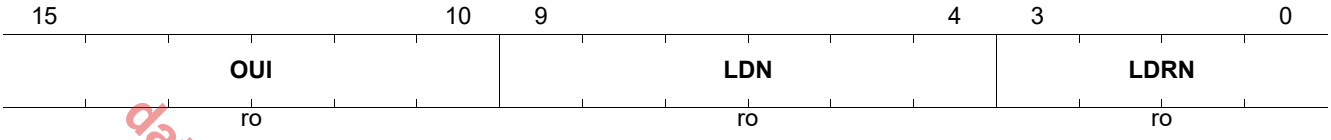
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### AN Package Identifier (Register 1.15)

IEEE Standard Register=1.15

**PMA_PACKID2** **Reset Value**

**AN Package Identifier (Register 1.15)** **$5400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several different products. |
| LDRN | 3:0 | RO | **Device Revision Number**<br>Specifies the device revision number[1)] to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

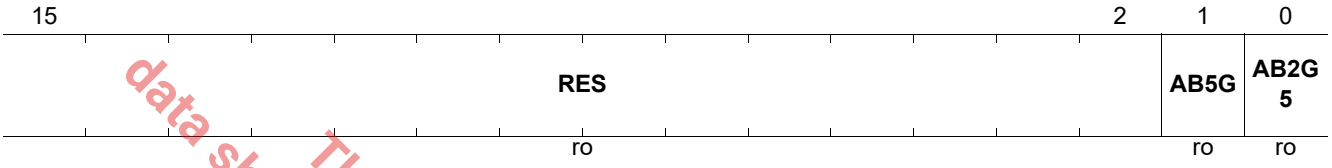
**PMAPMD Extended Ability (Register 1.21)**

Read only. Write from the STA has no effect.

IEEE Standard Register=1.21

**PMA_MGBT_EXTAB** **Reset Value**

**PMAPMD Extended Ability (Register 1.21)** **$0001_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:2 | RO | **Reserved**<br>Value always 0 |
| AB5G | 1 | RO | **PMA Ability to Perform 5GBASE-T**<br>$0_B$ **UNABLE** PMA is not able to perform 5GBASE-T.<br>$1_B$ **ABLE** PMA is able to perform 5GBASE-T. |
| AB2G5 | 0 | RO | **PMA Ability to Perform 2.5GBASE-T**<br>$0_B$ **UNABLE** PMA is not able to perform 2.5GBASE-T.<br>$1_B$ **ABLE** PMA is able to perform 2.5GBASE-T. |

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

**MULTIGBASE-T Status (Register 1.129)**

IEEE Standard Register=1.129

Indicates startup for 2.5G was completed.

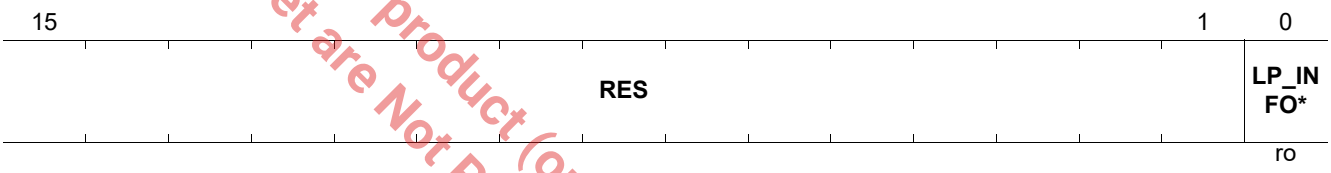
When read as a 1, indicates that the startup protocol (for 2.5G/5GBASE-T) was completed (link_status = OK, pcs_status = OK), and that the contents of bits 1.130.11:0 (Polarity), 1.131.15:10 (PBO), 1.145.14:8 (Skew), 1.146.14:8, and 1.146.6:0 (Skew), established during the startup protocol, are valid.

When read as a 0, indicates that the startup process was not completed, and that the contents of bit 1.129.0, established during the startup protocol, are invalid. A PMA must return a value of 0 in bit 1.129.1 when the PMA link_status = FAIL.

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

**PMA_MGBT_STAT** **Reset Value**

**MULTIGBASE-T Status (Register 1.129)** **$0000_H$**



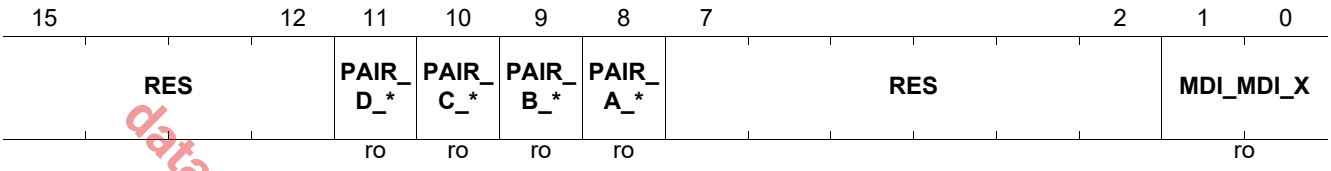

| Field | Bits | Type | Description |
|---|---|---|---|
| LP_INFORMATION_VALID | 0 | RO | **LP Information Valid**<br>When set, this bit indicates the startup protocol (126.4.2.5) was completed.<br>$0_B$ Link partner information is invalid<br>$1_B$ Link partner information is valid |

### MULTIGBASE-T Pair Swap and Polarity (Register 1.130)

IEEE Standard Register=1.130

**PMA_MGBT_POLARITY** **Reset Value**

**MULTIGBASE-T Pair Swap and Polarity (Register 1.130)** **$0003_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| PAIR_D_POLARITY | 11 | RO | **Pair D Polarity**<br>$0_B$ Polarity of pair D is not reversed.<br>$1_B$ Polarity of pair D is reversed. |
| PAIR_C_POLARITY | 10 | RO | **Pair C Polarity**<br>$0_B$ Polarity of pair C is not reversed.<br>$1_B$ Polarity of pair C is reversed. |
| PAIR_B_POLARITY | 9 | RO | **Pair B Polarity**<br>$0_B$ Polarity of pair B is not reversed.<br>$1_B$ Polarity of pair B is reversed. |
| PAIR_A_POLARITY | 8 | RO | **Pair A Polarity**<br>$0_B$ Polarity of pair A is not reversed.<br>$1_B$ Polarity of pair A is reversed. |
| MDI_MDI_X | 1:0 | RO | **MDI/MDI-X**<br>Indicates the status of pair swaps at the MDI / MD-X.<br>$00_B$ **ABCD CROSS** Pair AB and Pair CD crossover<br>$01_B$ **CD CROSS** Pair CD crossover only<br>$10_B$ **AB CROSS** Pair AB crossover only<br>$11_B$ **NORMAL** No crossover |

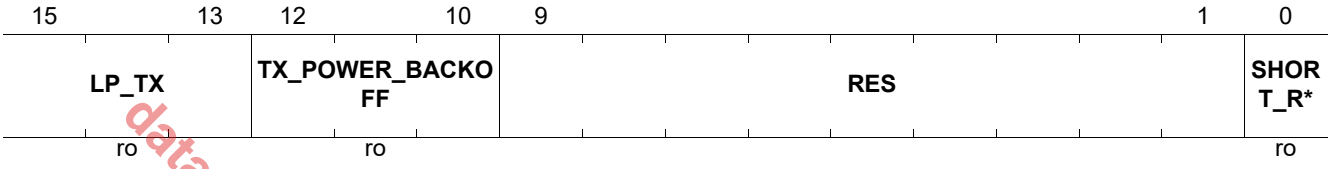
data sheet are Not Recommended for New Designs (NRND)
The product (or product(s) mentioned in this

### MULTIGBASE-T Tx Power Backoff and PHY Short Reach Setting (Register 1.131)

IEEE Standard Register=1.131

**PMA_MGBT_TX_PBO** **Reset Value**

**MULTIGBASE-T TX Power Backoff and PHY Short Reach Setting (Register 1.131)** **$0000_H$**




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The product (or products) mentioned in this

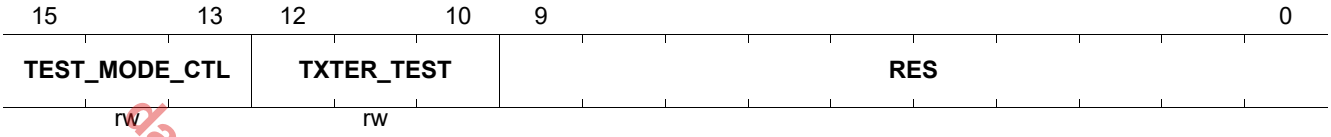
| Field | Bits | Type | Description |
|---|---|---|---|
| LP_TX | 15:13 | RO | **Link Partner Tx**<br>The power backoff setting of the link partner.<br>The bit number assignment order is: 15 14 13<br>$000_B$ 0 dB<br>$001_B$ 2 dB<br>$010_B$ 4 dB<br>$011_B$ 6 dB<br>$100_B$ 8 dB<br>$101_B$ 10 dB<br>$110_B$ 12 dB<br>$111_B$ 14 dB |
| TX_POWER_BACKOFF | 12:10 | RO | **Tx Power Backoff**<br>The power backoff of PHY211 PMA.<br>The bit number assignment order is: 12 11 10<br>$000_B$ 0 dB<br>$001_B$ 2 dB<br>$010_B$ 4 dB<br>$011_B$ 6 dB<br>$100_B$ 8 dB<br>$101_B$ 10 dB<br>$110_B$ 12 dB<br>$111_B$ 14 dB |
| SHORT_REACH_MODE | 0 | RO | **Short Reach Mode**<br>$0_B$ PHY is not operating in short reach mode<br>$1_B$ PHY is operating in short reach mode (not supported) |

### MULTIGBASE-T Test Mode (Register 1.132)

IEEE Standard Register=1.132

**PMA_MGBT_TEST_MODE** **Reset Value**

**MULTIGBASE-T Test Mode (Register 1.132)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| TEST_MODE_CTL | 15:13 | RW | **Test Mode Control**<br>$000_B$ Normal operation<br>$001_B$ Test mode 1<br>$010_B$ Test mode 2<br>$011_B$ Test mode 3<br>$100_B$ Test mode 4<br>$101_B$ Test mode 5<br>$110_B$ Test mode 6<br>$111_B$ Test mode 7 |
| TXTER_TEST | 12:10 | RW | **Transmitter Test**<br>Frequencies for tones used in Test Mode 4.<br>$000_B$ Reserved<br>$001_B$ Dual tone 1<br>$010_B$ Dual tone 2<br>$011_B$ Reserved<br>$100_B$ Dual tone 3<br>$101_B$ Dual tone 4<br>$110_B$ Dual tone 5<br>$111_B$ Reserved |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

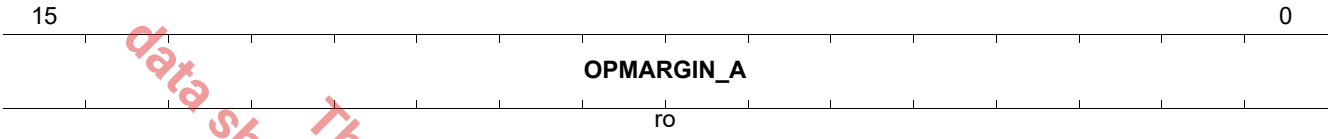
### MULTIGBASE-T SNR Margin Channel A (Register 1.133)

Register 1.133 contains the current SNR operating margin measured at the slicer input for channel A for the MULTIGBASE-T PMA.

IEEE Standard Register=1.133

**PMA_MGBT_SNR_OPMARGIN_A** **Reset Value**

**MULTIGBASE-T SNR Margin Channel A (Register 1.133)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_A | 15:0 | RO | **OPMARGIN_A**<br>SNR operating margin measured at the slicer input for channel A |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

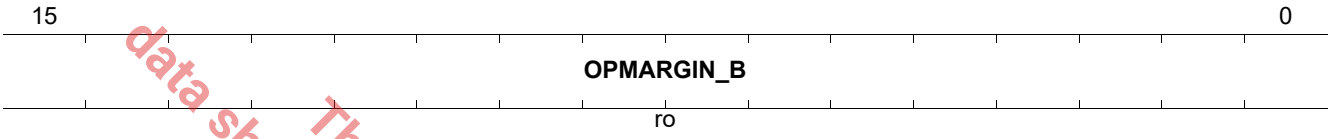
### MULTIGBASE-T SNR Margin Channel B (Register 1.134)

Register 1.134 contains the current SNR operating margin measured at the slicer input for channel B for the MULTIGBASE-T PMA.

IEEE Standard Register=1.134

**PMA_MGBT_SNR_OPMARGIN_B** **Reset Value**

**MULTIGBASE-T SNR Margin Channel B (Register 1.134)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_B | 15:0 | RO | **OPMARGIN_B**<br>SNR operating margin measured at the slicer input for channel B |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

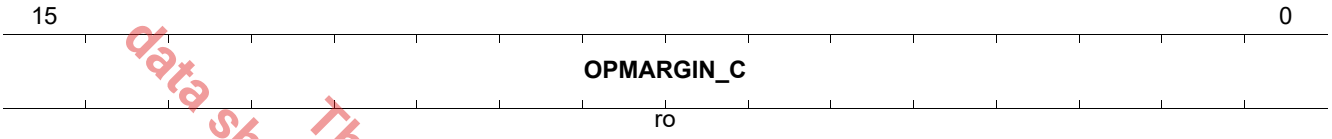
### MULTIGBASE-T SNR Margin Channel C (Register 1.135)

Register 1.135 contains the current SNR operating margin measured at the slicer input for channel C for the MULTIGBASE-T PMA.

IEEE Standard Register=1.135

**PMA_MGBT_SNR_OPMARGIN_C** **Reset Value**

**MULTIGBASE-T SNR Margin Channel C (Register 1.135)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_C | 15:0 | RO | **OPMARGIN_C**<br>SNR operating margin measured at the slicer input for channel C |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

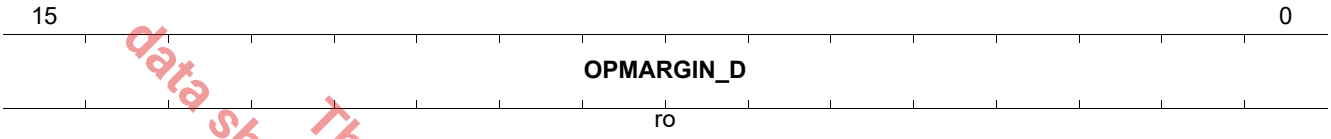
### MULTIGBASE-T SNR Margin Channel D (Register 1.136)

Register 1.136 contains the current SNR operating margin measured at the slicer input for channel D for the MULTIGBASE-T PMA.

IEEE Standard Register=1.136

**PMA_MGBT_SNR_OPMARGIN_D** **Reset Value**

**MULTIGBASE-T SNR Margin Channel D (Register 1.136)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OPMARGIN_D | 15:0 | RO | **OPMARGIN_D**<br>SNR operating margin measured at the slicer input for channel D |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

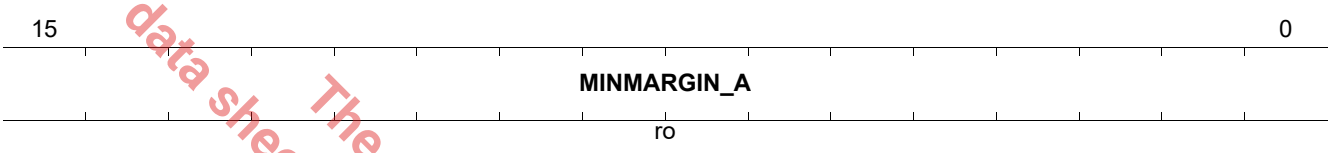
### MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read.

IEEE Standard Register=1.137

**PMA_MGBT_MINMARGIN_A** **Reset Value**

**MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_A | 15:0 | RO | **MINMARGIN_A**<br>Lowest value observed in the SNR operating margin channel A register (1.133) since the last read |

data sheet are not Recommended for New Designs (NRND)
The product(s) mentioned in this

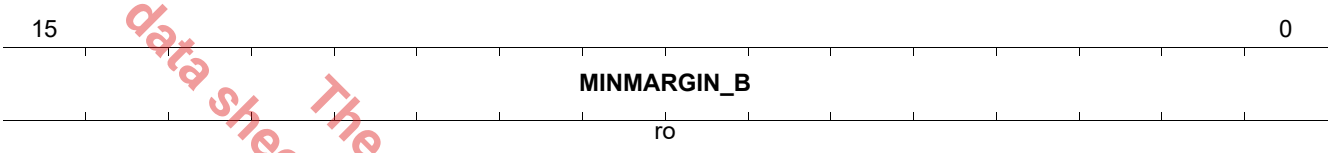
### MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel B register (1.134) since the last read.

IEEE Standard Register=1.138

**PMA_MGBT_MINMARGIN_B** **Reset Value**

**MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_B | 15:0 | RO | **MINMARGIN_B**<br>Lowest value observed in the SNR operating margin channel B register (1.134) since the last read |

data sheet are not Recommended for New Designs (NRND)
The product(s) mentioned in this

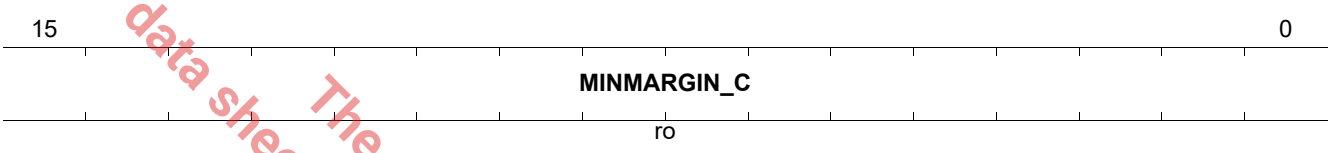
### MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139)

The minimum margin channel C register contains a latched copy of the lowest value observed in the SNR operating margin channel C register (1.135) since the last read.

IEEE Standard Register=1.139

**PMA_MGBT_MINMARGIN_C** **Reset Value**

**MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_C | 15:0 | RO | **MINMARGIN_C**<br>Lowest value observed in the SNR operating margin channel C register (1.135) since the last read |

data sheet are not Recommended for New Designs (NRND)
The product(s) mentioned in this

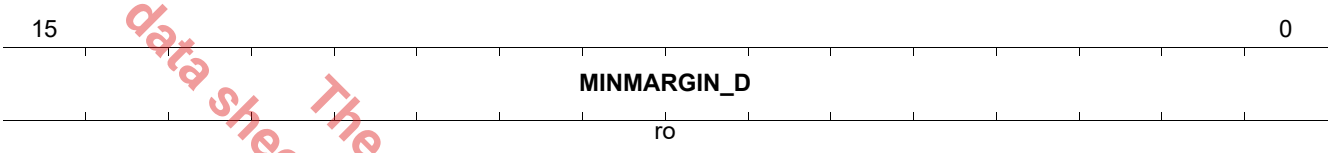
### MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140)

The Minimum margin channel D register contains a latched copy of the lowest value observed in the SNR operating margin channel D register (1.136) since the last read.

IEEE Standard Register=1.140

**PMA_MGBT_MINMARGIN_D** **Reset Value**

**MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| MINMARGIN_D | 15:0 | RO | **MINMARGIN_D**<br>Lowest value observed in the SNR operating margin channel D register (1.136) since the last read |

data sheet are not Recommended for New Designs (NRND)
The product(s) mentioned in this

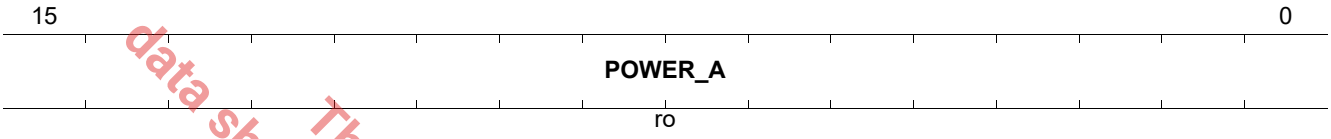
### MULTIGBASE-T Rx Power Channel A (Register 1.141)

The Rx signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.141

**PMA_MGBT_POWER_A** **Reset Value**

**MULTIGBASE-T Rx Power Channel A (Register 1.141)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_A | 15:0 | RO | **POWER_A**<br>Receive signal power measured at the MDI during training |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

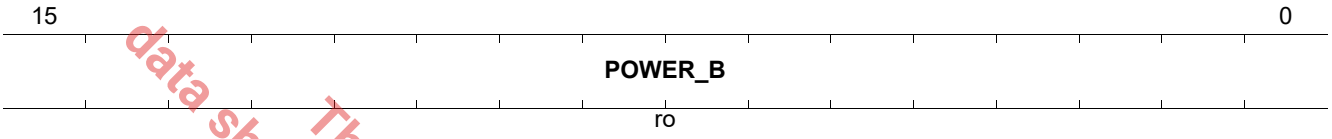
### MULTIGBASE-T Rx Power Channel B (Register 1.142)

The Rx signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.142

**PMA_MGBT_POWER_B** **Reset Value**

**MULTIGBASE-T Rx Power Channel B (Register 1.142)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_B | 15:0 | RO | **POWER_B**<br>Receive signal power measured at the MDI during training |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

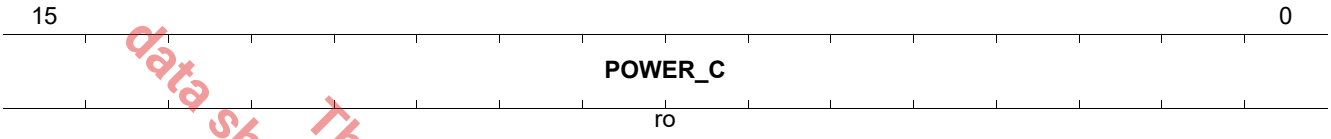
### MULTIGBASE-T Rx Power Chan C (Register 1.143)

The Rx signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.143

**PMA_MGBT_POWER_C** **Reset Value**

**MULTIGBASE-T Rx Power Chan C (Register 1.143)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_C | 15:0 | RO | **POWER_C**<br>Receive signal power measured at the MDI during training |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

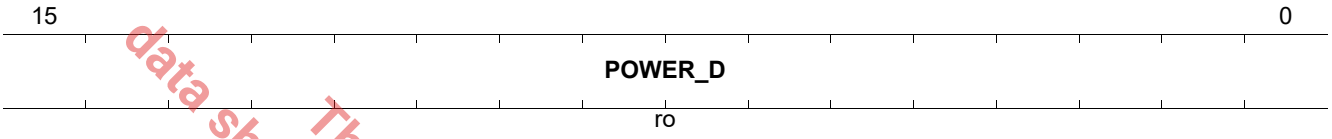
### MULTIGBASE-T Rx Power Chan D (Register 1.144)

The Rx signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.144

**PMA_MGBT_POWER_D** **Reset Value**

**MULTIGBASE-T Rx Power Chan D (Register 1.144)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| POWER_D | 15:0 | RO | **POWER_D**<br>Receive signal power measured at the MDI during training |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

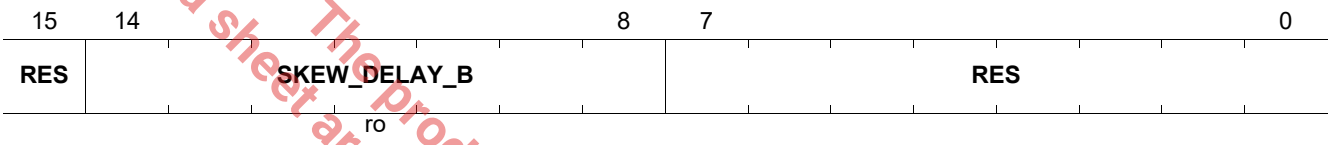
### MULTIGBASE-T Skew Delay 0 (Register 1.145)

IEEE Standard Register=1.145

The skew delay reports the current skew delay on each of the pairs with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. When the delay exceeds the maximum amount represented by the range -80 ns to +78.75 ns, the field displays the maximum value.

**PMA_MGBT_SKEW_DELAY_0** **Reset Value**

**MULTIGBASE-T Skew Delay 0 (Register 1.145)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| SKEW_DELAY_B | 14:8 | RO | **Skew Delay B**<br>Skew delay for pair B |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

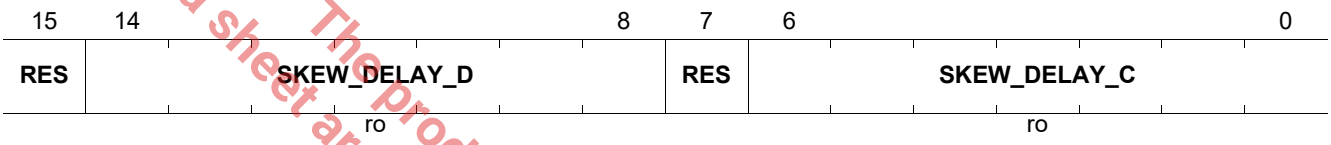
### MULTIGBASE-T Skew Delay 1 (Register 1.146)

IEEE Standard Register=1.146

The skew delay reports the current skew delay on each of the pairs with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. When the delay exceeds the maximum amount represented by the range -80 ns to +78.75 ns, the field displays the maximum value.

**PMA_MGBT_SKEW_DELAY_1** **Reset Value**

**MULTIGBASE-T Skew Delay 1 (Register 1.146)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| SKEW_DELAY_D | 14:8 | RO | **Skew Delay D**<br>Skew delay for pair D |
| SKEW_DELAY_C | 6:0 | RO | **Skew Delay C**<br>Skew delay for pair C |

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The product (or products) mentioned in this

### MULTIGBASE-T Skew Delay 2 (Register 1.147)

IEEE Standard Register=1.147

**PMA_MGBT_FAST_RETRAIN_STA_CTRL** **Reset Value**

**MULTIGBASE-T Skew Delay 2 (Register 1.147)** **$0010_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| LP_FAST_RETRAIN_COUNT | 15:11 | RO | **LP Fast Retrain Count**<br>Counts the number of fast retrains requested by the link partner. |
| LD_FAST_RETRAIN_COUNT | 10:6 | RO | **LD Fast Retrain Count**<br>Counts the number of fast retrains requested by the local device. |
| FAST_RETRAIN_ABILITY | 4 | RO | **Fast Retrain Ability**<br>$0_B$ Fast retrain capability is not supported.<br>$1_B$ Fast retrain capability is supported. |
| FAST_RETRAIN_NEGOTIATED | 3 | RO | **Fast Retrain Negotiated**<br>$0_B$ Fast retrain capability was not negotiated.<br>$1_B$ Fast retrain capability was negotiated. |
| FAST_RETRAIN_SIG_TYPE | 2:1 | RW | **Fast Retrain Signal Type**<br>$00_B$ PHY signals IDLE during fast retrain<br>$01_B$ PHY signals local fault during fast retrain<br>$10_B$ PHY signals link interruption during fast retrain<br>$11_B$ Reserved |
| FAST_RETRAIN_ENABLE | 0 | RW | **Fast Retrain Enable**<br>$0_B$ Fast retrain capability is disabled.<br>$1_B$ Fast retrain capability is enabled. |

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The product (or products) mentioned in this

**PMA TimeSync Capability Indication (Register 1.1800)**

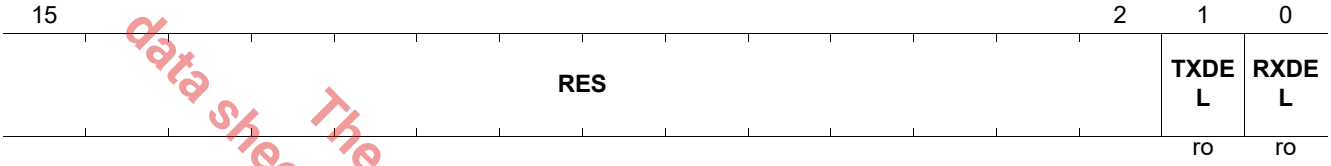
PMA TimeSync Capability indication register.

GPHY does not support providing data path delay information.

IEEE Standard Register=1.1800

**PMA_TIMESYNC_CAP** **Reset Value**

**PMA TimeSync Capability Indication (Register 1.1800)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| TXDEL | 1 | RO | **Transmit Data Path Delay Information**<br>Not supported by the GPHY.<br>$0_B$ **NONE** PHYs do not have this capability.<br>$1_B$ **CAPABLE** Minimum and maximum Tx data path delay available |
| RXDEL | 0 | RO | **Receive Data Path Delay Information**<br>Not supported by the GPHY.<br>$0_B$ **NONE** PHYs do not have this capability.<br>$1_B$ **CAPABLE** Minimum and maximum Rx data path delay available |

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The product(s) mentioned in this

## 6.2 Standard PCS Registers

This section describes the PCS registers for MMD device 0x03.

**Table 32 Registers Overview- Standard PCS Registers**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| PCS_CTRL1 | PCS Control 1 (Register 3.0) | $205C_H$ |
| PCS_STAT1 | PCS Status 1 (Register 3.1) | $0000_H$ |
| PCS_DEVID1 | PHY Identifier 1 (Register 3.2) | $C133_H$ |
| PCS_DEVID2 | PHY Identifier 2 (Register 3.3) | $5400_H$ 1) |
| PCS_SPEED_ABILITY | PCS Speed Ability (Register 3.4) | $0040_H$ |
| PCS_DIP1 | PCS Devices in Package 1 (Register 3.5) | $008B_H$ |
| PCS_DIP2 | PCS Devices in Package 2 (Register 3.6) | $C000_H$ |
| PCS_CTRL2 | PCS Control 2 (Register 3.7) | $000A_H$ |
| PCS_STAT2 | PCS Status 2 (Register 3.8) | $9000_H$ |
| PCS_PACKID1 | PCS Package Identifier 1 (Register 3.14) | $C133_H$ |
| PCS_PACKID2 | PCS Package Identifier 2 (Register 3.15) | $5400_H$ 1) |
| PCS_EEE_CAP | PCS EEE Capability (Register 3.20) | $0006_H$ |
| PCS_EEE_CAP2 | EEE Control and Capability 2 (Register 3.21) | $0001_H$ |
| PCS_EEE_WAKERR | PCS EEE Status Register 1 (Register 3.22) | $0000_H$ |
| PCS_2G5_STAT1 | BASE-R and 10GBASE-T PCS Status 1 (Register 3.32) | $0000_H$ |
| PCS_2G5_STAT2 | MULTIGBASE-T PCS Status 2 (Register 3.33) | $0000_H$ |
| PCS_TIMESYNC_CAP | PCS TimeSync Capability Register (Register 3.1800) | $0000_H$ |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

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The Product (or Products) mentioned in this

### 6.2.1 PCS Register Descriptions

This section describes all the PCS registers in detail.

**PCS Control 1 (Register 3.0)**

IEEE Standard Register=3.0

**PCS_CTRL1** **Reset Value**

**PCS Control 1 (Register 3.0)** **$205C_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 … 7 | 6 | 5 … 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RST | LOOP BACK | SSL | RES | LOW_ POW* | RXCK ST | RES | SSM | SPEED_SEL | RES | |
| rw | rw | rw | | rw | rw | | rw | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RW | **Reset**<br>$0_B$ Normal operation<br>$1_B$ PCS reset - Self-clearing |
| LOOPBACK | 14 | RW | **Loopback**<br>$0_B$ Disable loopback mode<br>$1_B$ Enable loopback mode |
| SSL | 13 | RW | **Forced Speed Selection (LSB)**<br>This bit is used in conjunction with SPEED_SEL_LSB.<br>The bit assignment order is: MSB LSB<br>$00_B$ 10 Mbps<br>$01_B$ 100 Mbps<br>$10_B$ 1000 Mbps<br>$11_B$ Bits [5:2] select the speed |
| LOW_POWER | 11 | RW | **Low Power**<br>$0_B$ Normal operation<br>$1_B$ Low-power mode |
| RXCKST | 10 | RW | **Clock Stop Enable**<br>The MAC sets this bit to active to allow the GPHY to stop the clocking during the LPI_MODE.<br>$0_B$ The clock is not stoppable.<br>$1_B$ The GPHY stops the (X)GMII clock during LPI. |
| SSM | 6 | RW | **Forced Speed Selection (MSB)**<br>This bit is used in conjunction with SPEED_SEL_MSB.<br>The bit assignment order is: MSB LSB<br>$00_B$ 10 Mbps<br>$01_B$ 100 Mbps<br>$10_B$ 1000 Mbps<br>$11_B$ Bits [5:2] select the speed |

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| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SPEED_SEL | 5:2 | RW | **Forced Speed Selection Values**<br>$0\ 0\ 0\ 0_B$ Unsupported, defaults to 2.5 Gbps<br>$0\ 0\ 0\ 1_B$ Unsupported, defaults to 2.5 Gbps<br>$0\ 0\ 1\ 0_B$ Unsupported, defaults to 2.5 Gbps<br>$0\ 0\ 1\ 1_B$ Unsupported, defaults to 2.5 Gbps<br>$0\ 1\ 0\ 0_B$ Unsupported, defaults to 2.5 Gbps<br>$0\ 1\ 0\ 1_B$ Reserved<br>$0\ 1\ 1\ 1_B$ 2.5 Gbps<br>$1\ 1\ x\ x_B$ Reserved |

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**PCS Status 1 (Register 3.1)**

IEEE Standard Register=3.1

**PCS_STAT1** **Reset Value**

**PCS Status 1 (Register 3.1)** **$0000_H$**

| 15 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RES | TX_LPI_* | RX_LPI_* | TX_LPI_* | RX_LPI_* | FAULT | TXCKST | RES | PCS_RX_* | LOW_POW* | RES |
| | ro | ro | ro | ro | ro | ro | | ro | ro | |

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The product (or products) mentioned in this

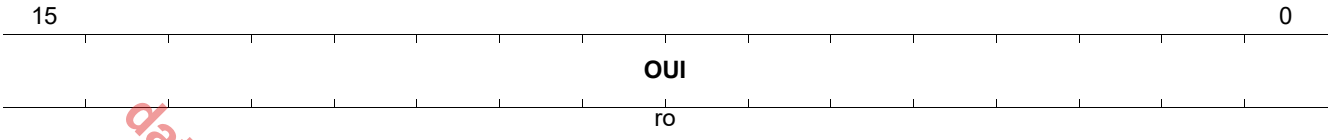
| Field | Bits | Type | Description |
|---|---|---|---|
| TX_LPI_RXD | 11 | RO | **Tx LPI Received**<br>$0_B$ LPI not received<br>$1_B$ Tx PCS received LPI |
| RX_LPI_RXD | 10 | RO | **Rx LPI Received**<br>$0_B$ LPI not received<br>$1_B$ Rx PCS received LPI |
| TX_LPI_INDICATION | 9 | RO | **Tx LPI Indication**<br>$0_B$ PCS is not currently receiving LPI.<br>$1_B$ Tx PCS is currently receiving LPI. |
| RX_LPI_INDICATION | 8 | RO | **Rx LPI Indication**<br>$0_B$ PCS is not currently receiving LPI.<br>$1_B$ Rx PCS is currently receiving LPI. |
| FAULT | 7 | RO | **Fault**<br>$0_B$ No fault condition detected<br>$1_B$ Fault condition detected |
| TXCKST | 6 | RO | **Clock Stop Capable**<br>$0_B$ The clock is not stoppable.<br>$1_B$ The MAC is allowed to stop the clock during LPI. |
| PCS_RX_LINK_STATUS | 2 | RO | **PCS Receive Link Status**<br>$0_B$ PCS receive link down<br>$1_B$ PCS receive link up |
| LOW_POWER_ABILITY | 1 | RO | **Low Power Ability**<br>$0_B$ PCS does not support low power mode.<br>$1_B$ PCS supports low power mode. |

**PHY Identifier 1 (Register 3.2)**

IEEE Standard Register=3.2

**PCS_DEVID1** **Reset Value**

**PHY Identifier 1 (Register 3.2)** **$C133_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier Bits 3:18** |

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The product (or products) mentioned in this

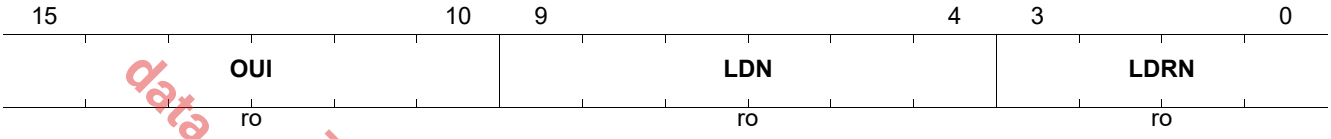
**PHY Identifier 2 (Register 3.3)**

Organizationally Unique Identifier Bits 19:24

IEEE Standard Register=3.3

**PCS_DEVID2** **Reset Value**

**PHY Identifier 2 (Register 3.3)** **$5400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1] to distinguish between several different products. |
| LDRN | 3:0 | RO | **Device Revision Number**<br>Specifies the device revision number[1] to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

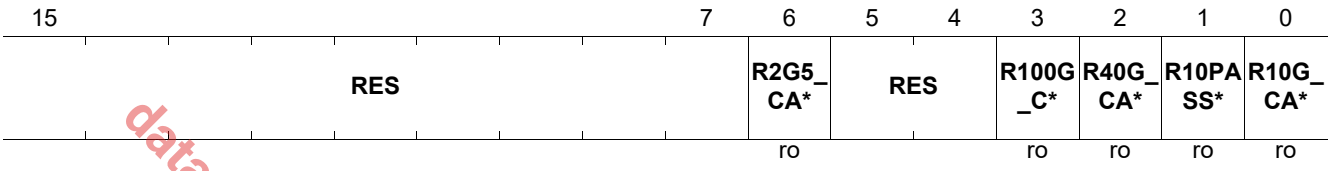
data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

**PCS Speed Ability (Register 3.4)**

IEEE Standard Register=3.4

**PCS_SPEED_ABILITY** **Reset Value**

**PCS Speed Ability (Register 3.4)** **$0040_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| R2G5_CAPABLE | 6 | RO | **2G5 Capable**<br>This bit is always set to $1_B$ because the PCS is capable of operating at 2.5 Gbps. |
| R100G_CAPABLE | 3 | RO | **100G Capable**<br>$0_B$ PCS is not capable of operating at 100 Gbps.<br>$1_B$ PCS is capable of operating at 100 Gbps. |
| R40G_CAPABLE | 2 | RO | **40G Capable**<br>$0_B$ PCS is not capable of operating at 40 Gbps.<br>$1_B$ PCS is capable of operating at 40 Gbps. |
| R10PASS_TS_2BASE_TL | 1 | RO | **10PASS-TS/2BASE-TL Capable**<br>$0_B$ PCS is not capable of operating as the 10P/2B PCS.<br>$1_B$ PCS is capable of operating as the 10P/2B PCS. |
| R10G_CAPABLE | 0 | RO | **10G Capable**<br>$0_B$ PCS is not capable of operating at 10 Gbps.<br>$1_B$ PCS is capable of operating at 10 Gbps. |

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The product (or products) mentioned in this

**PCS Devices in Package 1 (Register 3.5)**

IEEE Standard Register=3.5

**PCS_DIP1** **Reset Value**

**PCS Devices in Package 1 (Register 3.5)** **$008B_H$**

| 15 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | SEPARAT* | SEP_PMA* | SEPARAT* | SEPARAT* | ANEG | TC | DTE_XS | PHY_XS | PCS | WIS_PRE* | PMD_PMA | CL22 |
| ro | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Ignore on read |
| SEPARATED_PMA_4 | 11 | RO | **Separate PMA (4)**<br>$0_B$ Separate PMA (4) not present in package<br>$1_B$ Separate PMA (4) present in package |
| SEP_PMA_3 | 10 | RO | **Separate PMA (3)**<br>$0_B$ Separate PMA (3) not present in package<br>$1_B$ Separate PMA (3) present in package |
| SEPARATED_PMA_2 | 9 | RO | **Separate PMA (2)**<br>$0_B$ Separate PMA (2) not present in package<br>$1_B$ Separate PMA (2) present in package |
| SEPARATED_PMA_1 | 8 | RO | **Separate PMA (1)**<br>$0_B$ Separate PMA (1) not present in package<br>$1_B$ Separate PMA (1) present in package |
| ANEG | 7 | RO | **Auto-Negotiation Present**<br>$0_B$ Auto-negotiation not present in package<br>$1_B$ Auto-negotiation present in package |
| TC | 6 | RO | **TC Present**<br>$0_B$ TC not present in package<br>$1_B$ TC present in package |
| DTE_XS | 5 | RO | **DTE XS Present**<br>$0_B$ DTE XS not present in package<br>$1_B$ DTE XS present in package |
| PHY_XS | 4 | RO | **PHY XS Present**<br>$0_B$ PHY XS not present in package<br>$1_B$ PHY XS present in package |
| PCS | 3 | RO | **PCS Present**<br>$0_B$ PCS not present in package<br>$1_B$ PCS present in package |
| WIS_PRESENT | 2 | RO | **WIS Present**<br>$0_B$ WIS not present in package<br>$1_B$ WIS present in package |

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| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| PMD_PMA | 1 | RO | **PMD/PMA Present**<br>$0_B$ PMA/PMD not present in package<br>$1_B$ PMA/PMD present in package |
| CL22 | 0 | RO | **Clause 22 Registers Present**<br>$0_B$ Clause 22 registers not present in package<br>$1_B$ Clause 22 registers present in package |

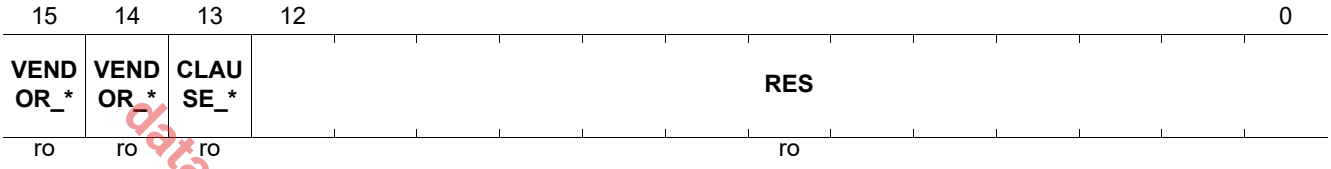
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**PCS Devices in Package 2 (Register 3.6)**

IEEE Standard Register=3.6

**PCS_DIP2** **Reset Value**

**PCS Devices in Package 2 (Register 3.6)** **$C000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| VENDOR_SPECIFIC_DEVICE_2 | 15 | RO | **Vendor-specific Device 2**<br>$0_B$ Vendor-specific device 2 not present in package<br>$1_B$ Vendor-specific device 2 present in package |
| VENDOR_SPECIFIC_DEVICE_1 | 14 | RO | **Vendor-specific Device 1**<br>$0_B$ Vendor-specific device 1 not present in package<br>$1_B$ Vendor-specific device 1 present in package |
| CLAUSE_22_EXTENSION | 13 | RO | **Clause 22 Extension**<br>$0_B$ Clause 22 extension not present in package<br>$1_B$ Clause 22 extension present in package |
| RES | 12:0 | RO | **Reserved**<br>Ignore on read. |

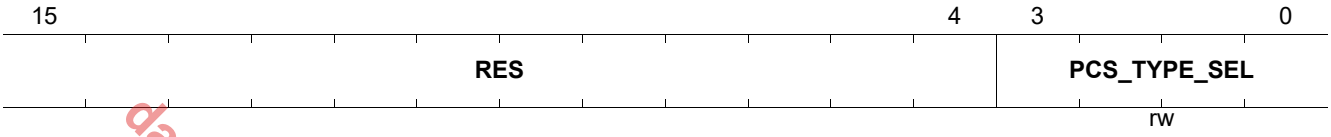
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

**PCS Control 2 (Register 3.7)**

IEEE Standard Register=3.7

**PCS_CTRL2** **Reset Value**

**PCS Control 2 (Register 3.7)** **$000A_H$**




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The product(or products)mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| PCS_TYPE_SEL | 3:0 | RW | **PCS Type Selection**<br>$0000_B$ Not supported, defaults to 2.5 Gbps<br>$0001_B$ Not supported, defaults to 2.5 Gbps<br>$0010_B$ Not supported, defaults to 2.5 Gbps<br>$0011_B$ Not supported, defaults to 2.5 Gbps<br>$0100_B$ Not supported, defaults to 2.5 Gbps<br>$0101_B$ Not supported, defaults to 2.5 Gbps<br>$0110_B$ Not supported, defaults to 2.5 Gbps<br>$0111_B$ Not supported, defaults to 2.5 Gbps<br>$1000_B$ Reserved<br>$1001_B$ Not supported, defaults to 2.5 Gbps<br>$1010_B$ Select 2.5 Gbps PCS type (Default)<br>$1011_B$ Not supported, defaults to 2.5 Gbps<br>$1100_B$ Not supported, defaults to 2.5 Gbps<br>$1101_B$ Not supported, defaults to 2.5 Gbps<br>$1110_B$ Reserved<br>$1111_B$ Reserved |

**PCS Status 2 (Register 3.8)**

IEEE Standard Register=3.8

**PCS_STAT2** **Reset Value**

**PCS Status 2 (Register 3.8)** **$9000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEVICE_PRESENT | | RES | R2G5_CA* | TX_FAULT | RX_FAULT | RES | | R100GBA* | R40GBAS* | R10GBAS* | R10GBAS* | R10GBAS* | R10GBAS* |
| ro | | | ro | ro | ro | | | ro | ro | ro | ro | ro | ro |

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The product (or products) mentioned in this

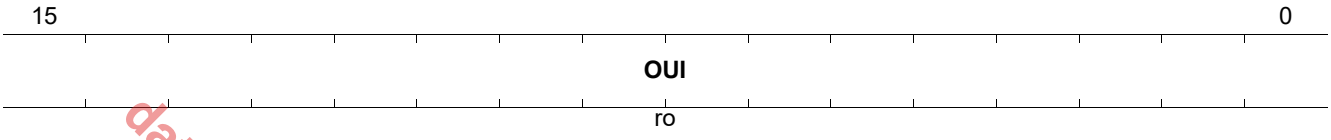
| Field | Bits | Type | Description |
|---|---|---|---|
| DEVICE_PRESENT | 15:14 | RO | **Device Present**<br>$00_B$ No device responding at this address<br>$01_B$ No device responding at this address<br>$10_B$ Device responding at this address<br>$11_B$ No device responding at this address |
| R2G5_CAPABLE | 12 | RO | **2G5BASE-T Capable**<br>$0_B$ PCS is not able to support 2.5GBASE-T PCS type.<br>$1_B$ PCS is able to support 2.5GBASE-T PCS type. |
| TX_FAULT | 11 | RO | **Transmit Fault**<br>$0_B$ No fault condition on transmit path<br>$1_B$ Fault condition on transmit path |
| RX_FAULT | 10 | RO | **Receive Fault**<br>$0_B$ No fault condition on receive path<br>$1_B$ Fault condition on receive path |
| R100GBASE_R_CAPABLE | 5 | RO | **100GBASE-R Capable**<br>$0_B$ PCS is not able to support 100GBASE-R PCS type.<br>$1_B$ PCS is able to support 100GBASE-R PCS type. |
| R40GBASE_R_CAPABLE | 4 | RO | **40GBASE-R Capable**<br>$0_B$ PCS is not able to support 40GBASE-R PCS type.<br>$1_B$ PCS is able to support 40GBASE-R PCS type. |
| R10GBASE_T_CAPABLE | 3 | RO | **10GBASE-T Capable**<br>$0_B$ PCS is not able to support 10GBASE-T PCS type.<br>$1_B$ PCS is able to support 10GBASE-T PCS type. |
| R10GBASE_W_CAPABLE | 2 | RO | **10GBASE-W Capable**<br>$0_B$ PCS is not able to support 10GBASE-W PCS type.<br>$1_B$ PCS is able to support 10GBASE-W PCS type. |
| R10GBASE_X_CAPABLE | 1 | RO | **10GBASE-X Capable**<br>$0_B$ PCS is not able to support 10GBASE-X PCS type.<br>$1_B$ PCS is able to support 10GBASE-X PCS type. |
| R10GBASE_R_CAPABLE | 0 | RO | **10GBASE-R Capable**<br>$0_B$ PCS is not able to support 10GBASE-R PCS types.<br>$1_B$ PCS is able to support 10GBASE-R PCS types. |

**PCS Package Identifier 1 (Register 3.14)**

IEEE Standard Register=3.14

**PCS_PACKID1** **Reset Value**

**PCS Package Identifier 1 (Register 3.14)** **$C133_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier Bits 3:18** |

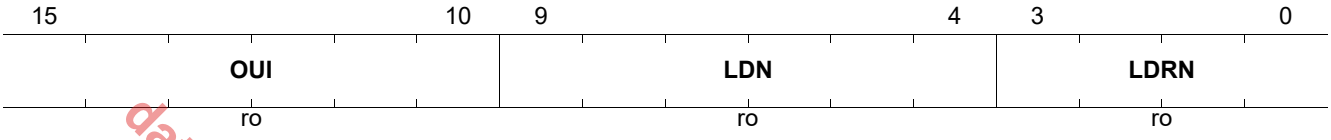
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### PCS Package Identifier 2 (Register 3.15)

IEEE Standard Register=3.15

**PCS_PACKID2** **Reset Value**

**PCS Package Identifier 2 (Register 3.15)** **$5400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several different products. |
| LDRN | 3:0 | RO | **Device Revision Number**<br>Specifies the device revision number to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

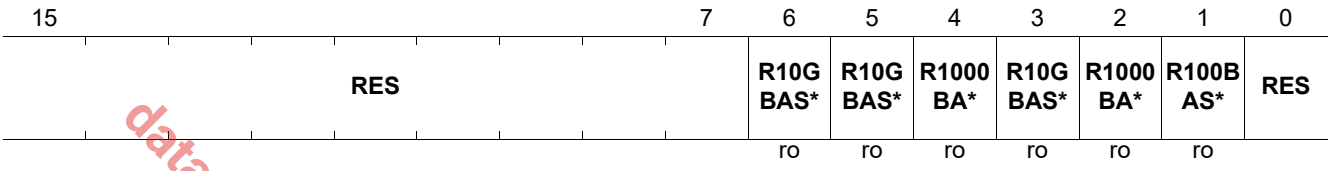
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The product(s) mentioned in this

**PCS EEE Capability (Register 3.20)**

IEEE Standard Register=3.20

**PCS_EEE_CAP** **Reset Value**

**PCS EEE Capability (Register 3.20)** **$0006_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| R10GBASE_KR_EEE | 6 | RO | **10GBASE-KR EEE**<br>$0_B$ EEE is not supported for 10GBASE-KR.<br>$1_B$ EEE is supported for 10GBASE-KR. |
| R10GBASE_KX4_EEE | 5 | RO | **10GBASE-KX4 EEE**<br>$0_B$ EEE is not supported for 10GBASE-KX4.<br>$1_B$ EEE is supported for 10GBASE-KX4. |
| R1000BASE_KX_EEE | 4 | RO | **1000BASE-KX EEE**<br>$0_B$ EEE is not supported for 1000BASE-KX.<br>$1_B$ EEE is supported for 1000BASE-KX. |
| R10GBASE_T_EEE | 3 | RO | **10GBASE-T EEE**<br>$0_B$ EEE is not supported for 10GBASE-T.<br>$1_B$ EEE is supported for 10GBASE-T. |
| R1000BASE_T_EEE | 2 | RO | **1000BASE-T EEE**<br>$0_B$ EEE is not supported for 1000BASE-T.<br>$1_B$ EEE is supported for 1000BASE-T. |
| R100BASE_TX_EEE | 1 | RO | **100BASE-TX EEE**<br>$0_B$ EEE is not supported for 100BASE-TX.<br>$1_B$ EEE is supported for 100BASE-TX. |

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The product (or products) mentioned in this

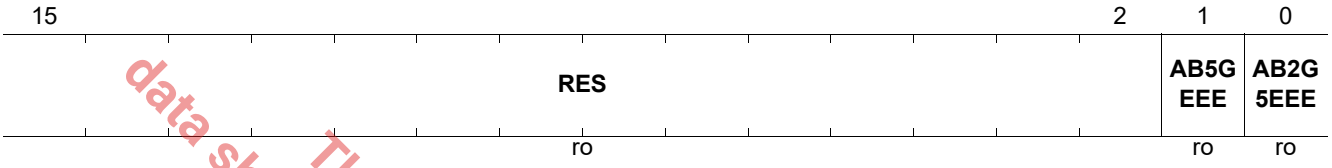
**EEE Control and Capability 2 (Register 3.21)**

Read only. Write from the STA has no effect.

IEEE Standard Register=3.21

**PCS_EEE_CAP2** **Reset Value**

**EEE Control and Capability 2 (Register 3.21)** **$0001_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:2 | RO | **Reserved**<br>Value always 0. |
| AB5GEEE | 1 | RO | **EEE Supported for 5GBASE-T**<br>$0_B$ **UNABLE** EEE is not supported for 5GBASE-T.<br>$1_B$ **ABLE** EEE is supported for 5GBASE-T. |
| AB2G5EEE | 0 | RO | **EEE Supported for 2.5GBASE-T**<br>$0_B$ **UNABLE** EEE is not supported for 2.5GBASE-T.<br>$1_B$ **ABLE** EEE is supported for 2.5GBASE-T. |

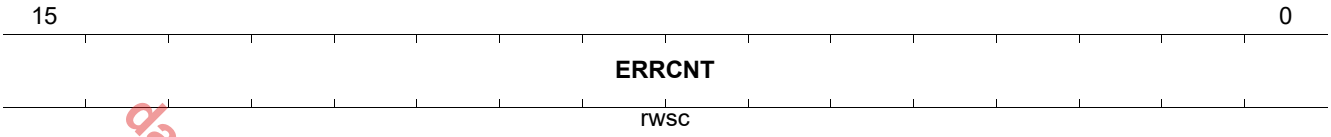
data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

**PCS EEE Status Register 1 (Register 3.22)**

IEEE Standard Register=3.22

**PCS_EEE_WAKERR** **Reset Value**

**PCS EEE Status Register 1 (Register 3.22)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| ERRCNT | 15:0 | RWSC | **EEE Wake Error Counter**<br>This is a 16-bit saturating counter indicating the number of times the GPHY PHY fails to wake up within the EEE time. This counter is cleared upon read from the STA. |

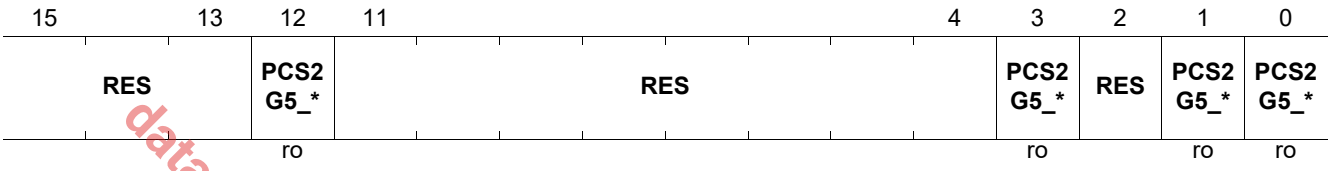
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### BASE-R and 10GBASE-T PCS Status 1 (Register 3.32)

IEEE Standard Register=3.32

**PCS_2G5_STAT1** **Reset Value**

**BASE-R and 10GBASE-T PCS Status 1 (Register 3.32)** **$0000_H$**



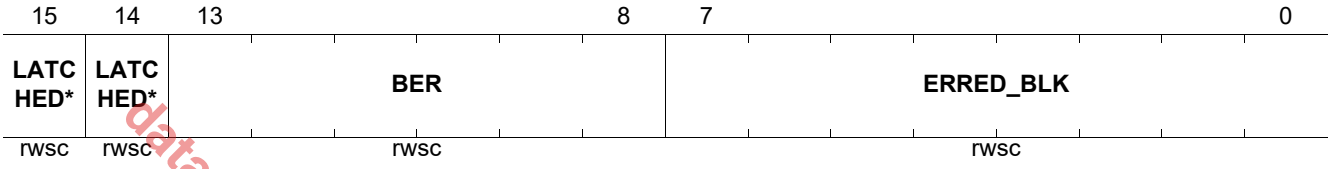

| Field | Bits | Type | Description |
|---|---|---|---|
| PCS2G5_LINK_STATUS | 12 | RO | **BASE-R and 10GBase-T Rx Link Status**<br>$0_B$ 2G5 PCS receive link down<br>$1_B$ 2G5 PCS receive link up |
| PCS2G5_PAT_TEST_AB | 3 | RO | **PRBS9 Pattern Testing Ability**<br>$0_B$ PCS is not able to support PRBS9 pattern testing.<br>$1_B$ PCS is able to support PRBS9 pattern testing. |
| PCS2G5_HI_BER | 1 | RO | **PCS 2G5 High BER**<br>This bit is a direct reflection of the state of the hi_lfer variable in 126.3.6.2.2 for 2.5GBASE-T.<br>A latch high view of this status is reflected in MDIO register 3.33.14.<br>$0_B$ The 64B/65B receiver detects a BER below 10^-4.<br>$1_B$ The 64B/65B receiver detects a BER above or equal to 10^-4. |
| PCS2G5_BLO_LOCK | 0 | RO | **PCS 2G5 Block Lock**<br>$0_B$ 64B/65B receiver does not have block lock.<br>$1_B$ 64B/65B receiver has block lock. |

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The product (or product(s) mentioned in this

**MULTIGBASE-T PCS Status 2 (Register 3.33)**

**PCS_2G5_STAT2** **Reset Value**

**MULTIGBASE-T PCS Status 2 (Register 3.33)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| LATCHED_BLOCK_LOCK | 15 | RWSC | **Latched Block Lock**<br>$0_B$ PCS 2G5 does not have block lock.<br>$1_B$ PCS 2G5 has block lock. |
| LATCHED_HIGH_BER | 14 | RWSC | **Latched High BER**<br>$0_B$ PCS 2G5 did not report a high BER.<br>$1_B$ PCS 2G5 reported a high BER. |
| BER | 13:8 | RWSC | **BER**<br>BER counter |
| ERRED_BLK | 7:0 | RWSC | **Errored Blocks**<br>Errored blocks counter |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### PCS TimeSync Capability Register (Register 3.1800)

IEEE Standard Register=3.1800

**PCS_TIMESYNC_CAP** **Reset Value**

**PCS TimeSync Capability Register (Register 3.1800)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| TIMESYNC_TX_PATH_DATA_DELAY | 1 | RO | **TimeSync Transmit Path Data Delay**<br>$0_B$ PCS does not provide information on transmit path data delay. For the GPHY, the value is always 0.<br>$1_B$ PCS provides information on transmit path data delay in registers 3.1801 through 3.1804. |
| TIMESYNC_RX_PATH_DATA_DELAY | 0 | RO | **TimeSync Receive Path Data Delay**<br>$0_B$ PCS does not provide information on receive path data delay. For the GPHY, the value is always 0.<br>$1_B$ PCS provides information on receive path data delay in registers 3.1805 through 3.1808. |

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## 6.3 Standard Auto-Negotiation Registers for MMD=0x07

This register file contains the auto-negotiation registers for MMD device 0x07.

**Table 33 Registers Overview- Standard Auto-Negotiation Registers**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| ANEG_CTRL | Auto-Negotiation Control (Register 7.0) | $3000_H$ |
| ANEG_STAT | Auto-Negotiation Status (Register 7.1) | $0008_H$ |
| ANEG_DEVID1 | PHY Identifier 1 (Register 7.2) | $C133_H$ |
| ANEG_DEVID2 | PHY Identifier 2 (Register 7.3) | $5400_H$ 1) |
| ANEG_DIP1 | Device in Package 1 (Register 7.5) | $008B_H$ |
| ANEG_DIP2 | Device in Package 2 (Register 7.6) | $C000_H$ |
| ANEG_PACKID1 | AN Package Identifier (Register 7.14) | $C133_H$ |
| ANEG_PACKID2 | AN Package Identifier (Register 7.15) | $5400_H$ 1) |
| ANEG_ADV | ANEG Adv. for GPHY (Register 7.16) | $9DE1_H$ |
| ANEG_LP_BP_AB | AN Link Partner Base Page Ability (Register 7.19) | $0DE0_H$ |
| ANEG_XNP_TX1 | ANEG Local Dev XNP TX1 (Register 7.22) | $0001_H$ |
| ANEG_XNP_TX2 | ANEG Local Dev XNP TX2 (Register 7.23) | $0000_H$ |
| ANEG_XNP_TX3 | ANEG Local Dev XNP TX3 (Register 7.24) | $0000_H$ |
| ANEG_LP_XNP_AB1 | ANEG Link Partner XNP RX (Register 7.25) | $0000_H$ |
| ANEG_LP_XNP_AB2 | ANEG Link Partner XNP RX (Register 7.26) | $0000_H$ |
| ANEG_LP_XNP_AB3 | ANEG Link Partner XNP RX (Register 7.27) | $0000_H$ |
| ANEG_MGBT_AN_CTRL | MULTI GBT AN Control (Register 7.32) | $0082_H$ |
| ANEG_MGBT_AN_STA | MultiGBASE-T AN Status (Register 7.33) | $0000_H$ |
| ANEG_EEE_AN_ADV1 | EEE Advertisement 1 (Register 7.60) | $0006_H$ |
| ANEG_EEE_AN_LPAB1 | EEE Link Partner Ability 1 (Register 7.61) | $0000_H$ |
| ANEG_EEE_AN_ADV2 | EEE Advertisement 2 (Register 7.62) | $0001_H$ |
| ANEG_EEE_LP_AB2 | EEE Link Partner Ability 2 (Register 7.63) | $0001_H$ |
| ANEG_MGBT_AN_CTRL2 | MGBT ANEG Control 2 (Register 7.64) | $0008_H$ |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

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### 6.3.1 ANEG Register Descriptions

This section describes all the ANEG registers in detail.

**Auto-Negotiation Control (Register 7.0)**

The register controls the main function of auto-negotiation as defined in Clause 45. Refer to IEEE 802.3 45.2.7.1.

This register mirrors register STD_CTRL from Clause 22.

IEEE Standard Register=7.0

**ANEG_CTRL** **Reset Value**

**Auto-Negotiation Control (Register 7.0)** **$3000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 0 |
|---|---|---|---|---|---|---|---|---|
| RST | RES3 | XNP | ANEG_EN* | RES2 | | ANEG_RE* | RES1 | |
| rw | ro | rw | rw | ro | | rw | ro | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | RW | **Reset**<br>This bit resets the entire PHY to its default state. Active links are terminated. This is a self-clearing bit. The GPHY firmware sets the bit to 0 via the hardware when the reset is completed.<br>$0_B$ **NORMAL** Normal GPHY operation<br>$1_B$ **RESET** GPHY reset |
| RES3 | 14 | RO | **Reserved**<br>Value always 0, writes ignored. |
| XNP | 13 | RW | **Extended Next Page Control**<br>$0_B$ **ZERO** Extended next page is disabled.<br>$1_B$ **ONE** Extended next page is enabled. |
| ANEG_ENAB | 12 | RW | **Auto-Negotiation Enable**<br>This bit enables the ANEG process to determine the link configuration. Bit 7.0.12 is a copy of bit 0.12 in register 0 (STD_CTRL).<br>$0_B$ **ZERO** ANEG process is disabled.<br>$1_B$ **ONE** ANEG process is enabled. |
| RES2 | 11:10 | RO | **Reserved**<br>Value always zero, writes ignored. |
| ANEG_RESTART | 9 | RW | **Restart Auto-Negotiation**<br>The ANEG process is restarted by setting bit 7.0.9 to 1.Bit 7.0.9 is a mirror of bit 0.9 in register 0 (STD_CTRL).<br>Completion of ANEG is indicated in bit 0.1.5 and 7.1.5.<br>$0_B$ **ZERO** Normal operation<br>$1_B$ **RESTART** Restarts ANEG process. |
| RES1 | 8:0 | RO | **Reserved**<br>Value always 0, writes ignored. |

Data sheet are Not Recommended for New Designs (NRND) The Product (or products) mentioned in this

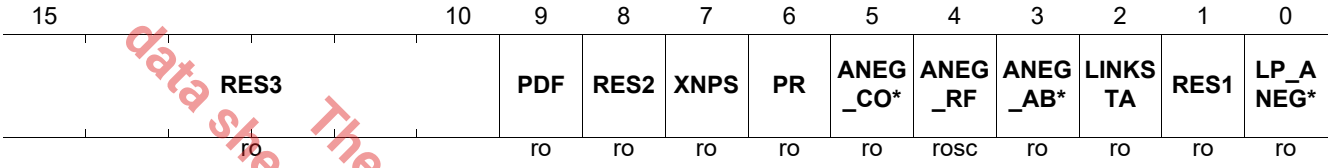
### Auto-Negotiation Status (Register 7.1)

All the bits in the ANEG_STA status register are read only and correspond to the outcome or current status of the auto-negotiation process.

IEEE Standard Register=7.1

**ANEG_STAT** **Reset Value**

**Auto-Negotiation Status (Register 7.1)** **$0008_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES3 | 15:10 | RO | **Reserved**<br>Value always zero, writes ignored. |
| PDF | 9 | RO | **Parallel Detection Fault**<br>$0_B$ **NOFAULT** No fault detected<br>$1_B$ **FAULT** Fault detected via the parallel mechanism |
| RES2 | 8 | RO | **Reserved**<br>Value always 0, writes ignored. |
| XNPS | 7 | RO | **Extended Next Page Status**<br>When set to $1_B$, bit 7.1.7 indicates that both the GPHY and the link partner confirmed support for extended next page. When set to $0_B$, bit 7.1.7 indicates that the extended next page feature is not used.<br>$0_B$ **ZERO** Extended next page is not allowed.<br>$1_B$ **ONE** Extended next page format is used. |
| PR | 6 | RO | **Page Received**<br>The Page Received bit (7.1.6) is set to $1_B$ to indicate that a new link codeword was received and stored in the AN LP Base Page ability registers 7.19 or AN LP XNP ability registers 7.25 to 7.27.<br>$0_B$ **ZERO** No page received<br>$1_B$ **ONE** Page received |
| ANEG_COMPLETE | 5 | RO | **Auto-Negotiation Complete**<br>When read as a 1, bit 7.1.5 indicates that the ANEG process was completed and that the contents of the ANEG registers 7.16 and 7.19 are valid. When read as a 0, bit 7.1.5 indicates that the ANEG process was not completed and that the contents of the 7.19, 7.22 through 7.27, and 7.33 registers are as defined by the current state of the ANEG protocol, or as written by manual configuration.<br>$0_B$ **ZERO** ANEG process not completed<br>$1_B$ **ONE** ANEG process completed |

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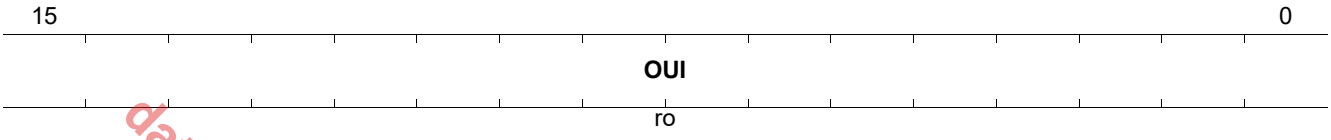
| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| ANEG_RF | 4 | ROSC | **Remote Fault**<br>When read as 1, bit 7.1.4 indicates that a remote fault condition was detected. Bit 7.1.4 is a copy of bit 1.4 in register 1, device 0.<br>$0_B$ **NORMAL** No remote fault condition detected<br>$1_B$ **FAULT** Remote fault condition detected |
| ANEG_ABLE | 3 | RO | **Auto-Negotiation Ability**<br>Bit 7.1.3 is a copy of bit 1.3 in register 1. This is the ANEG ability of the GPHY.<br>$0_B$ **UNABLE** PHY is not able to perform ANEG.<br>$1_B$ **ABLE** PHY is able to perform ANEG. |
| LINKSTA | 2 | RO | **Link Status**<br>When read as $1_B$, bit 7.1.2 indicates that the PMA/PMD determined that a valid link is established. This bit is a duplicate of the PMA/PMD link status bit in 1.1.2. This bit latches low so it does not represent the current status, but is used to indicate link drop since the last read from the management interface. Reading this bit from the MDIO resets the bit to the current value of the link.<br>$0_B$ **DOWN** Link is down.<br>$1_B$ **UP** Link is up. |
| RES1 | 1 | RO | **Reserved**<br>Value always 0, write ignored. |
| LP_ANEG_ABLE | 0 | RO | **Link Partner Auto-Negotiation Ability**<br>$0_B$ **UNABLE** Link partner is not capable of ANEG.<br>$1_B$ **ABLE** Link partner is capable of ANEG. |

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The product(s) mentioned in this

**PHY Identifier 1 (Register 7.2)**

**ANEG_DEVID1** **Reset Value**

**PHY Identifier 1 (Register 7.2)** **C133$_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier** |

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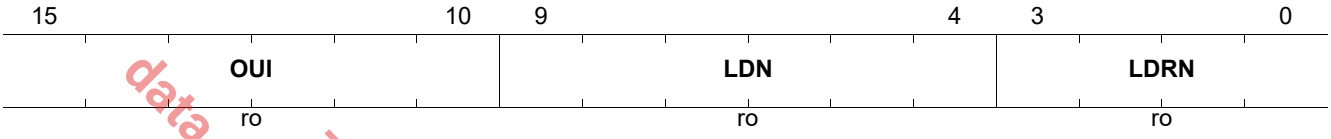
**PHY Identifier 2 (Register 7.3)**

Organizationally Unique Identifier

IEEE Standard Register=7.3

**ANEG_DEVID2** **Reset Value**

**PHY Identifier 2 (Register 7.3)** **$5400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several different products. |
| LDRN | 3:0 | RO | **Device Revision Number**<br>Specifies the device revision number[1)] to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

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**Device in Package 1 (Register 7.5)**

IEEE Standard Register=7.5

**ANEG_DIP1** **Reset Value**

**Device in Package 1 (Register 7.5)** **$008B_H$**

| 15 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | | PMA4 | PMA3 | PMA2 | PMA1 | ANEG | TC | DTEXS | PHYXS | PCS | WIS | PMAPMD | CL22 |
| ro | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:12 | RO | **Reserved**<br>Ignore on read. |
| PMA4 | 11 | RO | **Separate PMA4 Present in Package**<br>$0_B$ **ABSENT** Separate PMA4 not present in package<br>$1_B$ **PRESENT** Separate PMA4 present in package |
| PMA3 | 10 | RO | **Separate PMA3 Present in Package**<br>$0_B$ **ABSENT** Separate PMA3 not present in package<br>$1_B$ **PRESENT** Separate PMA3 present in package |
| PMA2 | 9 | RO | **Separate PMA2 Present in Package**<br>$0_B$ **ABSENT** Separate PMA2 not present in package<br>$1_B$ **PRESENT** Separate PMA2 present in package |
| PMA1 | 8 | RO | **Separate PMA1 Present in Package**<br>$0_B$ **ABSENT** Separate PMA1 not present in package<br>$1_B$ **PRESENT** Separate PMA1 present in package |
| ANEG | 7 | RO | **Auto-Negotiation Present in Package**<br>$0_B$ **ABSENT** ANEG not present in package<br>$1_B$ **PRESENT** ANEG present in package |
| TC | 6 | RO | **TC Present in Package**<br>$0_B$ **ABSENT** TC registers not present in package<br>$1_B$ **PRESENT** TC registers present in package |
| DTEXS | 5 | RO | **DTE XS Present in Package**<br>$0_B$ **ABSENT** DTE XS registers not present in package<br>$1_B$ **PRESENT** DTE XS registers present in package |
| PHYXS | 4 | RO | **PHYXS Present in Package**<br>$0_B$ **ABSENT** PHYXS registers not present in package<br>$1_B$ **PRESENT** PHYXS registers present in package |
| PCS | 3 | RO | **PCS Present in Package**<br>$0_B$ **ABSENT** PCS registers not present in package<br>$1_B$ **PRESENT** PCS registers present in package |
| WIS | 2 | RO | **WIS Present in Package**<br>$0_B$ **ABSENT** WIS registers present in package<br>$1_B$ **PRESENT** WIS registers present in package |

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The product(s) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| PMAPMD | 1 | RO | **PMA PMD Present in Package**<br>$0_B$ **ABSENT** PMA PMD registers not present in package<br>$1_B$ **PRESENT** PMA PMD registers present in package |
| CL22 | 0 | RO | **Clause 22 Register Present in Package**<br>$0_B$ **ABSENT** Clause 22 registers no present in package<br>$1_B$ **PRESENT** Clause 22 registers present in package |

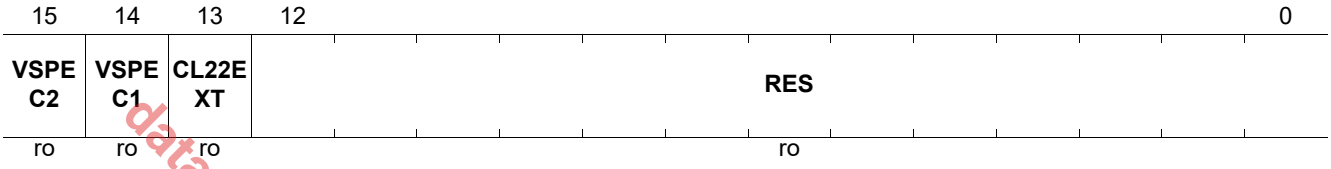
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**Device in Package 2 (Register 7.6)**

IEEE Standard Register=7.6

**ANEG_DIP2** **Reset Value**

**Device in Package 2 (Register 7.6)** **$C000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| VSPEC2 | 15 | RO | **Vendor Specific Device 2 Present in Package**<br>$0_B$ **ABSENT** Vendor Specific Device 2 not present in package<br>$1_B$ **PRESENT** Vendor Specific Device 2 present in package |
| VSPEC1 | 14 | RO | **Vendor Specific Device 1 Present in Package**<br>$0_B$ **ABSENT** Vendor Specific Device 1 not present in package<br>$1_B$ **PRESENT** Vendor Specific Device 1 present in package |
| CL22EXT | 13 | RO | **Clause 22 Extension Present in Package**<br>$0_B$ **ABSENT** Clause 22 extension not present in package<br>$1_B$ **PRESENT** Clause 22 extension present in package |
| RES | 12:0 | RO | **Reserved**<br>Ignore on read. |

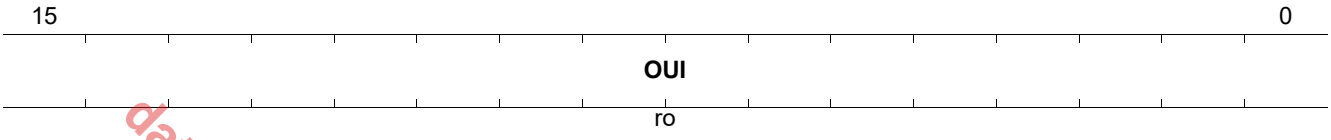
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### AN Package Identifier (Register 7.14)

IEEE Standard Register=7.14

**ANEG_PACKID1** **Reset Value**

**AN Package Identifier (Register 7.14)** **C133$_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:0 | RO | **Organizationally Unique Identifier Bits 3:18** |

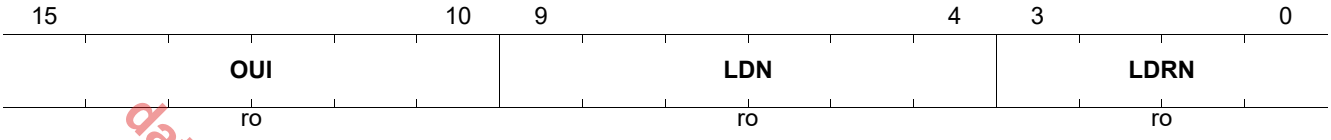
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

**AN Package Identifier (Register 7.15)**

IEEE Standard Register=7.15

**ANEG_PACKID2** **Reset Value**

**AN Package Identifier (Register 7.15)** **$5400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| OUI | 15:10 | RO | **Organizationally Unique Identifier Bits 19:24** |
| LDN | 9:4 | RO | **Device Number**<br>Specifies the device number[1)] to distinguish between several different products. |
| LDRN | 3:0 | RO | **Device Revision Number**<br>Specifies the device revision number[1)] to distinguish between several versions of this device. |

1) For the device specific reset value, see the Product and Package Naming table in the **Product Ordering Information** chapter.

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

### ANEG Adv. for GPHY (Register 7.16)

This register is a copy of the ANEG advertisement register (Register 4). A read to the AN advertisement register (7.16) reports the value of the ANEG advertisement register (Register 4). Writes to the AN advertisement register (7.16) cause a write to occur to the ANEG advertisement register (Register 4).

IEEE Standard Register=7.16

**ANEG_ADV** **Reset Value**

**ANEG Adv. for GPHY (Register 7.16)** **$9DE1_H$**

| 15 | 14 | 13 | 12 | 11 … 5 | 4 … 0 |
|---|---|---|---|---|---|
| **NP** | **RES** | **RF** | **XNP** | **TAF** | **SF** |
| rw | ro | rw | rw | rw | rw |

datasheet are not recommended for New Designs (NRND)

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page Able**<br>$0_B$ **INACTIVE** No next page allowed.<br>$1_B$ **ACTIVE** Additional next page(s) to follow. |
| RES | 14 | RO | **Reserved**<br>Write as zero, ignore on read. |
| RF | 13 | RW | **Remote Fault**<br>The remote fault bit allows indication of a fault to the link partner. Refer to IEEE 802.3 28.2.1.2.4. |
| XNP | 12 | RW | **Transmission of Extended Next Pages**<br>Indicates that the GPHY is able to transmit extended next pages.<br>$0_B$ **UNABLE** GPHY is XNP unable.<br>$1_B$ **ABLE** GPHY is XNP able. |
| TAF | 11:5 | RW | **Technology Ability Field**<br>The technology ability field is an 8-bit wide field containing information indicating supported technologies. The GPHY supports 10BASE-T (half- and full-duplex), 100BASE-TX (half- and full-duplex), and both symmetric and asymmetric PAUSE.<br>$40_H$ **PS_ASYM** Advertises asymmetric pause<br>$20_H$ **PS_SYM** Advertises symmetric pause<br>$10_H$ **DBT4** Advertises 100BASE-T4<br>$08_H$ **DBT_FDX** Advertises 100BASE-TX full-duplex<br>$04_H$ **DBT_HDX** Advertises 100BASE-TX half-duplex<br>$02_H$ **XBT_FDX** Advertises 10BASE-T full-duplex<br>$01_H$ **XBT_HDX** Advertises 10BASE-T half-duplex |
| SF | 4:0 | RW | **Selector Field**<br>This field is always set to $00001_B$ because the GPHY only supports the 802.3 Ethernet standard.<br>$00001_B$**IEEE8023** IEEE 802.3 technology. |

The product (or products) mentioned in this

### AN Link Partner Base Page Ability (Register 7.19)

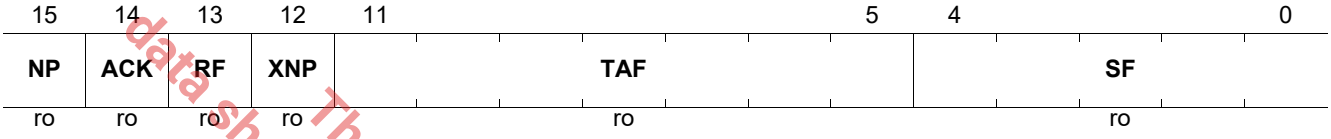
Register 7.19 is a copy of register 5 from Clause 28. It contains the Base Page received from the link partner.

All of the bits in the AN LP Base Page Ability register are read only.

IEEE Standard Register=7.19

**ANEG_LP_BP_AB** **Reset Value**

**AN Link Partner Base Page Ability (Register 7.19)** **$0DE0_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Link Partner Next Page**<br>Next page request indication from the link partner.<br>$0_B$ **INACTIVE** No next page to follow<br>$1_B$ **ACTIVE** Additional next page to follow |
| ACK | 14 | RO | **Link Partner Acknowledge**<br>Acknowledgment indication from the link partner's link code word.<br>$0_B$ **INACTIVE** Device did not successfully receive its link partner's link code word.<br>$1_B$ **ACTIVE** Device successfully received its link partner's link code word. |
| RF | 13 | RO | **Link Partner Remote Fault**<br>Remote fault indication from the link partner.<br>$0_B$ **NONE** Remote fault is not indicated by the link partner.<br>$1_B$ **FAULT** Remote fault is indicated by the link partner. |
| XNP | 12 | RO | **Link Partner XNP Ability**<br>$0_B$ **UNABLE** Link partner is not XNP able.<br>$1_B$ **ABLE** Link partner is XNP able. |
| TAF | 11:5 | RO | **Technology Ability Field**<br>These bits indicate the link partner's supported technologies received in the Base Page.<br>$40_H$ **PS_ASYM** Advertises asymmetric pause<br>$20_H$ **PS_SYM** Advertises symmetric pause<br>$10_H$ **DBT4** Advertises 100BASE-T4<br>$08_H$ **DBT_FDX** Advertises 100BASE-TX full-duplex<br>$04_H$ **DBT_HDX** Advertises 100BASE-TX half-duplex<br>$02_H$ **XBT_FDX** Advertises 10BASE-T full-duplex<br>$01_H$ **XBT_HDX** Advertises 10BASE-T half-duplex |

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

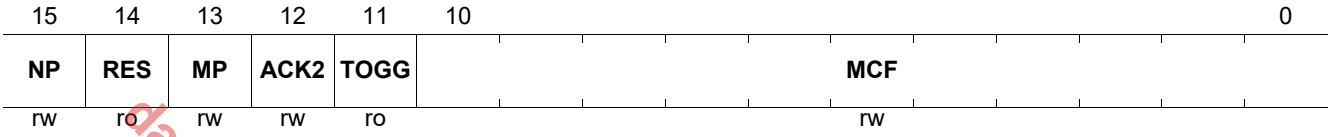
| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| SF | 4:0 | RO | **Link Partner Selector Field**<br>This selector field represents one of the 32 possible messages with encoding definitions defined in IEEE 802.3 Annex 28A.<br>$00_H$ Reserved<br>$01_H$ IEEE 802.3<br>$02_H$ IEEE 802.9 ISLAN-16T<br>$03_H$ IEEE 802.5<br>$04_H$ IEEE 1394<br>$05_H$ Reserved<br>...<br>$1F_H$ Reserved |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### ANEG Local Dev XNP TX1 (Register 7.22)

**ANEG_XNP_TX1** **Reset Value**

**ANEG Local Dev XNP TX1 (Register 7.22)** **$0001_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RW | **Next Page**<br>When the NP bit is set, the GPHY requests to transmit one additional page. The next page transmission ends when both ends of a link segment set their next page bits to logic 0, indicating that neither has anything additional to transmit.<br>$0_B$ **INACTIVE** No next page to follow.<br>$1_B$ **ACTIVE** Additional next page(s) to follow. |
| RES | 14 | RO | **Reserved**<br>Write as 0, ignore on read. |
| MP | 13 | RW | **Message Page**<br>Message Page (MP) is used by the next page function to differentiate a MP from an UP. Only MPs are used by the GPHY.<br>$0_B$ **UNFOR** Unformatted Page<br>$1_B$ **MESSG** Message Page |
| ACK2 | 12 | RW | **Acknowledge 2**<br>Not used during GPHY ANEG.<br>$0_B$ **INACTIVE** Device does not comply with message.<br>$1_B$ **ACTIVE** Device complies with message. |
| TOGG | 11 | RO | **Toggle**<br>The Toggle bit is used to ensure proper synchronization between the GPHY and the link partner.<br>$0_B$ **ZERO** Previous value of the Tx LCW was $1_B$.<br>$1_B$ **ONE** Previous value of the Tx LCW was $0_B$. |

data sheet are Not Recommended for New Designs (NRND)
The product(or products) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| MCF | 10:0 | RW | **Message Code Field**<br>When the Message Page bit is set to $1_B$ (7.16.1), this field is the Message Code Field of a message page used in a next page exchange. The message codes are described in IEEE 802.3 Appendix 28C.<br>This is used to indicate the type of message in UCF1 and UCF2.<br>$00_H$ Reserved<br>$01_H$ Null message<br>$02_H$ One Unformatted Page (UP) with TAF follows<br>$03_H$ Two UPs with TAF follows<br>$04_H$ Remote fault details message<br>$05_H$ OUI message<br>$06_H$ PHY ID message<br>$07_H$ 100BASE-T2 message<br>$08_H$ 1000BASE-T message<br>$09_H$ MULTIGBASE-T message<br>$0A_H$ EEE technology capability follows in next UP<br>$0B_H$ OUI XNP |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

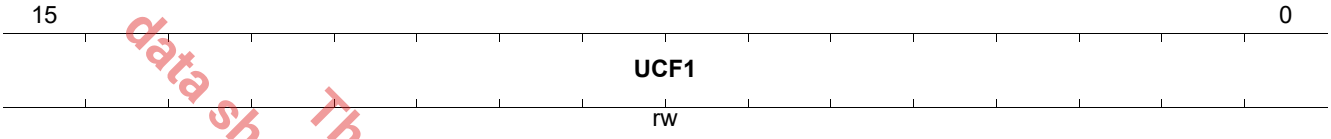
**ANEG Local Dev XNP TX2 (Register 7.23)**

Unformatted code field 1 contains seed information and advertises support of 1 GBT full-duplex and half-duplex. Refer to 28.2.3.4.

IEEE Standard Register=7.23

**ANEG_XNP_TX2** **Reset Value**

**ANEG Local Dev XNP TX2 (Register 7.23)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| UCF1 | 15:0 | RW | **Unformatted Code Field 1**<br>Transmits the master-slave seed bit to facilitate ANEG resolution, port type, and duplex capability. |

data sheet are Not Recommended for New Designs (NRND)
The product(s) or products(s) mentioned in this

**ANEG Local Dev XNP TX3 (Register 7.24)**

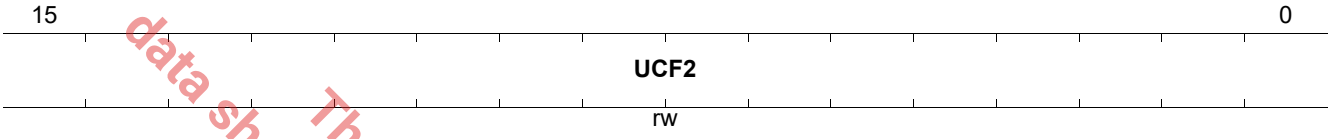
Unformatted code field 2 - Register 7.24

Refer to 28.2.3.4.

IEEE Standard Register=7.24

**ANEG_XNP_TX3** **Reset Value**

**ANEG Local Dev XNP TX3 (Register 7.24)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| UCF2 | 15:0 | RW | **Unformatted Code Field 2**<br>2.5 GBASE-T ability is advertised by default. |

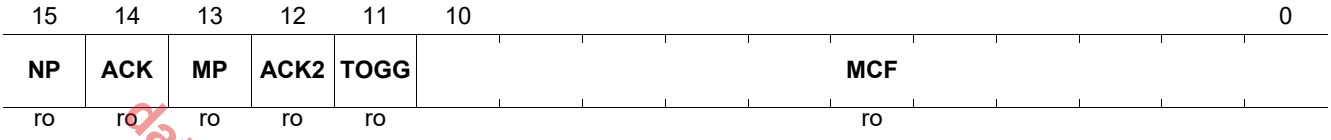
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

**ANEG Link Partner XNP RX (Register 7.25)**

IEEE Standard Register=7.25

**ANEG_LP_XNP_AB1** **Reset Value**

**ANEG Link Partner XNP RX (Register 7.25)** **$0000_H$**




data sheet are Not Recommended for New Designs (NRND)
The product (or product(s) mentioned in this

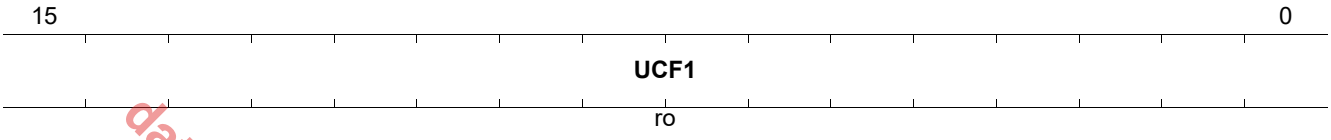
| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | RO | **Link Partner Next Page**<br>Refer to 28.2.3.4.3.<br>The NP bit is used by the next page function to indicate whether or not this is the last next page to be transmitted.<br>$0_B$ **INACTIVE** Last page<br>$1_B$ **ACTIVE** Additional next page(s) to follow |
| ACK | 14 | RO | **Link Partner Acknowledge**<br>As defined in 28.2.1.2.5.<br>The Acknowledge (Ack) bit is used by the ANEG function to indicate that the GPHY successfully received its link partner's link codeword. |
| MP | 13 | RO | **Link Partner Message Page**<br>Indicates that the content of MCF is either an unformatted page or a formatted message.<br>$0_B$ **UNFOR** Unformatted page<br>$1_B$ **MESSG** Message page |
| ACK2 | 12 | RO | **Link Partner Acknowledge 2**<br>$0_B$ **INACTIVE** Device is unable to comply with message.<br>$1_B$ **ACTIVE** Device complies with message. |
| TOGG | 11 | RO | **Link Partner Toggle**<br>This bit is set to the opposite of the TOGG bit in the previous page.<br>$0_B$ **ZERO** Previous value of the TX LCW was $1_B$.<br>$1_B$ **ONE** Previous value of the TX LCW was $0_B$. |
| MCF | 10:0 | RO | **Link Partner Message Code Field**<br>This field indicates the type of Message Code.<br>$009_H$ **MC_2G5BT** Message code for 2.5GBASE-T |

### ANEG Link Partner XNP RX (Register 7.26)

IEEE Standard Register=7.26

**ANEG_LP_XNP_AB2** **Reset Value**

**ANEG Link Partner XNP RX (Register 7.26)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| UCF1 | 15:0 | RO | **Unformatted Code Field 1**<br>Refer to 28.2.3.4. |

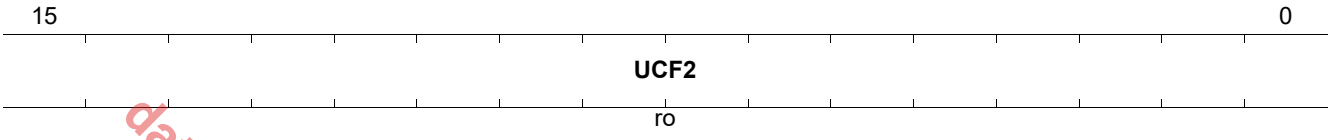
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

### ANEG Link Partner XNP RX (Register 7.27)

IEEE Standard Register=7.27

**ANEG_LP_XNP_AB3** **Reset Value**

**ANEG Link Partner XNP RX (Register 7.27)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| UCF2 | 15:0 | RO | **Unformatted Code Field 2**<br>Refer to 28.2.3.4. |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

**MULTI GBT AN Control Register (Register 7.32)**

This register advertises the GPHY capabilities.

IEEE Standard Register=7.32

**ANEG_MGBT_AN_CTRL** **Reset Value**

**MULTI GBT AN Control Register (Register 7.32)** **$0082_H$**

| 15 | 14 | 13 | 12 | 11 9 | 8 | 7 | 6 | 5 | 4 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MS_MAN_* | MSCV | PT | AB_10GBT | RES2 | AB_5GBT | AB_2G5BT | FR_5GBT | FR_2G5BT | RES1 | LDPMA | FR | LDL |
| rw | rw | rw | ro | ro | ro | rw | ro | rw | ro | rw | rw | rw |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| MS_MAN_EN | 15 | RW | **Master Slave Manual Config Enable**<br>$0_B$ **ANEG** ANEG is used to determine the master-slave selection.<br>$1_B$ **MAN** Manual configuration. The MSCV bit determines the master-slave selection. |
| MSCV | 14 | RW | **Master Slave Config Value**<br>$0_B$ **SLAVE** Manual set to SLAVE<br>$1_B$ **MASTER** Manual set to MASTER |
| PT | 13 | RW | **Port Type**<br>$0_B$ **MASTER** Preference as Master - single port device<br>$1_B$ **SLAVE** Preference as Slave - multi-port device |
| AB_10GBT | 12 | RO | **10GBASE-T Ability**<br>Not supported. Value always 0. |
| RES2 | 11:9 | RO | **Reserved**<br>Value always 0, writes ignored. |
| AB_5GBT | 8 | RO | **5GBASE-T Ability**<br>Not supported by the GPHY.<br>$0_B$ **UNABLE** Do not advertise PHY as 5GBASE-T capable.<br>$1_B$ **ABLE** Advertises PHY as 5GBASE-T capable. Not supported. |
| AB_2G5BT | 7 | RW | **2.5GBASE-T Ability**<br>$0_B$ **UNABLE** Do not advertise PHY as 2.5GBASE-T capable.<br>$1_B$ **ABLE** Advertises PHY as 2.5GBASE-T capable. |
| FR_5GBT | 6 | RO | **5GBASE-T Fast Retrain Ability**<br>Not supported by GPHY.<br>$0_B$ **UNABLE** Do not advertise PHY as 5GBASE-T fast retrain able.<br>$1_B$ **ABLE** Advertises PHY as 5GBASE-T fast retrain capable. Not supported. |
| FR_2G5BT | 5 | RW | **2.5GBASE-T Fast Retrain Ability**<br>$0_B$ **UNABLE** Do not advertise PHY as 2.5G fast retrain able.<br>$1_B$ **ABLE** Advertises PHY as 2.5G fast retrain able. |
| RES1 | 4:3 | RO | **Reserved**<br>Value always 0, writes ignored. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LDPMA | 2 | RW | **GPHY PMA Training Reset Request**<br>When this bit is set to $1_B$, the GPHY expects the link partner to reset the PMA training PRBS for every PMA training frame.<br>When this bit is set to $0_B$, the GPHY expects the link partner to run the PMA training PRBS continuously through every PMA training frame. |
| FR | 1 | RW | **Fast Retrain Ability** |
| LDL | 0 | RW | **GPHY Loop Timing Ability** |

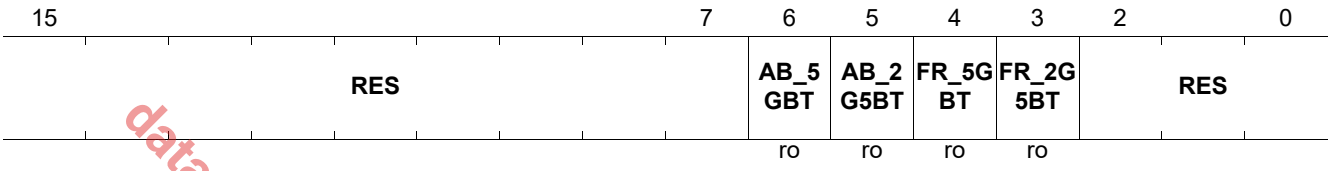
The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

### MultiGBASE-T AN Status Register (Register 7.33)

IEEE Standard Register=7.33

**ANEG_MGBT_AN_STA** **Reset Value**

**MultiGBASE-T AN Status register (Register 7.33)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| AB_5GBT | 6 | RO | **5GBASE-T Ability of Link Partner**<br>This bit is only valid when the link is established and ANEG completed.<br>$0_B$ **UNABLE** Link partner is not capable of 5GBASE-T.<br>$1_B$ **ABLE** Link partner is capable of 5GBASE-T. |
| AB_2G5BT | 5 | RO | **2.5GBASE-T Ability of Link Partner**<br>This bit is only valid when the link is established and ANEG completed (bit 7.1.5 is set to $1_B$).<br>$0_B$ **UNABLE** Link partner is not capable of 2.5GBASE-T.<br>$1_B$ **ABLE** Link partner is capable of 2.5GBASE-T. |
| FR_5GBT | 4 | RO | **5GBASE-T Fast Retrain Ability of Link Partner**<br>This bit is only valid when the link is established and ANEG completed.<br>$0_B$ **UNABLE** Link partner is not capable of 5GBASE-T fast retrain.<br>$1_B$ **ABLE** Link partner is capable of 5GBASE-T fast retrain |
| FR_2G5BT | 3 | RO | **2.5GBASE-T Fast Retrain Ability of Link Partner**<br>This bit is only valid when the link is established and ANEG completed (bit 7.1.5 is set to $1_B$).<br>$0_B$ **UNABLE** Link partner is not capable of 2.5GBASE-T fast retrain.<br>$1_B$ **ABLE** Link partner is capable of 2.5GBASE-T fast retrain. |

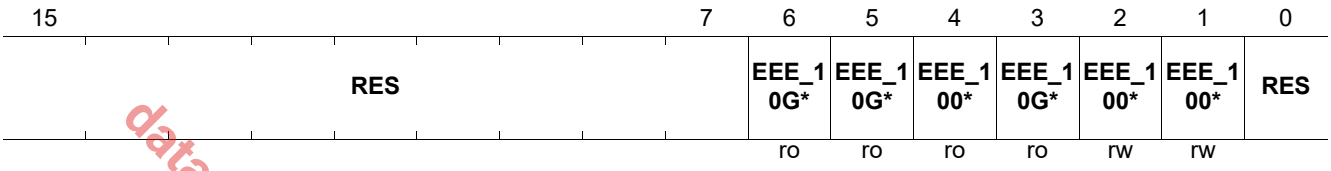
data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

**EEE Advertisement 1 (Register 7.60)**

IEEE Standard Register=7.60

**ANEG_EEE_AN_ADV1** **Reset Value**

**EEE Advertisement 1 (Register 7.60)** **$0006_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| EEE_10GBKR | 6 | RO | **Support of 10GBASE-KR EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_10GBKX4 | 5 | RO | **Support of 10GBASE-KX4 EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_1000BKX | 4 | RO | **Support of 1000BASE-KX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_10GBT | 3 | RO | **Support of 10GBASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_1000BT | 2 | RW | **Support of 1000BASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_100BTX | 1 | RW | **Support of 100BASE-TX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |

data sheet are Not Recommended for New Designs (NRND)
The product (or product(s) mentioned in this

### EEE Link Partner Ability 1 (Register 7.61)

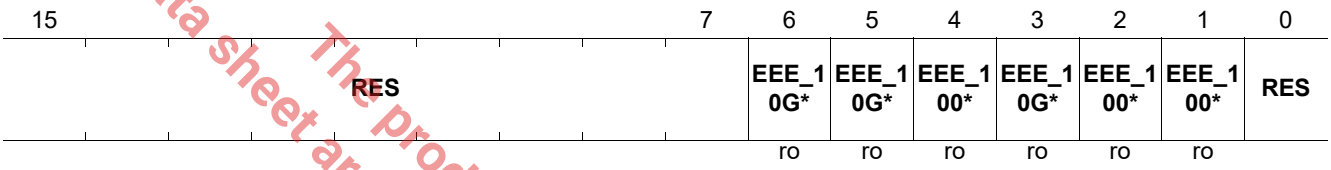
After the AN process is completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE AN advertisement 1 register.

IEEE Standard Register=7.61

All of the bits in the EEE LP ability 1 register are read only. A write operation to the EEE LP advertisement register has no effect.

**ANEG_EEE_AN_LPAB1** **Reset Value**

**EEE Link Partner Ability 1 (Register 7.61)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| EEE_10GBKR | 6 | RO | **Support of 10GBASE-KR EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_10GBKX4 | 5 | RO | **Support of 10GBASE-KX4 EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_1000BKX | 4 | RO | **Support of 1000BASE-KX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_10GBT | 3 | RO | **Support of 10GBASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_1000BT | 2 | RO | **Support of 1000BASE-T EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |
| EEE_100BTX | 1 | RO | **Support of 100BASE-TX EEE**<br>$0_B$ **DISABLED** This PHY mode is not supported for EEE.<br>$1_B$ **ENABLE** This PHY mode is supported for EEE. |

data sheet are Not Recommended for New Design (NRND)
The product (or products) mentioned in this

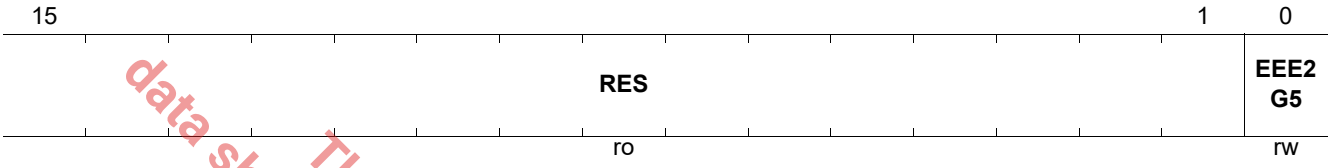
**EEE Advertisement 2 (Register 7.62)**

EEE advertisement 2 register is a continuation of EEE advertisement 1 register.

IEEE Standard Register=7.62

**ANEG_EEE_AN_ADV2** **Reset Value**

**EEE Advertisement 2 (Register 7.62)** **$0001_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:1 | RO | **Reserved** |
| EEE2G5 | 0 | RW | **Advertise 2.5GBASE-T EEE Capability**<br>$0_B$ **DISABLED** This PHY mode does not advertise 2.5GBASE-T EEE.<br>$1_B$ **ENABLE** This PHY mode advertises 2.5GBASE-T EEE. |

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The product(s) mentioned in this

### EEE Link Partner Ability 2 (Register 7.63)

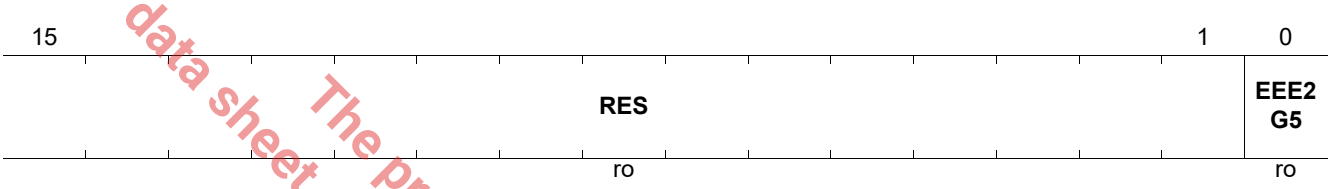
When the AN and training processes are complete, this register reflects the contents of the link partner's EEE advertisement 2 register.

IEEE Standard Register=7.63

All the bits in the EEE LP Ability 2 register are read-only. A write to the EEE LP Ability 2 register has no effect.

**ANEG_EEE_LP_AB2** **Reset Value**

**EEE Link Partner Ability 2 (Register 7.63)** **$0001_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 15:1 | RO | **Reserved** |
| EEE2G5 | 0 | RO | **Link Partner Advertised 2.5GBASE-T EEE Capability**<br>$0_B$ **DISABLED** LP is not 2.5GBASE-T EEE capable.<br>$1_B$ **ENABLE** LP is 2.5GBASE-T EEE capable. |

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**MGBT ANEG Control 2 (Register 7.64)**

This register is an extension of the ANEG Control Register for Multi GBT. It is used for 2.5 G ANEG configuration.

IEEE Standard Register=7.64

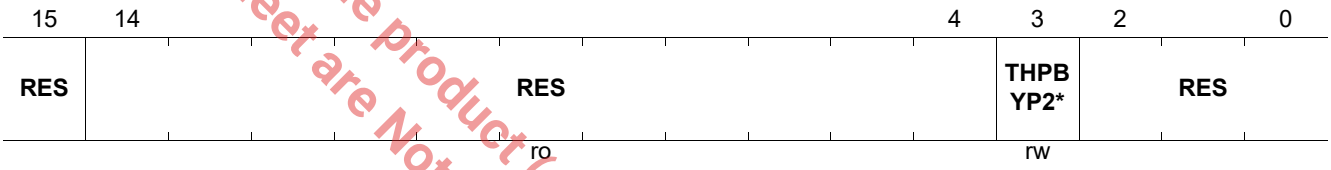
Bit 7.64.3 is valid only when 7.32.5 is set to $1_B$ advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, refer to 126.4.2.5.10.

When bit 7.64.3 is set to $0_B$, the GPHY requests the link partner not to reset THP during fast retrain.

When bit 7.64.3 is set to $1_B$, the GPHY requests the link partner to initially reset THP during fast retrain.

**ANEG_MGBT_AN_CTRL2** **Reset Value**

**MGBT ANEG Control 2 (Register 7.64)** **$0008_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| RES | 14:4 | RO | **Reserved** |
| THPBYP2G5 | 3 | RW | **THP Bypass During Fast Retrain**<br>The GPHY requests a THP bypass during fast retrain.<br>$0_B$ **NORST** GPHY requests the link partner NOT to initially reset THP during fast retrain.<br>$1_B$ **RST** GPHY requests the link partner to initially reset THP during fast retrain. |

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The product (or products) mentioned in this

## 6.4 Vendor Specific 1 Device Registers

This register file contains GPHY-specific registers for MMD=30 (decimal).

**Table 34 Registers Overview- Vendor Specific 1 Device Registers**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| VSPEC1_LED0 | Configuration for LED Pin 0 (Register 30.1) | $0310_H$ |
| VSPEC1_LED1 | Configuration for LED Pin 1 (Register 30.2) | $0320_H$ |
| VSPEC1_LED2 | Configuration for LED Pin 2 (Register 30.3) | $0340_H$ |
| VSPEC1_TXS_SCL_OFFSET | PHY Transmit Amplitude Control Register (Register 30.8) | $0000_H$ |
| VSPEC1_NBT_DS_CTRL | NBASE-T Downshift Control Register (Register 30.10) | $0400_H$ |
| VSPEC1_NBT_DS_STA | NBASE-T Downshift Status Register (Register 30.11) | $0000_H$ |
| VSPEC1_PM_CTRL | Packet Manager Control (Register 30.12) | $3000_H$ |
| VSPEC1_TEMP_STA | Temperature Code (Register 30.14) | $0000_H$ |
| VSPEC1_IMASK | VSPEC1 Interrupt Mask Register (Register 30.17) | $0000_H$ |
| VSPEC1_ISTAT | VSPEC1 Interrupt Mask Register (Register 30.18) | $0000_H$ |
| VSPEC1_LANE_ASP_MAP | ASP Mapping to Physical Lanes (Register 30.20) | $00E4_H$ |
| VSPEC1_LOW_POWER_ENTRY_TIME | Time to Enter Low Power (Register 30.21) | $0001_H$ |
| VSPEC1_FRCTL | Fast Retrain Control and Status (Register 30.22) | $0000_H$ |

Data sheet are Not Recommended for New Designs (NRND)
The product(or products) mentioned in this

### 6.4.1 VSPEC1 Register Descriptions

This section describes all the VSPEC1 registers in detail.

**Configuration for LED Pin 0 (Register 30.1)**

This register configures the behavior of the LED0 pin depending on predefined states or events the PHY entered into or raised. Since more than one event/state may be active at the same time, more than one function may apply at the same time. The priority from highest to lowest is given by the order: PULSE, BLINKS, BLINKF, and CON. The LED PULSE for the selected activity is only displayed for the link speed selected in CON. When CON is selected as NONE, no PULSE is displayed on the LED for any activity. To avoid the LED being constantly on when it is configured for pulsing alone, set the NO_CON bit in the PULSE field (bit 11).

IEEE Standard Register=30.1

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The Product(or products) mentioned in this

**VSPEC1_LED0** **Reset Value**

**Configuration for LED Pin 0 (Register 30.1)** **$0310_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| BLINKS | 15:12 | RW | **Slow Blinking Configuration**<br>The BLINKS field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not active<br>$0001_B$**LINK10** Blink when link is 10 Mbps.<br>$0010_B$**LINK100** Blink when link is 100 Mbps.<br>$0100_B$**LINK1000** Blink when link is 1000 Mbps.<br>$1000_B$**LINK2500** Blink when link is 2500 Mbps. |
| PULSE | 11:8 | RW | **Pulsing Configuration**<br>The PULSE field is a mask field that combines certain events, such as TXACT\|RXACT, to generate a pulse on the LED when such an event is detected.<br>$0000_B$**NONE** No pulsing<br>$0001_B$**TXACT** Transmit activity<br>$0010_B$**RXACT** Receive activity<br>$0100_B$**COL** Collision<br>$1000_B$**NO_CON** Constant on behavior is switched off. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| CON | 7:4 | RW | **Constant On Configuration**<br>The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not active<br>$0001_B$**LINK10** On when link is 10 Mbps.<br>$0010_B$**LINK100** On when link is 100 Mbps.<br>$0100_B$**LINK1000** On when link is 1000 Mbps.<br>$1000_B$**LINK2500** On when link is 2500 Mbps. |
| BLINKF | 3:0 | RW | **Fast Blinking Configuration**<br>The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** No active<br>$0001_B$**LINK10** Blink when Link is 10 Mbps.<br>$0010_B$**LINK100** Blink when Link is 100 Mbps.<br>$0100_B$**LINK1000** Blink when Link is 1000 Mbps.<br>$1000_B$**LINK2500** Blink when Link is 2500 Mbps. |

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The product(s) mentioned in this

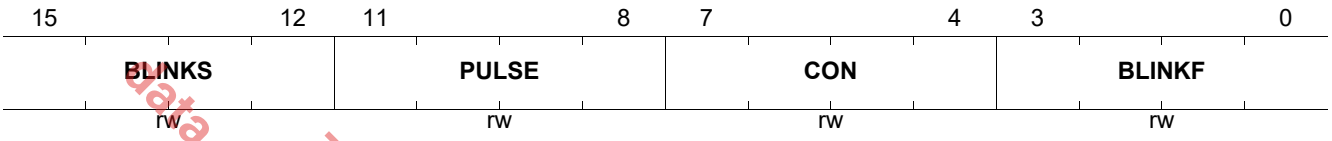
**Configuration for LED Pin 1 (Register 30.2)**

Configuration register for LED pin 1

IEEE Standard Register=30.2

**VSPEC1_LED1** **Reset Value**

**Configuration for LED Pin 1 (Register 30.2)** **$0320_H$**




Data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| BLINKS | 15:12 | RW | **Slow Blinking Configuration**<br>The BLINKS field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not active<br>$0001_B$**LINK10** Blink when link is 10 Mbps.<br>$0010_B$**LINK100** Blink when link is 100 Mbps.<br>$0100_B$**LINK1000** Blink when link is 1000 Mbps.<br>$1000_B$**LINK2500** Blink when link is 2500 Mbps. |
| PULSE | 11:8 | RW | **Pulsing Configuration**<br>The PULSE field is a mask field that combines certain events, such as TXACT\|RXACT, to generate a pulse on the LED when such an event is detected.<br>$0000_B$**NONE** No pulsing<br>$0001_B$**TXACT** Transmit activity<br>$0010_B$**RXACT** Receive activity<br>$0100_B$**COL** Collision<br>$1000_B$**NO_CON** Constant on behavior is switched off. |
| CON | 7:4 | RW | **Constant On Configuration**<br>The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not active<br>$0001_B$**LINK10** On when link is 10 Mbps.<br>$0010_B$**LINK100** On when link is 100 Mbps.<br>$0100_B$**LINK1000** On when link is 1000 Mbps.<br>$1000_B$**LINK2500** On when link is 2500 Mbps. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| BLINKF | 3:0 | RW | **Fast Blinking Configuration**<br>The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not active<br>$0001_B$**LINK10** Blink when link is 10 Mbps.<br>$0010_B$**LINK100** Blink when link is 100 Mbps.<br>$0100_B$**LINK1000** Blink when link is 1000 Mbps.<br>$1000_B$**LINK2500** Blink when link is 2500 Mbps. |

The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

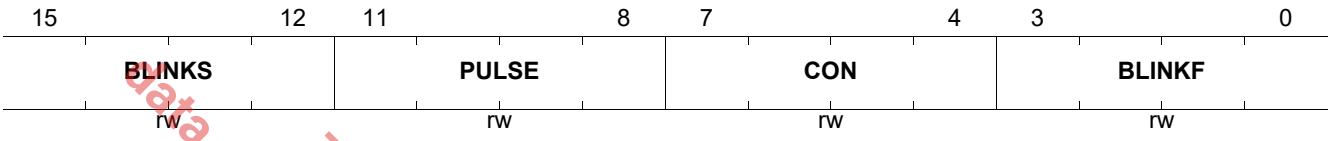
**Configuration for LED Pin 2 (Register 30.3)**

Configuration register for LED pin 2

IEEE Standard Register=30.3

**VSPEC1_LED2** **Reset Value**

**Configuration for LED Pin 2 (Register 30.3)** **$0340_H$**




Data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

| Field | Bits | Type | Description |
|---|---|---|---|
| BLINKS | 15:12 | RW | **Slow Blinking Configuration**<br>The BLINKS field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not active<br>$0001_B$**LINK10** Blink when link is 10 Mbps.<br>$0010_B$**LINK100** Blink when link is 100 Mbps.<br>$0100_B$**LINK1000** Blink when link is 1000 Mbps.<br>$1000_B$**LINK2500** Blink when link is 2500 Mbps. |
| PULSE | 11:8 | RW | **Pulsing Configuration**<br>The PULSE field is a mask field that combines certain events, such as TXACT\|RXACT, to generate a pulse on the LED when such an event is detected.<br>$0000_B$**NONE** No pulsing<br>$0001_B$**TXACT** Transmit activity<br>$0010_B$**RXACT** Receive activity<br>$0100_B$**COL** Collision<br>$1000_B$**NO_CON** Constant on behavior is switched off. |
| CON | 7:4 | RW | **Constant On Configuration**<br>The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not active<br>$0001_B$**LINK10** On when link is 10 Mbps.<br>$0010_B$**LINK100** On when link is 100 Mbps.<br>$0100_B$**LINK1000** On when link is 1000 Mbps.<br>$1000_B$**LINK2500** On when link is 2500 Mbps. |

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| BLINKF | 3:0 | RW | **Fast Blinking Configuration**<br>The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior.<br>$0000_B$**NONE** Not Active<br>$0001_B$**LINK10** Blink when link is 10 Mbps.<br>$0010_B$**LINK100** Blink when link is 100 Mbps.<br>$0100_B$**LINK1000** Blink when link is 1000 Mbps.<br>$1000_B$**LINK2500** Blink when link is 2500 Mbps. |

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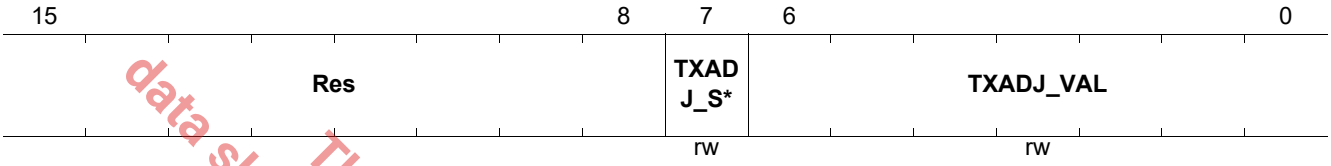
**PHY Transmit Amplitude Control Register (Register 30.8)**

This register adjusts the transmit amplitude of the PHY.

IEEE Standard Register=30.8

**VSPEC1_TXS_SCL_OFFSET** **Reset Value**

**PHY Transmit Amplitude Control Register (Register 30.8)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| TXADJ_SGN | 7 | RW | **Transmit Amplitude Adjustment Sign**<br>$0_B$ **INC** Increase transmit amplitude<br>$1_B$ **DEC** Decrease transmit amplitude |
| TXADJ_VAL | 6:0 | RW | **Transmit Amplitude Adjustment Value**<br>Multiply the transmit amplitude by the following factor.<br>(1 + (1-TXADJ_SGN*2)*TXADJ_VAL/128)<br>The amplitude adjustment takes effect on the next link up. |

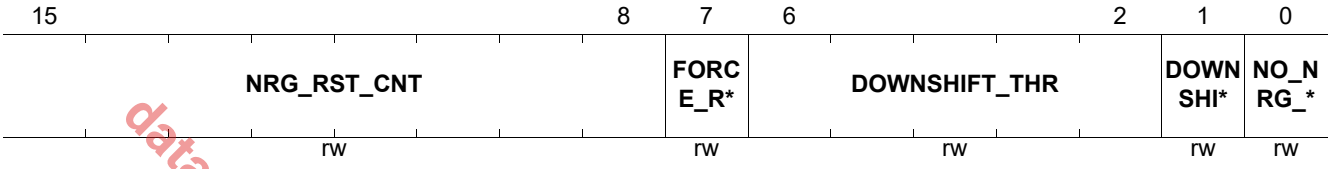
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The product (or products) mentioned in this

**NBASE-T Downshift Control Register (Register 30.10)**

IEEE Standard Register=30.10

**VSPEC1_NBT_DS_CTRL** **Reset Value**

**NBASE-T Downshift Control Register (Register 30.10)** **$0400_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| NRG_RST_CNT | 15:8 | RW | **Timer to Reset the Downshift Process**<br>When the energy is zero for a duration equal to NRG_RST_CNT seconds, the ANEG advertised capabilities are reset to the maximum GPHY capabilities. When NRG_RST_CNT is lower than 2, the ADS feature cannot be enabled.<br>Default is 4 seconds.<br>*Note: This timer only takes effect when NO_NRG_RST is set.* |
| FORCE_RST | 7 | RW | **Force Reset of Downwshift Process**<br>Setting this bit to 1 immediately resets the ANEG advertised capabilities to the maximum GPHY capabilities. |
| DOWNSHIFT_THR | 6:2 | RW | **NBASE-T Downshift Training Counter Threshold**<br>dsh_thr variable in NBASE-T specification<br>This is a 4-bit counter from 0 to 15 used to control the number of training cycles allowed for linkup, otherwise downshift. |
| DOWNSHIFT_EN | 1 | RW | **NBASE-T Downshift Enable**<br>dsh_en variable in NBASE-T specification<br>$0_B$ **DISABLE** Disables NBT downshift.<br>$1_B$ **ENABLE** Enables NBT downshift. |
| NO_NRG_RST | 0 | RW | **Advertise All Speeds if No Energy Detected**<br>When no energy is detected, this resets to advertise all speeds.<br>Energy variable in NBASE-T specification<br>$0_B$ **DISABLE** Do not reset speeds advertised when no energy is detected.<br>$1_B$ **ENABLE** Reset speeds advertised when no energy is detected. |

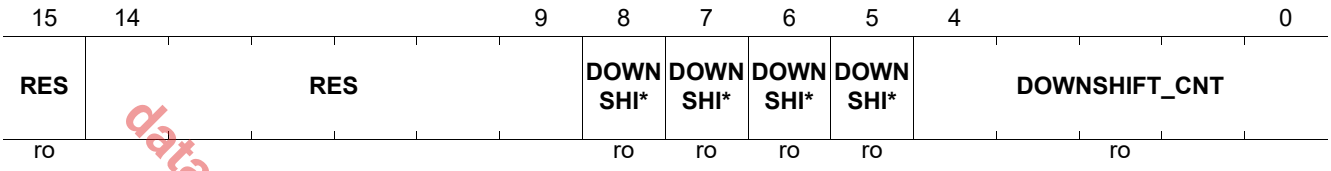
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The product (or products) mentioned in this

### NBASE-T Downshift Status Register (Register 30.11)

IEEE Standard Register=30.11

**VSPEC1_NBT_DS_STA** **Reset Value**

**NBASE-T Downshift Status Register (Register 30.11)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| DOWNSHIFT_1G | 8 | RO | **Downshift from 1G to Lower Speed** |
| DOWNSHIFT_2G5 | 7 | RO | **Downshift from 2.5 G to Lower Speed** |
| DOWNSHIFT_5G | 6 | RO | **Downshift 5G to Lower Speed**<br>Not supported by the GPHY |
| DOWNSHIFT_10G | 5 | RO | **Downshift 10G to Lower Speed**<br>Not supported by the GPHY |
| DOWNSHIFT_CNT | 4:0 | RO | **Training Attempt Counter**<br>Counts training attempts to select the operating speed.<br>dsh_cnt state variable in NBASE-T specification |

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**Packet Manager Control (Register 30.12)**

IEEE Standard Register=30.12

Control the Packet Manager Configuration

**VSPEC1_PM_CTRL** **Reset Value**

**Packet Manager Control (Register 30.12)** **$3000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES | RES | | | MDINT_M* | RES | RES | RES | RES | RES | | RES | RES | RES | SI | RES |
| rw | rw | | | rw | rw | rw | rw | rw | rw | | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| MDINT_MODE | 11 | RW | **MDIO Interrupt Mode**<br>Sets the mode of the MDIO interrupt signal.<br>$0_B$ **TRI** Tristate mode<br>The MDIO interrupt signal is tristate when the interrupt is inactive. It is driven only when the interrupt is active.<br>$1_B$ **PP** Push-pull mode<br>The MDIO interrupt signal is constantly driven. |
| SI | 1 | RW | **Super Isolate**<br>Use in Super Isolate mode. Forces the device into a power down state by pin strapping (SLEEP) in which power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode. See also IEEE 802.3-2008 22.2.4.1.5. The SI bit is only used to release the device from Super Isolate mode. Entering Super Isolate mode can only be activated by pin strapping at power up.<br>$0_B$ **NORMAL** Normal operational mode<br>$1_B$ **SUPER_ISOLATE** Super Isolate mode |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

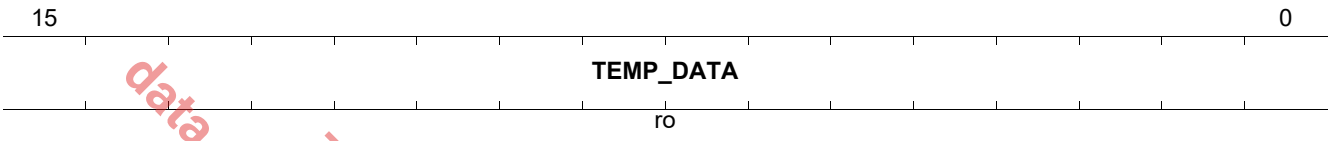
**Temperature Code (Register 30.14)**

Junction temperature is presented in degrees Celsius

IEEE Standard Register=30.14

**VSPEC1_TEMP_STA** **Reset Value**

**Temperature Code (Register 30.14)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| TEMP_DATA | 15:0 | RO | **Junction Temperature**<br>The temperature is represented as a two's complement binary fixed point number, of which the 7 LSBs are fractional. The STA must take the thermal mitigation measures when the junction temperature exceeds the normal operating range if ADS is disabled.<br>TEMP_DATA is invalid when the value is $0000_H$.<br>Example Tj Values (Decimal):<br>• For Tj = -40 degC, TEMP_DATA = $EC00_H$<br>• For Tj= +125 degC, TEMP_DATA = $3E80_H$ |

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The product(s) mentioned in this

### VSPEC1 Interrupt Mask Register (Register 30.17)

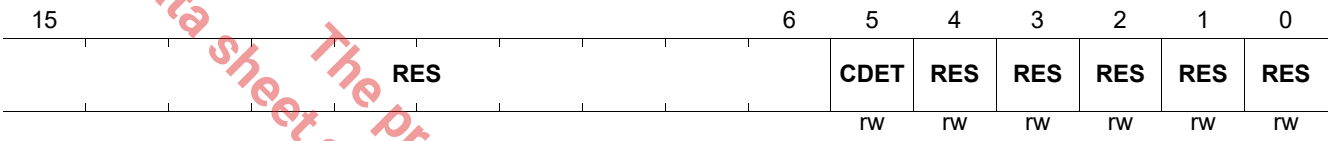
This register defines the mask for the Interrupt Status Register (ISTAT), which contains the event source for the MDINT interrupt sent from the GPHY to an external chip. The mask is cleared whenever the corresponding interrupt is serviced.

The information about the interrupt source is indicated in the VSPEC1_ISTAT register.

IEEE Standard Register=30.17

**VSPEC1_IMASK** **Reset Value**

**VSPEC1 Interrupt Mask Register (Register 30.17)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| CDET | 5 | RW | **Cable Detect Interrupt**<br>When active, MDINT is activated upon interrupt from detection of energy on the link.<br>$0_B$ **INACTIVE** Interrupt is masked out.<br>$1_B$ **ACTIVE** Interrupt is activated. |

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

### VSPEC1 Interrupt Status Register (Register 30.18)

This register defines the event source for the MDINT interrupt sent from the GPHY to an external chip based on the mask settings in the VSPEC1_IMASK register.

VSPEC1_ISTAT is a cleared on read by the STA.

IEEE Standard Register=30.18

**VSPEC1_ISTAT** **Reset Value**

**VSPEC1 Interrupt Status Register (Register 30.18)** **$0000_H$**

| 15 … 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| RES | CDET | RES | RES | RES | RES | RES |
| | rosc | rosc | rosc | rosc | rosc | rosc |

| Field | Bits | Type | Description |
|---|---|---|---|
| CDET | 5 | ROSC | **Cable Detect Interrupt**<br>When this bit is set, MDINT is activated upon interrupt from detection of energy on the link.<br>$0_B$ **INACTIVE** This event is not the interrupt source.<br>$1_B$ **ACTIVE** The cable detect interrupt is the source of the interrupt. |

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The product(s) mentioned in this

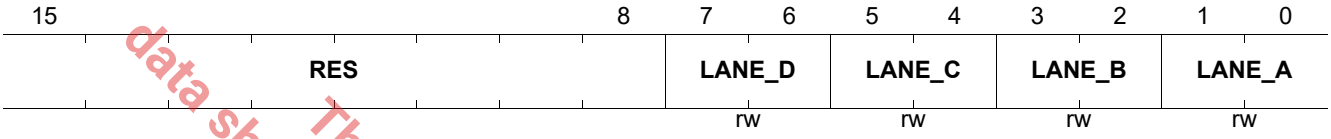
### ASP Mapping to Physical Lanes (Register 30.20)

This register offers a programmable option to map physical lanes A, B, C, and D of the TPI to the ASPs. Each ASP must be mapped to each lane.

IEEE Standard Register=30.20

**VSPEC1_LANE_ASP_MAP** **Reset Value**

**ASP Mapping to Physical Lanes (Register 30.20)** **$00E4_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| LANE_D | 7:6 | RW | **Map Physical Lane-D to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-D to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-D to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-D to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-D to the ASP-D |
| LANE_C | 5:4 | RW | **Map Physical Lane-C to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-C to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-C to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-C to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-C to the ASP-D |
| LANE_B | 3:2 | RW | **Map Physical Lane-B to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-B to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-B to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-B to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-B to the ASP-D |
| LANE_A | 1:0 | RW | **Map Physical Lane-A to the ASP**<br>$00_B$ **ASPA** Map Physical Lane-A to the ASP-A<br>$01_B$ **ASPB** Map Physical Lane-A to the ASP-B<br>$10_B$ **ASPC** Map Physical Lane-A to the ASP-C<br>$11_B$ **ASPD** Map Physical Lane-A to the ASP-D |

data sheet are Not Recommended for New Designs (NRND)
The product (s/products) mentioned in this

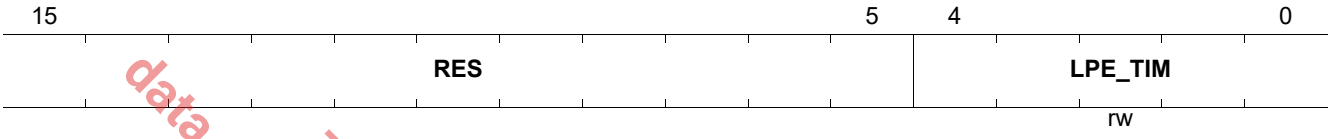
**Time to Enter Low Power (Register 30.21)**

Programmable option to delay the time taken to enter low power mode.

IEEE Standard Register=30.21

**VSPEC1_LOW_POWER_ENTRY_TIME** **Reset Value**

**Time to Enter Low Power (Register 30.21)** **$0001_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| LPE_TIM | 4:0 | RW | **Low Power Entry Time**<br>This is the time taken from detection of no activity on the line to the low power completion. The granularity is 4 seconds and adds 2.4 seconds to 5.6 seconds on to the initial time. |

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The product(s) mentioned in this

**Fast Retrain Control and Status (Register 30.22)**

This register supports fast retrain (FR) as follows:

1. Configures the FR capability (IEEE, CISCO(THPBYP,TXDIS,EXT) [4]).
2. Records the link partner FR capability.
3. Reports the FW resolution of the FR capability.
4. Defines the maximum allowed number of times to try FR before performing a full link down.

IEEE Standard Register=30.22

**VSPEC1_FRCTL** **Reset Value**

**Fast Retrain Control and Status (Register 30.22)** **$0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **MAX_FR_*** | **STAT_IE*** | **STAT_CI*** | **STAT_TH*** | **STAT_TX*** | **STAT_EXT** | **LP_IEEE** | **LP_CISCO** | **LP_THPB*** | **LP_TXDIS** | **LP_EXT** | **CAP_IEEE** | **CAP_CIS*** | **CAP_THP*** | **CAP_TXD*** | **CAP_EXT** |
| rw | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| MAX_FR_RETRY | 15 | RW | **Maximum Number of FR Retries Before Taking Linking Down**<br>$0_B$ **DISABLE** Maximum number of retries limited to 4.<br>$1_B$ **ENABLE** Maximum number of retries limited to 8. |
| STAT_IEEE | 14 | RO | **Resolved for IEEE FR**<br>$0_B$ **DISABLE** Resolved to no IEEE FR.<br>$1_B$ **ENABLE** Resolved to IEEE FR. |
| STAT_CISCO | 13 | RO | **Resolved for CISCO FR**<br>$0_B$ **DISABLE** Resolved to no CISCO FR<br>$1_B$ **ENABLE** Resolved to CISCO FR |
| STAT_THPBYP | 12 | RO | **Resolved Status THP BYP during COEF_EXCH for Either CISCO FR or IEEE FR**<br>$0_B$ **DISABLE** Resolved that THP is not BYP for either CISCO FR or IEEE FR<br>$1_B$ **ENABLE** Resolved that THP is BYP during COEF EXCH for either CISCO FR or IEEE FR |
| STAT_TXDIS | 11 | RO | **Resolved Status for CISCO FR with TX DISABLE**<br>$0_B$ **DISABLE** Resolved that CISCO FR is not followed by TX DISABLE after link fail signaling<br>$1_B$ **ENABLE** Resolved that CISCO FR is followed by TX DISABLE after link fail signaling |
| STAT_EXT | 10 | RO | **Resolved Status for CISCO Extended FR Timing**<br>$0_B$ **DISABLE** Resolved for no CISCO FR with extended timing<br>$1_B$ **ENABLE** Resolved for CISCO FR with extended timing |
| LP_IEEE | 9 | RO | **LP Request for IEEE FR**<br>$0_B$ **DISABLE** No advertise for IEEE FR<br>$1_B$ **ENABLE** Advertise capable of doing IEEE FR |

Data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

| Field | Bits | Type | Description (cont'd) |
|---|---|---|---|
| LP_CISCO | 8 | RO | **LP Request for CISCO FR**<br>$0_B$ **DISABLE** No advertise for CISCO FR<br>$1_B$ **ENABLE** Advertise capable of doing CISCO FR |
| LP_THPBYP | 7 | RO | **LP Request for THP BYP During COEF_EXCH for Either CISCO FR or IEEE FR**<br>$0_B$ **DISABLE** No request for THP BYP for either CISCO FR or IEEE FR<br>$1_B$ **ENABLE** Request for THP BYP during COEF EXCH for either CISCO FR or IEEE FR |
| LP_TXDIS | 6 | RO | **LP Request for CISCO FR with TX DISABLE**<br>$0_B$ **DISABLE** No request that CISCO FR is followed by TX DISABLE after link fail signaling<br>$1_B$ **ENABLE** Request that CISCO FR is followed by TX DISABLE after link fail signaling |
| LP_EXT | 5 | RO | **LP Request for CISCO Extended FR Timing**<br>$0_B$ **DISABLE** No request for CISCO FR with extended timing<br>$1_B$ **ENABLE** Request for CISCO FR with extended timing |
| CAP_IEEE | 4 | RW | **Request for IEEE FR**<br>$0_B$ **DISABLE** No advertise for IEEE FR<br>$1_B$ **ENABLE** Advertise capable of doing IEEE FR |
| CAP_CISCO | 3 | RW | **Capable of Advertising CISCO FR**<br>$0_B$ **DISABLE** No advertise for CISCO FR<br>$1_B$ **ENABLE** Advertise capable of doing CISCO FR |
| CAP_THPBYP | 2 | RW | **Request LP for THP BYP during COEF_EXCH for Both CISCO FR and IEEE FR**<br>$0_B$ **DISABLE** No request to LP for THP BYP for either CISCO FR or IEEE FR<br>$1_B$ **ENABLE** Request LP for THP BYP during COEF EXCH for either CISCO FR or IEEE FR |
| CAP_TXDIS | 1 | RW | **Request for CISCO FR with TX DISABLE**<br>$0_B$ **DISABLE** No request for CISCO FR with TX DISABLE after link fail signaling<br>$1_B$ **ENABLE** Advertise request that CISCO FR is followed by TX DISABLE after link fail signaling |
| CAP_EXT | 0 | RW | **Request for CISCO Extended FR Timing**<br>$0_B$ **DISABLE** No request for CISCO FR with extended timing<br>$1_B$ **ENABLE** Advertise request for CISCO FR with extended timing |

data sheet are Not Recommended for New Designs (NRND)
The product (or product(s) mentioned in this

## 6.5 Vendor Specific 2 Device Registers

This register file contains the GPHY-specific registers for MMD=31 (decimal).

**Table 35 Registers Overview- Vendor Specific 2 Device Registers**

| Register Short Name | Register Long Name | Reset Value |
|---|---|---|
| VPSPEC2_WOL_CTL | WoL Control Register (Register 31.3590) | $0000_H$ |
| VPSPEC2_WOL_AD01 | WoL Address Byte 0 and 1 (Register 31.3592) | $0000_H$ |
| VPSPEC2_WOL_AD23 | WoL Address Byte 2 and 3 (Register 31.3593) | $0000_H$ |
| VPSPEC2_WOL_AD45 | WoL Address Byte 4 and 5 (Register 31.3594) | $0000_H$ |
| VPSPEC2_WOL_PW01 | WoL SecureON Password Byte 0 (Register 31.3595) | $0000_H$ |
| VPSPEC2_WOL_PW23 | WoL SecureON Password Byte 2 and 3 (Register 31.3596) | $0000_H$ |
| VPSPEC2_WOL_PW45 | WoL SecureON Password Byte 4 and 5 (Register 31.3597) | $0000_H$ |

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### 6.5.1 VSPEC2 Register Descriptions

This section describes all the VSPEC2 registers in detail.

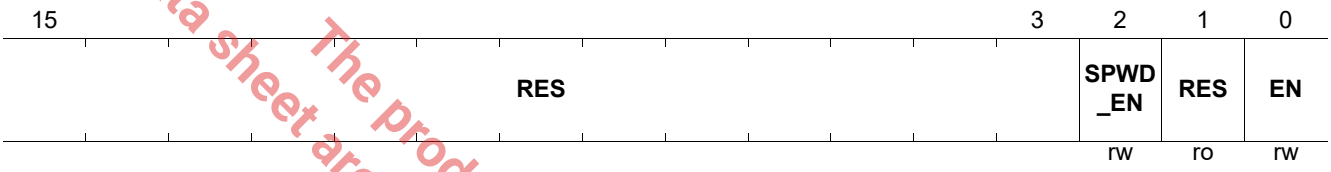
**Wake-on-LAN Control Register (Register 31.3590)**

This is the Wake-on-LAN control register. Redirected to PCS_PDI_WOL_CTL.

IEEE Standard Register=31.3590

**VPSPEC2_WOL_CTL** **Reset Value**

**Wake-on-LAN Control Register (Register 31.3590)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| SPWD_EN | 2 | RW | **Secure-ON Password Enable**<br>When this bit is set to enabled, the SecureON password is checked after 16 MAC address repetitions.<br>$0_B$ **DISABLED** Disables the SecureON password check<br>$1_B$ **ENABLED** Enables the SecureON password check |
| RES | 1 | RO | **Reserved**<br>Must always be written to 0. |
| EN | 0 | RW | **Enables the Wake-on-LAN Functionality**<br>When WoL is enabled, the PHY scans for the configured magic packet and indicates its reception via the register bit ISTAT. WoL and optionally also via interrupt.<br>$0_B$ **DISABLED** Disables the WoL functionality<br>$1_B$ **ENABLED** Enables the WoL functionality |

Data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

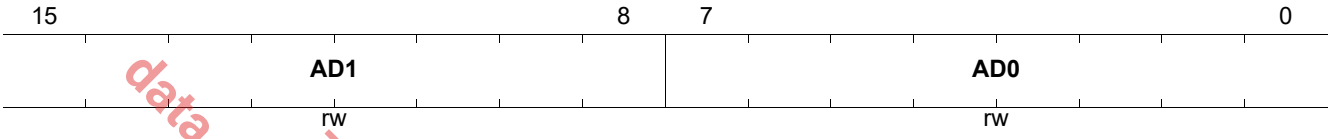
**Wake-on-LAN Address Byte 0 and 1 (Register 31.3592)**

Wake-on-LAN Address Byte 0 and 1. Redirected to PCS_PDI_WOL_AD01.

IEEE Standard Register=31.3592

**VPSPEC2_WOL_AD01** **Reset Value**

**Wake-on-LAN Address Byte 0 and 1 (Register 31.3592)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| AD1 | 15:8 | RW | **Address Byte 1**<br>Defines byte 1 of the WoL-designated MAC address to which the PHY is sensitive. |
| AD0 | 7:0 | RW | **Address Byte 0**<br>Defines byte 0 of the WoL-designated MAC address to which the PHY is sensitive. |

The product(s) mentioned in this data sheet are Not Recommended for New Designs (NRND)

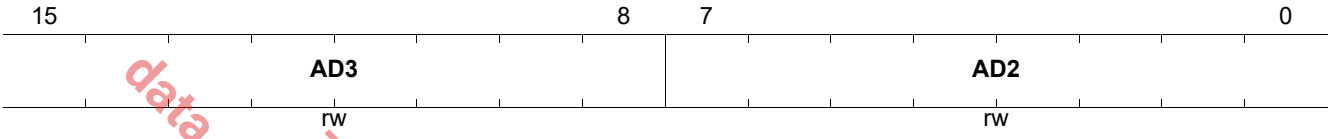
**Wake-on-LAN Address Byte 2 and 3 (Register 31.3593)**

Wake-on-LAN Address Byte 2 and 3. Redirected to PCS_PDI_WOL_AD23.

IEEE Standard Register=31.3593

**VPSPEC2_WOL_AD23** **Reset Value**

**Wake-on-LAN Address Byte 2 and 3 (Register 31.3593)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| AD3 | 15:8 | RW | **Address Byte 3**<br>Defines byte 3 of the WoL-designated MAC address to which the PHY is sensitive. |
| AD2 | 7:0 | RW | **Address Byte 2**<br>Defines byte 2 of the WoL-designated MAC address to which the PHY is sensitive. |

The product(s) mentioned in this data sheet are Not Recommended for New Designs (NRND)

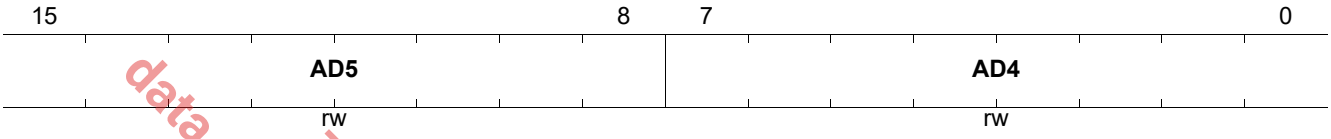
**Wake-on-LAN Address Byte 4 and 5 (Register 31.3594)**

Wake-on-LAN Address Byte 4 and 5. Redirected to PCS_PDI_WOL_AD45.

IEEE Standard Register=31.3594

**VPSPEC2_WOL_AD45** **Reset Value**

**Wake-on-LAN Address Byte 4 and 5 (Register 31.3594)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| AD5 | 15:8 | RW | **Address Byte 5**<br>Defines byte 5 of the WoL-designated MAC address to which the PHY is sensitive. |
| AD4 | 7:0 | RW | **Address Byte 4**<br>Defines byte 4 of the WoL-designated MAC address to which the PHY is sensitive. |

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

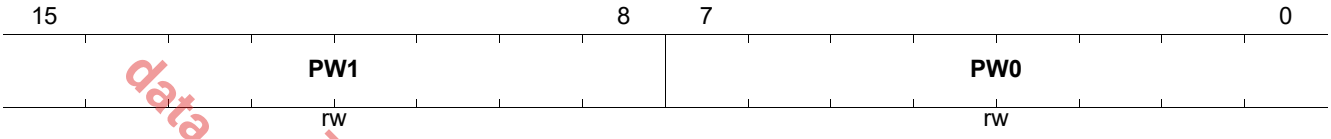
**Wake-on-LAN SecureON Password Byte 0 (Register 31.3595)**

Wake-on-LAN SecureON Password Byte 0. Redirected to PCS_PDI_WOL_PWD01.

IEEE Standard Register=31.3595

**VPSPEC2_WOL_PW01** **Reset Value**

**Wake-on-LAN SecureON Password Byte 0 (Register 31.3595)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| PW1 | 15:8 | RW | **SecureON Password Byte 1**<br>Defines byte 1 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW0 | 7:0 | RW | **SecureON Password Byte 0**<br>Defines byte 0 of the WoL-designated SecureON password to which the PHY is sensitive. |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

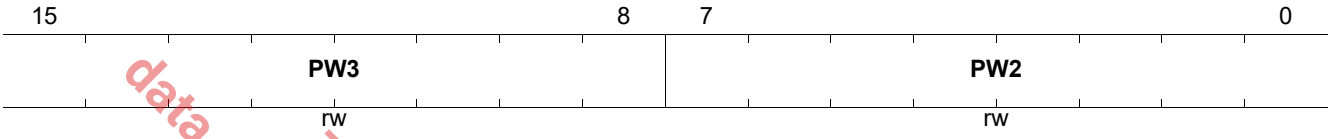
**Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)**

Wake-on-LAN SecureON Password Byte 2 and 3. Redirected to PCS_PDI_WOL_PWD23.

IEEE Standard Register=31.3596

**VPSPEC2_WOL_PW23** **Reset Value**

**Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| PW3 | 15:8 | RW | **SecureON Password Byte 3**<br>Defines byte 3 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW2 | 7:0 | RW | **SecureON Password Byte 2**<br>Defines byte 2 of the WoL-designated SecureON password to which the PHY is sensitive. |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

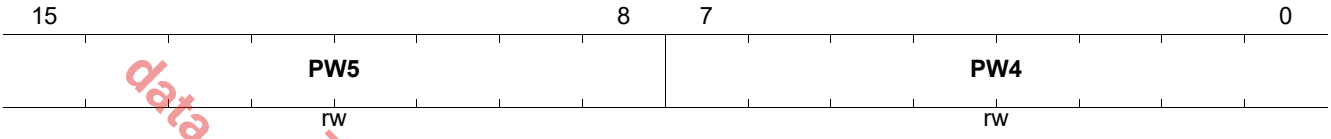
**Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)**

Wake-on-LAN SecureON Password Byte 4 and 5. Redirected to PCS_PDI_WOL_PWD45.

IEEE Standard Register=31.3597

**VPSPEC2_WOL_PW45** **Reset Value**

**Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)** **$0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| PW5 | 15:8 | RW | **SecureON Password Byte 5**<br>Defines byte 5 of the WoL-designated SecureON password to which the PHY is sensitive. |
| PW4 | 7:0 | RW | **SecureON Password Byte 4**<br>Defines byte 4 of the WoL-designated SecureON password to which the PHY is sensitive. |

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The product (or products) mentioned in this

# 7 Electrical Characteristics

This chapter provides the electrical characteristics for the MxL86280C.

## 7.1 Absolute Maximum Ratings

Table 36 shows the absolute maximum ratings for the MxL86280C.

**Table 36 Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Storage Temperature Limits | $T_{STG}$ | -55.0 | – | 125.0 | °C | – |
| Soldering Temperature | $T_{SOL}$ | – | – | 260.0 | °C | Compliance with lead free re-flow soldering profile as J-STD-020D |
| Moisture Level 3 Temperature Limits | $T_{ML3}$ | – | – | 260.0 | °C | According to IPS J-STD 020 |
| Absolute Junction Temperature | $T_{JABS}$ | -40.0 | | 125 | °C | The thermal solution must ensure that $T_J$ never exceeds $T_{JABS}$ maximum. The chip resets the device when $T_J$ > $T_{JABS}$ maximum to prevent any damage to occur. |
| DC Voltage Limits on VDD3V3PAD1, VDD3V3PAD2 Pins | $V_{DDP3V3}$ | -0.5 | – | +3.63 | V | Generic ball $V_{HIGH}$ supply |
| DC Voltage Limits on VDDP_PAD Pins when Ball K4 Pin Strap PS_MDIO_VOLTAGE is HIGH | $V_{DDP}$ | -0.5 | – | +3.63 | V | Multi voltage ball $V_{HIGH}$ supply |
| DC Voltage Limits on VDDP_PAD Pins when Ball K4 Pin Strap PS_MDIO_VOLTAGE is LOW | $V_{DDP}$ | -0.5 | – | +1.98 | V | Multi voltage ball supply. 1.8 V supply dedicated to MDIO pins in lower mode |
| DC Voltage Limits on VDDA3V3_0, VDDA3V3_1, VDDA3V3_2, VDDA3V3_3, VDDA3V3_4, VDDA3V3_5, VDDA3V3_6, and VDDA3V3_7 Pins | $V_{DDA3V3}$ | -0.5 | – | +3.63 | V | Chip analog $V_{HIGH}$ supply |
| DC Voltage Limits on VDDA1V8_0, VDDA1V8_1 Pins | $V_{DDA1V8}$ | -0.5 | – | +1.98 | V | Chip analog supply |

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The product (or products) mentioned in this

**Table 36 Absolute Maximum Ratings** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DC Voltage Limits on VDDA1V8PORXO, VDDA1V8_PVT, VCC1V8_OTP, and VDDA1V8_CML Pins | $V_{DDA1V8PORXO}$ $V_{DDA1V8PVT}$ $V_{CC1V8OTP}$ $V_{DDA1V8CML}$ | -0.5 | – | +1.98 | V | Chip clocking supply |
| DC Voltage Limits on VPHA1V8_0, VPHA1V8_1, and VDDA1V8_PLL Pins | $V_{PH}$ $V_{DDA1V8PLL}$ | -0.5 | – | +1.98 | V | LJ PLL $V_{HIGH}$ supply |
| DC Voltage Limits on VDDA1V2CDB0, VDDA1V2CDB1 Pins | $V_{DDA1V2CDB}$ | -0.5 | – | +1.32 | V | Chip analog supply |
| DC Voltage Limits on VDDA0V8_0, VDDA0V8_1, VDDD0V8REF, VDDD0V8POST, and VDDA0V8_CML Pins | $V_{DDA0V8}$ $V_{DDD0V8PLL}$ $V_{DDA0V8CML}$ | -0.5 | – | +0.88 | V | Chip analog $V_{LOW}$ supply, LJ PLL $V_{LOW}$ supply |
| DC Voltage Limits on VDDD0V8_COR Pins | $V_{DD}$ | -0.5 | – | +0.88 | V | Chip core supply |
| DC Voltage Limits on VA0V8_0, VA0V8_1 Pins | $V_P$ | -0.5 | – | +0.88 | V | $V_{LOW}$ supply |
| DC Voltage Limits on Any Other Pins[1] with Respect to Ground | $V_{DC}$ | -0.5 | – | $V_{DDP3V3}$+ 0.5 | V | Unless specified otherwise |
| XTAL1 Input Voltage | $V_{XTAL1}$ | -0.30 | – | 2.0 | V | – |
| ESD HBM Robustness | $V_{ESD,HBM}$ | – | – | 1000.0 | V | According to ANSI/ESDA/JEDEC JS-001-2014 |
| ESD CDM Robustness | $V_{ESD,CDM}$ | – | – | 250.0 | V | According to ANSI/ESDA/JEDEC JS-002-2014 |

1) Any pin that is not a supply pin out of one of the domains: $V_{DDP}$, $V_{PH}$, $V_P$, $V_{DDA3V3}$, $V_{DDA1V8PORXO}$, $V_{DDA1V2CDB}$, $V_{DDA0V8}$, $V_{DD}$, and $V_{DDA1V8}$.

***Attention: Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.***

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The product (or products) mentioned in this

## 7.2 Operating Range

Table 37 defines the limit values of voltages and temperature which may be applied to guarantee proper operation of the MxL86280C.

**Table 37 Operating Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Ambient Temperature under Bias | $T_A$ | 0 | – | 70 | °C | The thermal design must ensure that the maximum junction temperature is not exceeded. The use of a heat sink may be suitable. |
| Junction Temperature | $T_j$ | – | – | 110.0 | °C | Thermal solution must ensure that $T_j$ remains within operating range and never exceeds maximum absolute ratings ($T_{JABS}$). |
| Generic Pin Supply Voltage | $V_{DDP3V3}$ | 3.14 | 3.30 | 3.46 | V | Generic pin $V_{HIGH}$ supply |
| Multi Voltage Pin Supply Voltage for MDIO Signals when Ball K4 Pin Strap PS_MDIO_VOLTAGE is HIGH | $V_{DDP}$ | 3.14 | 3.30 | 3.46 | V | Multi voltage pin $V_{HIGH}$ supply |
| Multi Voltage Pin Supply Voltage for MDIO Signals when Ball K4 Pin Strap PS_MDIO_VOLTAGE is LOW | $V_{DDP}$ | 1.71 | 1.80 | 1.89 | V | Multi voltage pin supply. 1.8 V supply dedicated to MDIO pins in lower mode |
| Analog High Supply Voltage | $V_{DDA3V3}$ | 3.14 | 3.30 | 3.46 | V | Chip analog $V_{HIGH}$ supply |
| XO Supply Voltage | $V_{DDA1V8PORXO}$ | 1.71 | 1.80 | 1.89 | V | Chip clocking $V_{HIGH}$ supply |
| Analog Medium Supply Voltage | $V_{DDA1V8}$ | 1.71 | 1.80 | 1.89 | V | Chip analog $V_{MED}$ supply |
| CDB Supply Voltage | $V_{DDA1V2CDB}$ | 1.14 | 1.20 | 1.26 | V | Chip analog supply |
| High Supply Voltage | $V_{PH}$ | 1.71 | 1.80 | 1.89 | V | $V_{HIGH}$ supply |
| LJ PLL High Supply Voltage | $V_{DDA1V8PLL}$ | 1.71 | 1.80 | 1.89 | V | LJ PLL $V_{HIGH}$ supply |
| Analog Low Supply Voltage | $V_{DDA0V8}$ | 0.76 | 0.8 | 0.84 | V | Chip analog $V_{LOW}$ supply |
| LJ PLL Low Supply Voltage | $V_{DDD0V8PLL}$ | 0.76 | 0.8 | 0.84 | V | LJ PLL $V_{LOW}$ supply |
| Chip Core Supply Voltage | $V_{DD}$ | 0.76 | 0.8 | 0.84 | V | Chip core supply |
| Low Supply Voltage | $V_P$ | 0.76 | 0.8 | 0.84 | V | $V_{LOW}$ supply |
| Ground | $V_{SS}$ | 0.00 | 0.00 | 0.00 | V | – |

***Attention: Operations above the maximum values listed here for extended periods may adversely affect long-term reliability of the device.***

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

## 7.3 Typical Power Consumption

Table 38 lists the typical power consumption for different modes. Typical power is the power consumed by a nominal process device, nominal supply voltages, at 25°C ambient temperature and a CAT5e link segment.

The conditions for Link-up are full speed and bidirectional, full duplex traffic on all 8 ports. The switch operates at 20 Gbps wirespeed with 8 ports.

**Table 38 Typical Power Consumption**

| Conditions: 25°C | 3.3 V $V_{HIGH}$ Domain Current | 1.8 V Domain Current | 1.2 V Domain Current | 0.8 V $V_{LOW}$ Domain Current | Chip Power |
|---|---|---|---|---|---|
| **Unit** | **mA** | **mA** | **mA** | **mA** | **W** |
| 2500BASE-T Link-up, 100 m Cable | 383 | 60 | 473 | 3699 | 4.9 |
| 2500BASE-T Link-up, 30 m Cable | 351 | 70 | 448 | 3189 | 4.4 |
| 2500BASE-T EEE | 294 | 48 | 134 | 1531 | 2.4 |
| 1000BASE-T Link-up, 100 m Cable | 301 | 60 | 435 | 1688 | 3 |
| 1000BASE-T EEE | 30 | 49 | 118 | 813 | 1 |
| 100BASE-TX Link-up, 100 m Cable | 103 | 48 | 113 | 873 | 1.3 |
| 100BASE-TX EEE | 25 | 46 | 119 | 588 | 0.8 |
| 10BASE-Te Link-up, 100 m Cable | 93 | 47 | 66 | 800 | 1.1 |
| Cable Unplugged - ANEG | 51 | 46 | 65 | 581 | 0.8 |
| Cable Unplugged - Low Power | 32 | 41 | 3 | 265 | 0.4 |
| Reset | 2 | 25 | 0 | 60 | 0.1 |

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The product(or products) mentioned in this

## 7.4 Maximum Thermal Design Power

Table 39 lists the maximum Thermal Design Power (TDP). The TDP is the power consumption for a full traffic load and worst-case process, supply voltage, cable, and temperature conditions. This value is relevant to design the thermal solution.

**Table 39 Maximum Power Consumption**

| Condition | Maximum Power (W) |
|---|---|
| Maximum Chip Power at Maximum Operating Range | 7.1 |

*Note: With a properly designed thermal solution (heat sink), it is unlikely that Tj exceeds the maximum operating junction temperature. An excess is reported in the MDIO register VSPEC1_TEMP_STA and the STA can initiate a renegotiation to a lower link rate to get Tj back into the operating temperature range if ADS is disabled.*

## 7.5 Maximum Current

Table 40 provides the maximum current to dimension the power supply. It is the maximum current consumption per rail for a full traffic load and worst-case process, supply voltage and temperature conditions that may occur in any operating state of the device. The maximum current can be higher than the steady state current, for instance in training phases of the internal filters.

**Table 40 Maximum Current Per Rail**

| 3.3 V Domain Current | 1.8 V Domain Current | 1.2 V Domain Current | 0.8 V Domain Current |
|---|---|---|---|
| **mA** | **mA** | **mA** | **mA** |
| 476 | 73 | 590 | 6341 |

The product (or products) mentioned in this data sheet are Not Recommended for New Designs (NRND)

## 7.6 DC Characteristics

These sections document the DC characteristics of the MxL86280C external interfaces.

### 7.6.1 Digital Interfaces

This section defines the DC characteristics of the GPIO interface as follows:

- General Purpose IO
- MDIO
- QSPI
- UART
- Interrupts
- Clock Input and Outputs
- LED
- JTAG
- HRSTN

Table 41 summarizes the DC characteristics for $V_{DDP}$ = 3.3 V.

**Table 41 DC Characteristics of the GPIO Interfaces (VDDP = 3.3 V)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input High Voltage | $V_{IH}$ | 0.7*$V_{DDP}$ | – | $V_{DDP}$+0.3 | V | – |
| Input Low Voltage | $V_{IL}$ | –0.3 | – | 0.3*$V_{DDP}$ | V | – |
| Output High Voltage | $V_{OH}$ | $V_{DDP}$-0.4 | – | – | V | $I_{OH}$ = 2, 4, 8, 12 mA |
| Output Low Voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 2, 4, 8, 12 mA |

Table 42 summarizes the DC characteristics for $V_{DDP}$ = 1.8 V.

**Table 42 DC Characteristics of the GPIO Interfaces (VDDP = 1.8 V[1])**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input High Voltage | $V_{IH}$ | 0.65*$V_{DDP}$ | – | $V_{DDP}$+0.3 | V | – |
| Input Low Voltage | $V_{IL}$ | –0.3 | – | 0.35*$V_{DDP}$ | V | – |
| Output High Voltage | $V_{OH}$ | $V_{DDP}$-0.4 | – | – | V | $I_{OH}$ = 2, 4, 8, 12 mA |
| Output Low Voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 2, 4, 8, 12 mA |

1) 1.8V is only applicable to the pins specified in PS_MDIO_VOLTAGE of Table 15.

### 7.6.2 Twisted Pair Interface

The TPI conforms to the specifications of 10BASE-Te (Clause 14), 100BASE-TX (Clause 25), 1000BASE-T (Clause 40), and 2.5GBASE-T (Clause 126) given in IEEE802.3, and ANSI X3.263-1995.

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The product (or products) mentioned in this

### 7.6.3 Built-in Temperature Sensor

Table 43 provides the parameters of the integrated temperature sensor.

**Table 43 Temperature Sensor Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Temperature Range | $T_{range}$ | -40 | | 125 | °C | The thermal mitigation measures must ensure that $T_j$ remains within the operating range. When $T_j$ exceeds the maximum ratings, the device performs a self-reset to prevent damage. |
| Resolution | | – | 12 | – | bits | – |
| Accuracy | | -3 | – | +3 | °C | Without calibration |

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The product (or products) mentioned in this

## 7.7 AC Characteristics

The AC characteristics of the external interfaces are specified under these operating conditions:

$T_A$ = 0 to 70°C

$V_{DDP}$ = 3.3 V ± 5%

$V_{SS}$ = 0 V

The timing measurements are made at minimum $V_{IH}$ for a logical 1 and at maximum $V_{IL}$ for a logical 0. See **Table 41** and **Table 42** for more details.

**Figure 24** shows the AC testing input/output waveforms. The load capacitors are according to the specific interface standard. All non-specified interfaces use 30 pF as assumed loading.

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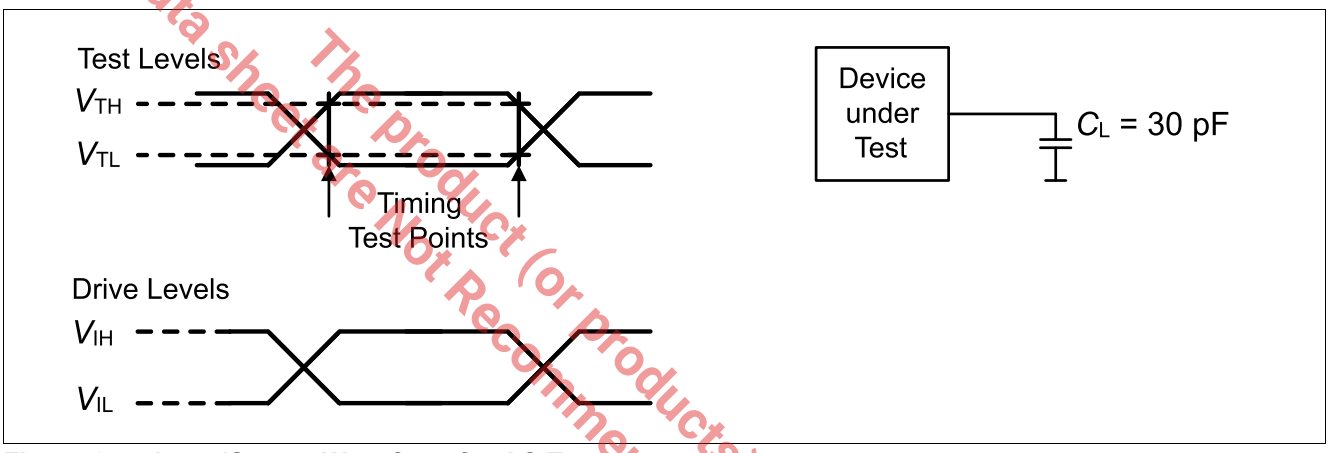



**Figure 24 Input/Output Waveform for AC Tests**

### 7.7.1 Power Up Sequence

All $V_{HIGH}$, $V_{PH}$, $V_{DDA}$, and $V_{LOW}$ are supplied externally.

In this section, for the sake of simplicity:

- All 3.3 V supplies are represented as $V_{HIGH}$.
- All 1.8 V supplies are represented as $V_{PH}$.
- All 1.2 V supplies are represented as $V_{DDA}$.
- All 0.8 V supplies are represented as $V_{LOW}$.

All the supply domains $V_{HIGH}$, $V_{PH}$, $V_{DDA}$, and $V_{LOW}$, and the input reference clock must be stabilized before releasing the reset HRSTN.

There is no known voltage rail power up sequence except that $V_{HIGH}$ must be ramped up and stable before $V_{PH}$ is ramped up, and $V_{LOW}$ must be ramped up and stable before $V_{PH}$ is ramped up. MaxLinear recommends implementing the power-up sequence defined in the reference board. Refer to the relevant hardware documentation available at **https://maxlinear.com/myMxL** for more information on the power circuitry.

The MxL86280C supports an asynchronous hardware reset HRSTN. **Table 44** lists the timing requirements of the power supply pins. The timings refer to the signal sequence waveforms depicted in **Figure 25**.

When PS_MDIO_VOLTAGE is low, $V_{DDP}$ is treated as $V_{PH}$.

When PS_MDIO_VOLTAGE is high, $V_{DDP}$ is treated as $V_{HIGH}$.

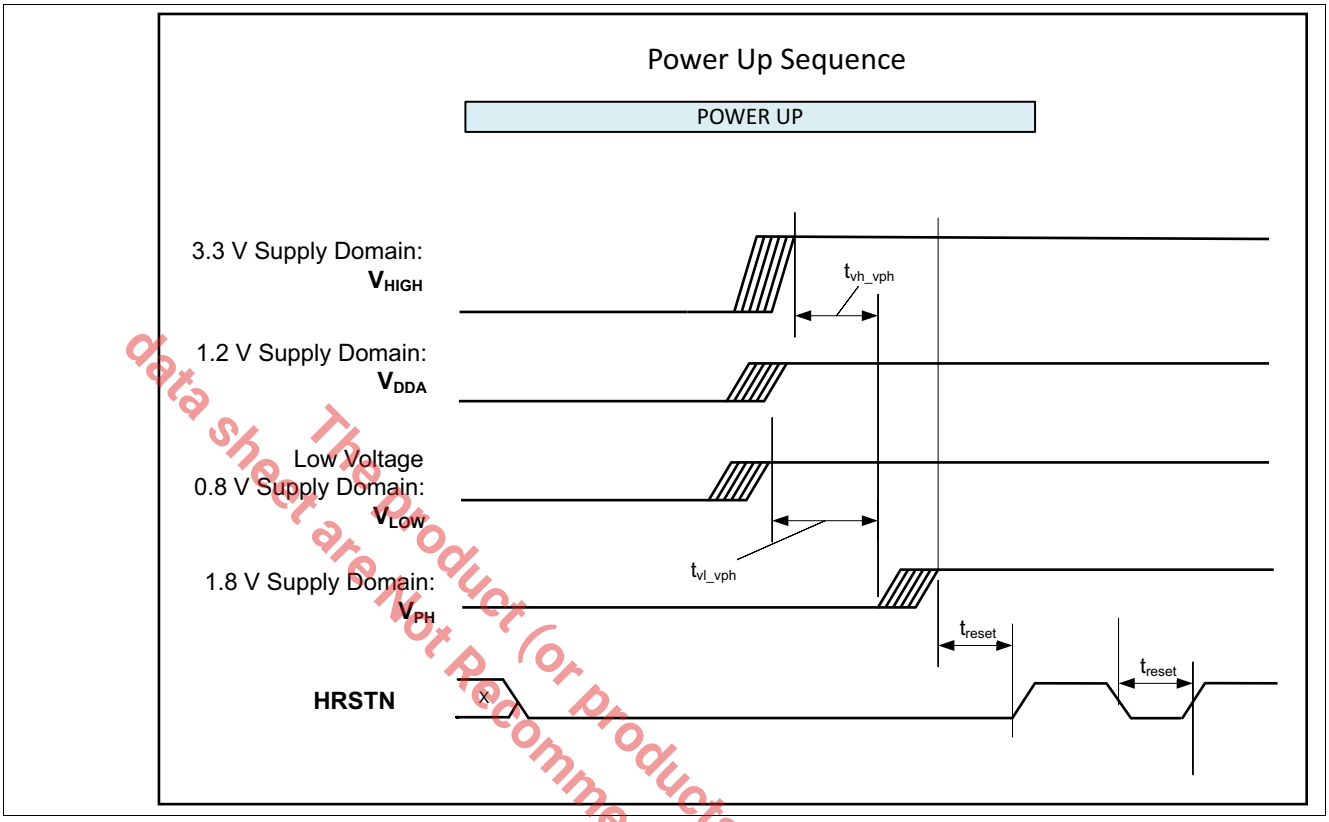



**Figure 25 Timing Diagram for the Reset Sequence**

**Table 44 Power Supply Timings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Delay between $V_{HIGH}$ and $V_{PH}$ Domains Voltage Ramp Up | $t_{vh_vph}$ | 50 | - | - | µs | The $V_{PH}$ voltage must never be higher than $V_{HIGH}$ voltage |
| Delay between $V_{LOW}$ and $V_{PH}$ Domains Voltage Ramp Up | $t_{vl_vph}$ | 50 | - | - | µs | The $V_{PH}$ voltage must never power up before $V_{LOW}$ voltage. |
| Reset Time after all Voltage Domains are Stabilized | $t_{reset}$ | 100 | – | – | ns | HRSTN must be released after the power supplies stabilized. |

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### 7.7.2 Input Clock

Table 45 lists the input clock requirements when not using a crystal, for example when an external reference clock is injected into the XTAL1 pin of the MxL86280C, such as nominal frequency, frequency deviation, duty cycle, and signal characteristics. When a crystal is applied to generate the reference clock using the integrated XO, the clock requirements stated here are explicitly met as long as the specification for the crystal is satisfied.

**Table 45 AC Characteristics of Input Clock on XTAL1 Pin**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Frequency with 25 MHz Input | $f_{clk25}$ | – | 25.0 | – | MHz | – |
| Frequency with 50 MHz Input | $f_{clk50}$ | – | 50.0 | – | MHz | – |
| Frequency Deviation[1)] | | -50.0 | – | +50.0 | ppm | – |
| Duty Cycle | | 40.0 | 50.0 | 60.0 | % | – |
| Rise/Fall Times with 25 MHz Input | | – | – | 10.0 | ns | 25 MHz |
| Rise/Fall Times with 50 MHz Input | | – | – | 5.0 | ns | 50 MHz |
| Input Long Term Jitter (Jrms) | | – | – | 2.0 | ps | 1 kHz to 10 MHz |
| Input Voltage Swing | | 300.0 | – | – | mV | Peak to Peak value |
| Input Voltage | | 0 | – | 1.8 | V | – |

1) Including the frequency stability tolerance due to temperature, and aging effects over the product lifetime.

### 7.7.3 Power Supply Rail Requirements

Table 46 lists the required characteristics of the power supplies. The definitions of the power supply rails are the same as that described in Section 7.7.1.

**Table 46 AC Characteristics of the Power Supply**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power Supply Ripple on $V_P$ | $R_{VP}$ | – | – | 40.0 | mV | Peak to Peak value |
| Power Supply Ripple on $V_{LOW}$ | $R_{VLOW}$ | – | – | 40.0 | mV | Peak to Peak value |
| Power Supply Ripple on $V_{DDA}$ | $R_{VDDA}$ | – | – | 50.0 | mV | Peak to Peak value |
| Power Supply Ripple on $V_{HIGH}$ | $R_{VHIGH}$ | – | – | 50.0 | mV | Peak to Peak value |
| Power Supply Ripple on $V_{PH}$ | $R_{VPH}$ | – | – | 50.0 | mV | Peak to Peak value |

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### 7.7.4 MDIO Slave Interface

**Figure 26** shows a timing diagram of the MDIO slave interface for a clock cycle in the read, write, and turnaround mode, respectively. The timing measures are annotated. **Table 47** summarizes the defined absolute values.

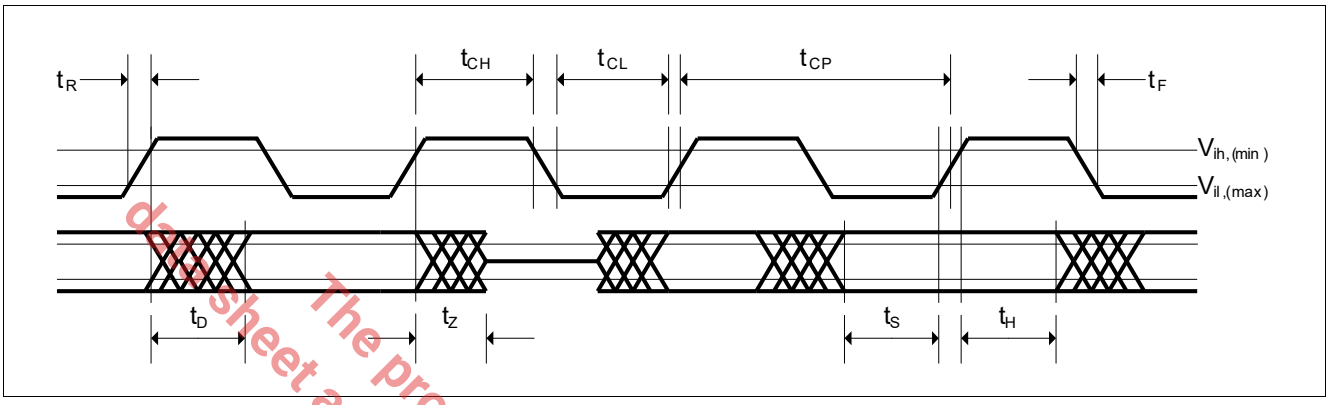



**Figure 26 Timing Diagram for the MDIO Slave Interface**

**Table 47 Timing Characteristics of the MDIO Slave Interface**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| MDC High Time | $t_{CH}$ | 10.0 | – | – | ns | The MDC signal must conform to the specified MDC timings when measured at the MxL86280C's MDC_S pin. |
| MDC Low Time | $t_{CL}$ | 10.0 | – | – | ns | |
| MDC Clock Period | $t_{CP}$ | 40.0 | 400.0 | – | ns | |
| MDC Clock Frequency[1)] | $t_{CP}$ | – | 2.5 | 25.0 | MHz | |
| MDC Rise Time | $t_R$ | – | – | 5.0 | ns | |
| MDC Fall Time | $t_F$ | – | – | 5.0 | ns | |
| MDIO Input Setup Time Subject to ↑ MDC | $t_S$ | 10.0 | – | – | ns | MxL86280C Receive |
| MDIO Input Hold Time Subject to ↑ MDC | $t_H$ | 10.0 | – | – | ns | MxL86280C Receive |
| MDIO Output Delay Time Subject to ↑ MDC | $t_D$ | 0.0 | – | 10 | ns | MxL86280C Transmit |
| Standard at 2.5 MHz | | | | | | |
| MDIO Output Delay Subject to ↑ MDC | $t_D$ | 0.0 | – | 300.0 | ns | PHY Transmit |

1) The MDC clock supports a range of frequencies up to 25 MHz. The default/typical frequency is 2.5 MHz.

data sheet are Not Recommended for New Designs (NRND)
The product(s) mentioned in this

### 7.7.5 Quad Serial Peripheral Interface (QSPI)

**Figure 27** shows the QSPI master timing.

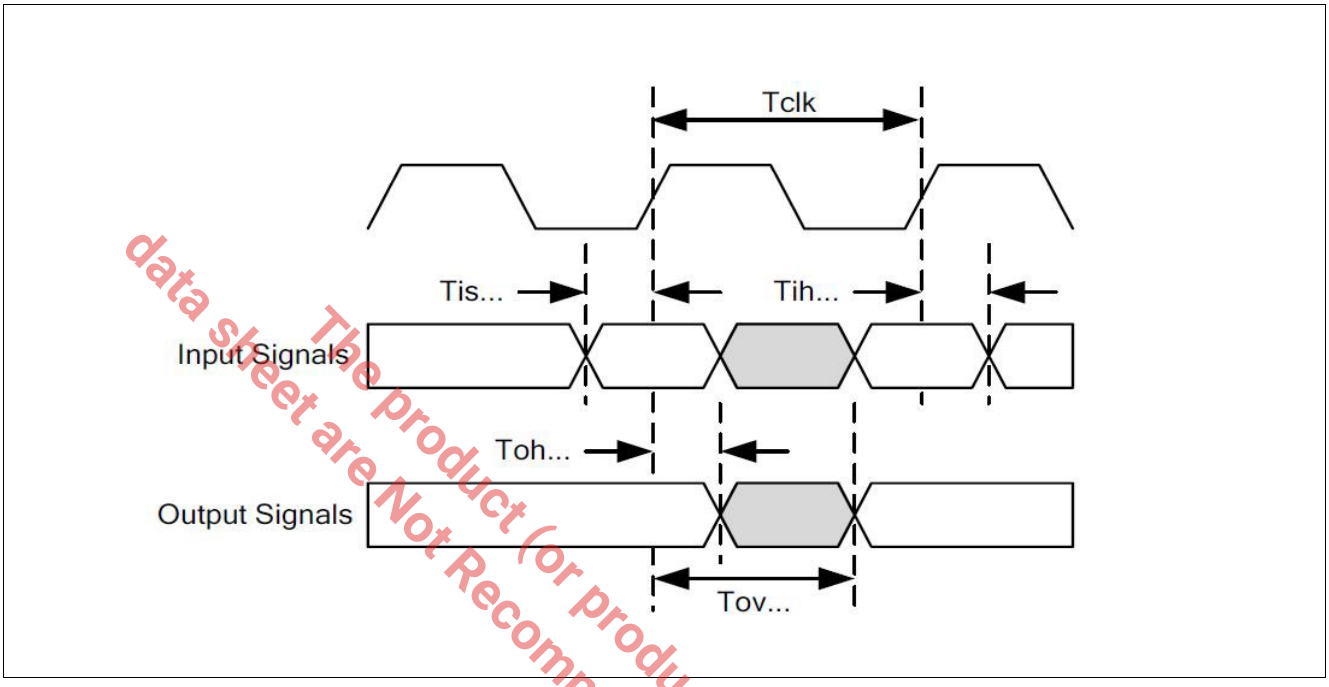



**Figure 27 QSPI Master Interface Timing**

**Table 48 QSPI Interface Timing Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Master Mode** | | | | | | |
| TX Data Output Hold | *Toh* | 5% | – | – | Tclk | For Tclk = 20 ns |
| Tx Data Output Delay | *Tov* | 0 | – | 50% | Tclk | For Tclk = 20 ns |
| Rx Data Input Setup time | *Tis* | 35% | – | – | Tclk | For Tclk = 20 ns |
| Rx Data Hold Time | *Tih* | 5% | – | – | Tclk | For Tclk = 20 ns |
| SPI Clock Period (Master Mode) | *Tclk* | 9.846 | – | – | ns | Maximum 101.5625 MHz |
| SPI Clock Rising | $S_7$ | 0.1 | – | – | V/ns | – |
| SPI Clock Falling | $S_6$ | 0.1 | – | – | V/ns | – |

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### 7.7.6 JTAG Interface

The JTAG test interface is used for debugging the CPU and boundary scan.

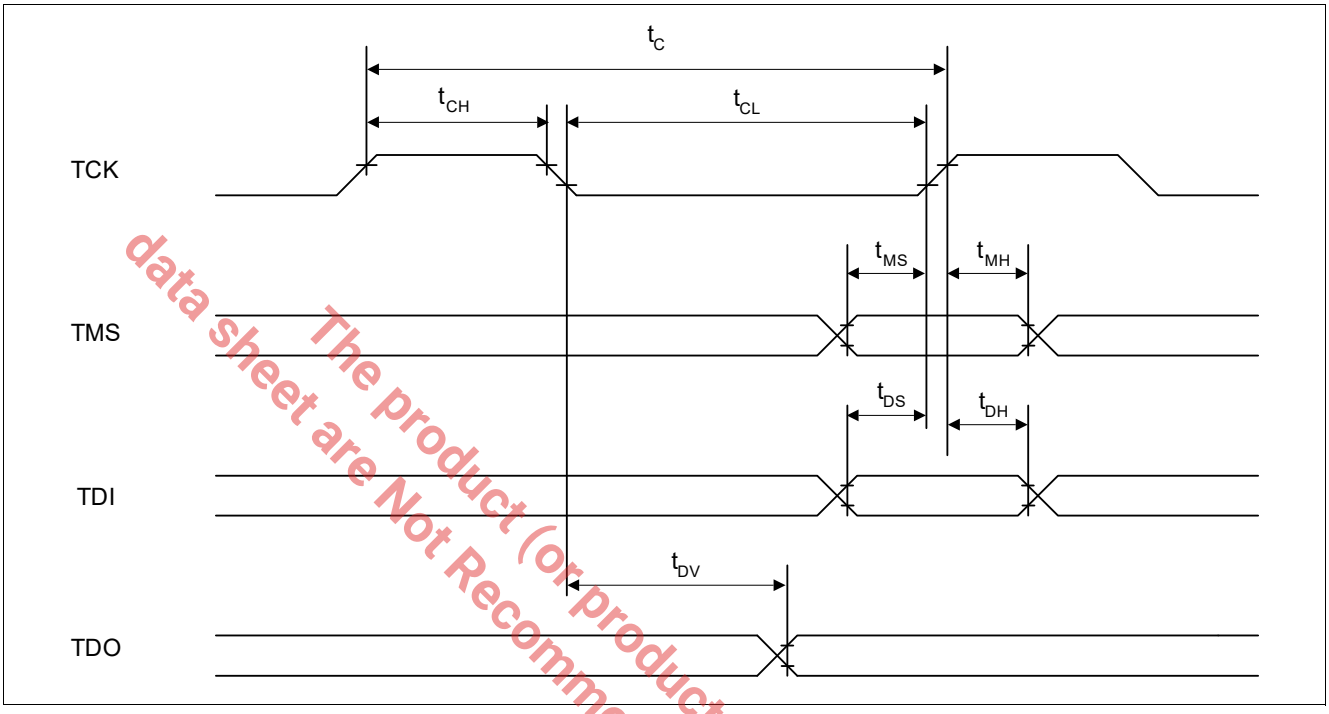



**Figure 28 Test Interface Timing**

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The product (or products) mentioned in this

Table 49 and Table 50 describe the timing values for the test interface.

**Table 49 Test Interface Clock**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK Clock Period | $t_C$ | 100 | – | – | ns | – |
| TCK High Time | $t_{CH}$ | 40 | – | – | ns | – |
| TCK Low Time | $t_{CL}$ | 40 | – | – | ns | – |

**Table 50 JTAG Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TMS Setup Time | $t_{MS}$ | 40 | – | – | ns | – |
| TMS Hold Time | $t_{MH}$ | 40 | – | – | ns | – |
| TDI Setup Time | $t_{DS}$ | 40 | – | – | ns | – |
| TDI Hold Time | $t_{DH}$ | 40 | – | – | ns | – |
| Hold: TRSTN After TCK | $t_{HD}$ | 10 | – | – | ns | – |
| TDO Valid Delay | $t_{DV}$ | – | – | 60 | ns | – |

### 7.7.7 Differential Reference Clock Interface

Table 51 describes the CML differential reference clock output.

**Table 51 Reference Clock Output Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Reference Clock Frequency | – | -300 | – | +300 | ppm | – |
| Clock Rising Edge Rate | $t_{rise}$ | 0.62 | 1 | 2 | V/ns | -150 mv to 150 mv |
| Clock Falling Edge Rate | $t_{fall}$ | 0.62 | 1 | 2 | V/ns | -150 mv to 150 mv |
| Peak to Peak Jitter | $t_{ppjitter}$ | 0.5 | 1.2 | 1.7 | ps | 100 mV power noise on 1.8 V |
| Clock Duty Cycle | - | 45 | 50 | 55 | % | – |
| Output Voltage High | - | 0.25 | 0.4 | 0.5 | V | – |
| Output Voltage Low | - | 0 | 0.05 | 0.1 | V | – |
| Differential Output Voltage | - | 500 | – | 900 | mV | 2 * $\lvert V_{CLKP}-V_{CLKN}\rvert$ |
| Termination | - | 45 | – | 60 | Ω | |

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The product (or products) mentioned in this

### 7.7.8 Crystal Specification

The 25 MHz crystal must follow the specification given in Table 52.

**Table 52 Specification of the Crystal**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Frequency with 25 MHz Input | $f_{clk25}$ | – | 25.0 | – | MHz | – |
| Total Frequency Stability | – | -50 | – | +50 | ppm | Refers to the sum of all effects: such as general tolerance, aging, and temperature dependency |
| Series Resonant Resistance | – | – | – | 40 | Ω | – |
| Drive Level | – | – | 0.1 | 0.2 | mW | – |
| Load Capacitance | $C_L$ | 16 | – | 26 | pF | – |
| Shunt Capacitance | $C_0$ | – | – | 7 | pF | – |

data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

## 7.8 External Circuitry

This section specifies the component characteristics of the external circuitry connected to the TPIs of the MxL86280C.

### 7.8.1 Twisted-Pair Common-Mode Rejection and Termination Circuitry

Figure 29 shows the external circuitry necessary to properly terminate the common mode of the TPI.

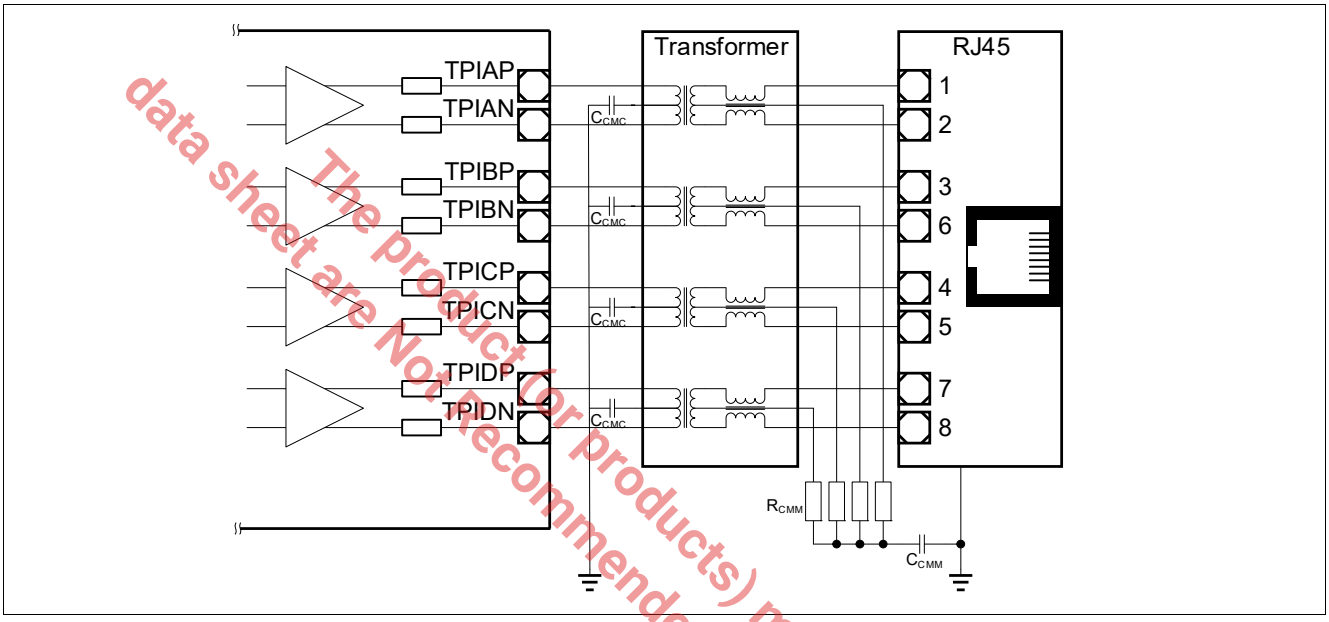



**Figure 29 Twisted Pair Common-Mode Rejection and Termination Circuitry**

Table 53 defines the component values and their supported tolerances.

**Table 53 Electrical Characteristics for Common-Mode Rejection and Termination Circuitry**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Common-Mode Decoupling Capacitance (Media End) | $C_{CMM}$ | 800 | 1000 | 1200 | pF | ±15%, 3 kV |
| Common-Mode Decoupling Capacitance (Chip End) | $C_{CMC}$ | 80 | 100 | 120 | nF | ±15%, 25 V |
| Common-Mode Termination Resistance (Media End) | $R_{CMM}$ | 67.5 | 75 | 82.5 | Ω | ±5% |

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The product (or products) mentioned in this

## 7.8.2 Transformer (Magnetics)

This section specifies the required electrical characteristics of the transformer[1)] devices that are supported. The specifications listed here guarantee proper operation according to IEEE 802.3 [2].

Figure 30 depicts a typical Gigabit Ethernet capable transformer device.

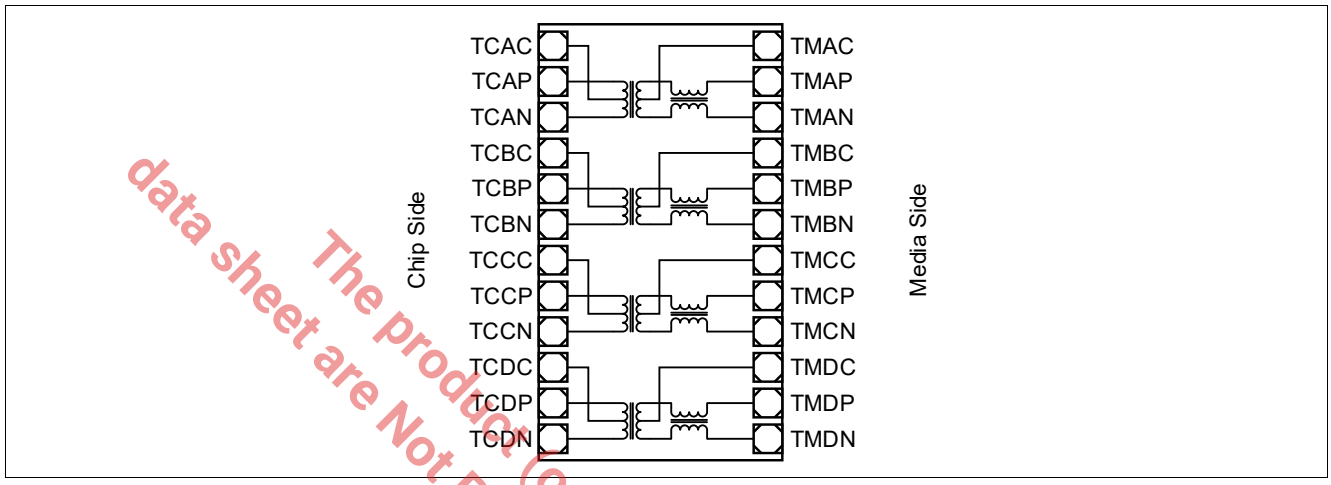



**Figure 30 Schematic of an Ethernet Transformer Device**

Table 54 lists the characteristics of the supported transformer devices. These characteristics represent the minimum values for achieving standard performance. Since the transformer significantly impacts the link performance, it is possible to increase the loop reach by selecting transformers with improved parameters.

**Table 54 Electrical Characteristics for Supported Transformers (Magnetics)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Turns Ratio | 1:tr | 0.95 | 1.00 | 1.05 | | ±5% |
| Differential-to-Common-mode Rejection | DCMR | 40 | – | – | dB | 30 MHz |
| | | 35 | – | – | dB | 60 MHz |
| | | 30 | – | – | dB | 100 MHz |
| Crosstalk Attenuation | CTA | 45 | – | – | dB | 30 MHz |
| | | 40 | – | – | dB | 60 MHz |
| | | 35 | – | – | dB | 100 MHz |
| Insertion Loss | IL | – | – | 1 | dB | 1 MHz ≤ f ≤ 250 MHz |
| Return Loss | RL | 16 | – | – | dB | 1 MHz ≤ f ≤ 40 MHz |
| Return Loss | RL | 16-10*log10(f/40) | – | – | dB | 40 MHz ≤ f ≤ 250 MHz |

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1) Also often referred to as magnetics.

### 7.8.3 RJ45 Plug

Table 55 describes the electrical characteristics of the RJ45 plug to be used in conjunction with MxL86280C.

**Table 55 Electrical Characteristics for Supported RJ45 Plugs**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Crosstalk Attenuation | CTA | 45 | – | – | dB | 30 MHz |
| | | 40 | – | – | dB | 60 MHz |
| | | 35 | – | – | dB | 100 MHz |
| Insertion Loss | IL | – | – | 1 | dB | 1 MHz ≤ f ≤ 250 MHz |
| Return Loss | RL | 16 | – | – | dB | 1 MHz ≤ f ≤ 40 MHz |
| Return Loss | RL | 16-10*log10(f/40) | – | – | dB | 40 MHz ≤ f ≤ 250 MHz |

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The product (or products) mentioned in this

# 8 Package Outline

The product is assembled in a PG-FCLBGA-277 package, which complies with regulations requiring lead free material. **Table 56** lists the parameters generated in accordance with JEDEC JESD51 standards **[3]**.

**Table 56 JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network**

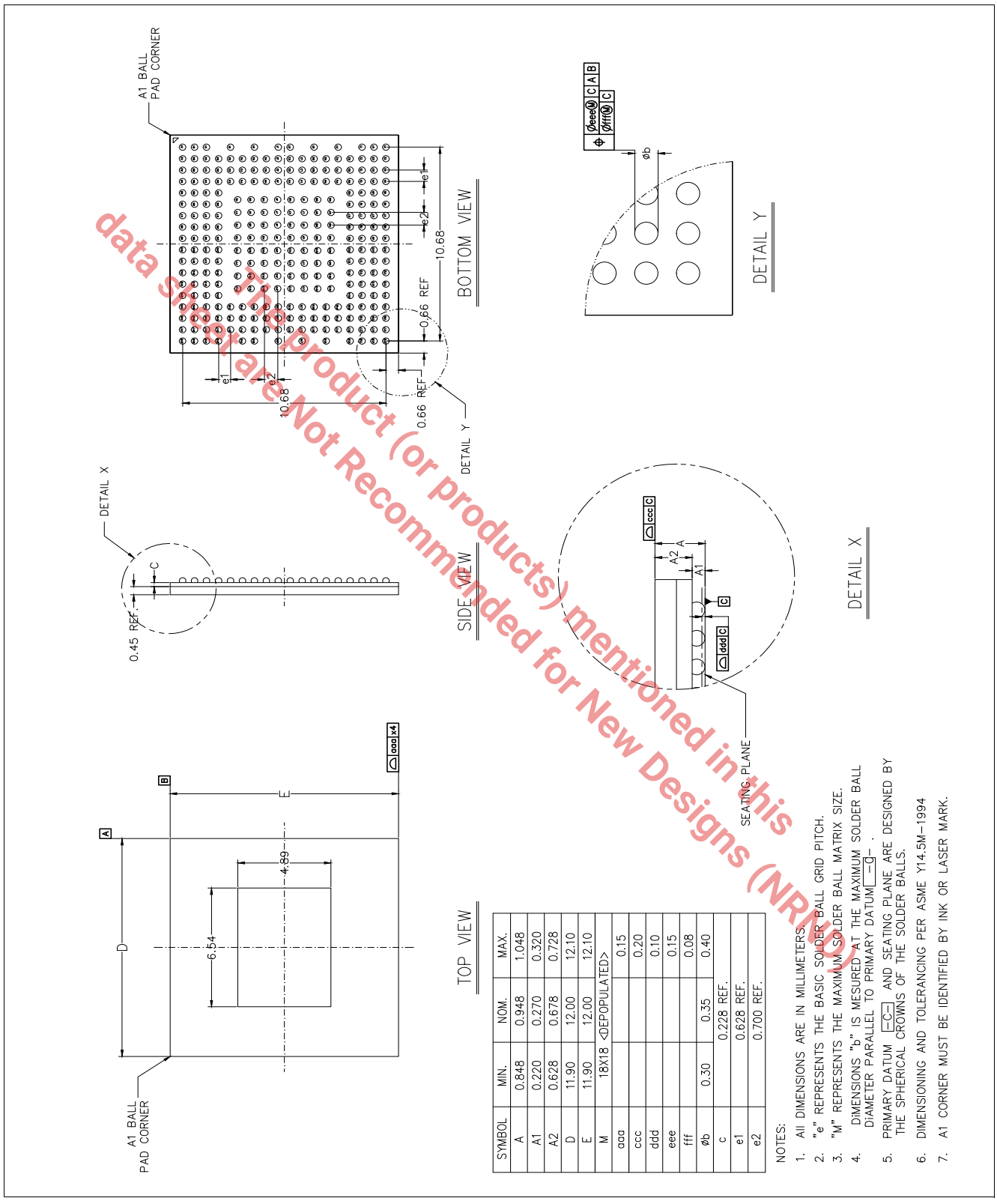
| Item | Name/Value |
|---|---|
| Thermal Resistance - Junction to Case Top | $R_{th,\ JCtop}$ = 0.082 K/W |
| Minimum Thermal Resistance - Junction to 0 mm from package edge on PCB | $R_{th,\ JB}$ = 2.70 K/W |

**Table 57 Stress Force Package Parameter**

| Item | Value |
|---|---|
| Force | 1.939 kg |
| Pressure | 1.346528 kg/cm$^2$ |
| | 19.15207 PSI |

Data sheet are Not Recommended for New Designs (NRND) The product (or products) mentioned in this

**Figure 31** shows the mechanical drawings for this package. The dimensions are in millimeters.




| SYMBOL | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.848 | 0.948 | 1.048 |
| A1 | 0.220 | 0.270 | 0.320 |
| A2 | 0.628 | 0.678 | 0.728 |
| D | 11.90 | 12.00 | 12.10 |
| E | 11.90 | 12.00 | 12.10 |
| M | 18X18 <DEPOPULATED> | | |
| aaa | | | 0.15 |
| ccc | | | 0.20 |
| ddd | | | 0.10 |
| eee | | | 0.15 |
| fff | | | 0.08 |
| ϕb | 0.30 | 0.35 | 0.40 |
| e | | 0.228 REF. | |
| e1 | | 0.628 REF. | |
| e2 | | 0.700 REF. | |

NOTES:
1. All dimensions are in millimeters.
2. "e" represents the basic solder ball grid pitch.
3. "M" represents the maximum solder ball matrix size.
4. Dimensions "b" is mesured at the maximum solder ball diameter parallel to primary datum [-G-] .
5. Primary datum [-C-] and seating plane are designed by the spherical crowns of the solder balls.
6. Dimensioning and tolerancing per ASME Y14.5M–1994
7. A1 corner must be identified by ink or laser mark.

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**Figure 31 PG-FCLBGA-277 12 mm x 12 mm Package Outline**

# 9 Product Ordering Information

Table 58 provides the product ordering information.

**Table 58 Product and Package Naming**

| Marketing Part Number | Ordering Part Number | Shipping Format | Package | Device Number[1)] | Device Revision Number[2)] | PHY Identifier[3)] |
|---|---|---|---|---|---|---|
| MxL86280C | MXL86280C-ABE-T | Tray | PG-FCLBGA-277 | 0x11 | 0x8 | 0x5518 |

1) LDN field in CL22 and CL45 registers.
2) LDRN field in CL22 and CL45 registers.
3) PHY Identifier 2 register 16-bit value.

*Note: For more information about part numbers, as well as the most up-to-date information and additional information on environmental rating, go to https://www.maxlinear.com/products/interface/ethernet.*

data sheet are Not Recommended for New Designs (NRND)
The Product (or products) mentioned in this

## Literature References

[1] Ethernet Switch MxL862xx Unmanaged and Managed-Attached Configuration User Guide Rev. 1.0

***Attention: Refer to the latest revisions of the documents.***

## Standards References

[2] IEEE 802.3-2022: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, IEEE Computer Society, May 2022
https://standards.ieee.org/ieee/802.3/10422/

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data sheet are Not Recommended for New Designs (NRND)
The product (or products) mentioned in this

# Terminology

| | |
|---|---|
| **A** | |
| ADS | Auto-Downspeed |
| AFE | Analog Front End |
| ANEG | Auto-Negotiation |
| ANSI | American National Standards Institute |
| ASP | Analog Signal Processing |
| **B** | |
| BW | Bandwidth |
| **C** | |
| Cat 5 | Category 5 Cabling |
| CDB | Clock Distribution Block |
| CDR | Clock and Data Recovery |
| CML | Current Mode Logic |
| **D** | |
| DSP | Digital Signal Processing |
| DWRR | Deficit Weighted Round Robin |
| **E** | |
| EEE | Energy-Efficient Ethernet |
| EEPROM | Electrically Erasable Programmable ROM |
| EMI | Electromagnetic Interference |
| ESD | Electrostatic Discharge |
| **F** | |
| FCA | Flash Configuration Area |
| FCS | Frame Check Sequence |
| FLP | Fast Link Pulse |
| **G** | |
| GMII | Gigabit Media-Independent Interface |
| GPIO | General Purpose Input/Output |
| **H** | |
| HBM | Human Body Model |
| **I** | |
| $I^2C$ | Internally Integrated Circuit Interface (also I2C) |
| IC | Integrated Circuit |
| IEEE | Institute of Electrical and Electronics Engineers |
| **J** | |
| JTAG | Joined Test Action Group |
| **L** | |
| LAG | Link Aggregation Group |

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| | |
|---|---|
| LAN | Local Area Network |
| LED | Light Emitting Diode |
| LJPLL | Low Jitter Phase-Locked Loop |
| LPI | Low Power Idle |
| LSB | Least Significant Bit |
| **M** | |
| MAC | Media Access Controller |
| MDI | Media-Dependent Interface |
| MDIO | Management Data Input/Output |
| MDIX | Media-Dependent Interface Crossover |
| MMD | MDIO Manageable Device |
| MSB | Most Significant Bit |
| **N** | |
| NLP | Normal Link Pulse |
| **O** | |
| OSI | Open Systems Interconnection |
| OUI | Organizationally Unique Identifier |
| **P** | |
| PCB | Printed Circuit Board |
| PCS | Physical Coding Sublayer |
| PD | Power Down |
| PFC | Priority Flow Control |
| PHY | Physical Layer (device) |
| PLL | Phase-Locked Loop |
| PMA | Physical Media Attachment |
| **Q** | |
| QSPI | Quad Serial Peripheral Interface |
| **R** | |
| Rx | Receive |
| **S** | |
| SerDes | Serializer-Deserializer |
| SFP | Small Form-Factor Pluggable |
| SMD | Surface Mounted Device |
| SoC | System on Chip |
| SP | Strict Priority |
| STA | Station Management Entity (MAC SoC) |
| SVN | Security Version Number |
| **T** | |
| TLE | Transformerless Ethernet |
| TPG | Test Packet Generator |

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| | |
|---|---|
| TPI | Twisted Pair Interface |
| Tx | Transmit |
| **W** | |
| WoL | Wake-on-LAN |
| WRED | Weighted Random Early Detection |
| **X** | |
| XO | Crystal Oscillator |

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